Low Power System-on-Chip Design Lab.

In System-on-Chip (SoC) design, increasing thermal densities and the portability of emerging computing systems demand further reduction of design power. However, in integrated-circuit (IC) designs, there is a tradeoff between energy and performance, and the solution space for any given design is bounded by the lowest possible energy and the highest possible performance. To extend the achievable energy-performance envelope, Low Power SoC Design Lab is focused on system- and design-level techniques such as (i) error-resilient design, (ii) dynamic voltage and frequency scaling (DVFS), (iii) approximate arithmetic design, and (iv) adaptive power gating. Our research proposes innovative techniques which exploit the system and application information, and connect them into design optimization and physical implementation to enable more energy-efficient designs.

Research Keywords
System-on-Chip, Low Power, Computer-aided Design, Physical implementation

Research interests
Energy-efficient SoC/VLSI design, adaptive and resilient design, system and application-aware optimization, IC physical implementation

On going research Topics (selected)
1. Exploiting error resilience in low-power design
2. Approximate arithmetic design

Research Publications (selected)

Patents (selected)