Open-Source Digital EDA Today

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Open-Source EDA: 2018 Activity

• DAC-2018 “Birds of a Feather” meeting
  • [https://drive.google.com/open?id=1k1s5yQs0b7U4dWwnfWarwmKyMrGAyA3I](https://drive.google.com/open?id=1k1s5yQs0b7U4dWwnfWarwmKyMrGAyA3I)
  • Inventory (maintained by Minsoo Kim, [msk226@eng.ucsd.edu](mailto:msk226@eng.ucsd.edu))
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• Lots of well-known source codes
  • Open-source flow to support tapeout down to ~130nm, limited scale: qflow
  • Logic synthesis: ABC, yosys
• Please help improve this inventory, which helps point out gaps, avoid reinventing wheels
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<table>
<thead>
<tr>
<th>CATEGORY</th>
<th>Tool</th>
<th>Tool provider</th>
<th>Download URL</th>
<th>Created</th>
<th>License type</th>
<th>Inputs</th>
<th>Dev. Status</th>
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<tbody>
<tr>
<td>Logic Synthesis</td>
<td>yosys</td>
<td>Clifford Wolf</td>
<td><a href="http://www.clifford.at/yosys/">http://www.clifford.at/yosys/</a></td>
<td>2017</td>
<td>ISC (MIT/BSD like)</td>
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<td></td>
<td>ABC</td>
<td>Alan Mishchenko</td>
<td><a href="https://people.eecs.berkeley.edu/~alanmi/abc/">https://people.eecs.berkeley.edu/~alanmi/abc/</a></td>
<td>2005</td>
<td>GNU (?)</td>
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<td>CirKit</td>
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<td><a href="https://github.com/msoeken/cirkit">https://github.com/msoeken/cirkit</a></td>
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<td></td>
<td>GrayWolf</td>
<td>Ruben Undheim</td>
<td><a href="https://github.com/rubund/graywolf">https://github.com/rubund/graywolf</a></td>
<td>2014</td>
<td>GPL (license TBD)</td>
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<td></td>
<td>NTUPlace 2.0</td>
<td>National Taiwan University</td>
<td><a href="http://eda.ee.ntu.edu.tw/research.htm">http://eda.ee.ntu.edu.tw/research.htm</a></td>
<td>2012</td>
<td>GPL 2.0</td>
<td>Active</td>
<td>Last update: 2012</td>
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<tr>
<td>Clock Tree Synthesis</td>
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<tr>
<td>Global Routing</td>
<td>NTHU</td>
<td>NTHU</td>
<td><a href="https://github.com/luckyrantanplan/nthu-route">https://github.com/luckyrantanplan/nthu-route</a></td>
<td>2008</td>
<td>GPL 3.0</td>
<td>Academic</td>
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<tr>
<th>Static Timing Analysis</th>
<th>OpenTimer</th>
<th>UIUC</th>
<th><a href="https://web.engr.illinois.edu/~thuang19/software/timer/OpenTimer.html">https://web.engr.illinois.edu/~thuang19/software/timer/OpenTimer.html</a></th>
<th>2014 GPL V3.0</th>
<th>Industry: .lib, .v, .spef, .sdc, .lef, .def</th>
<th>Active</th>
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</thead>
<tbody>
<tr>
<td>Several academic STA tools</td>
<td></td>
<td></td>
<td><a href="https://sites.google.com/site/taucontest2017/resources">https://sites.google.com/site/taucontest2017/resources</a></td>
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<th>Global Routing</th>
<th>EnRouter</th>
<th>University of Calgary/Waterloo</th>
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<tbody>
<tr>
<td></td>
<td>Ophidian</td>
<td>Federal University of Santa Catarina</td>
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<td>Proton</td>
<td>efabless</td>
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<td>Full design flow</td>
<td>flow to stitch existing KAIST</td>
<td><a href="https://github.com/jinwookjungs/date_robust_design">https://github.com/jinwookjungs/date_robust_design</a></td>
<td>2017 Unclear</td>
<td>Academic contests</td>
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<td>FPGA-SPICE</td>
<td>from VPR to SPICE</td>
<td>University of Utah</td>
<td><a href="https://sites.google.com/site/peagallard/fpga-spice">https://sites.google.com/site/peagallard/fpga-spice</a></td>
<td>2015</td>
<td>License not defined</td>
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<td>verilog simulator</td>
<td>icarus verilog</td>
<td>Tim Edwards</td>
<td>?</td>
<td></td>
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Library

Library Prep | OpenRAM Memory Compiler/Characterizer | http://openram.soec.ucsd.edu
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  - + good discussion of blockers, key gaps, goals for next year, …

- WOSET-2018
  - Flows: DATC RDF, CloudV, efabless
  - Open-source codes: logic synthesis, circuit analysis / simulation, static timing
  - Perspectives on open-source EDA: ARL/UT experiences, IBM sustainable OS
  - Panel 4:30pm – 5:00pm (Olofsson, Stok, Edwards, Renau): users, gaps/blockers, mindsets …
• Goal of open-source: should be chips, not just papers

• Wishlists/Gaps:
  • DRC, PDKs
  • Restrictions on commercial use
  • Parsers (.sdc, .v, ...)
  • Lots of “contest binaries” in P&R space, very little high-quality open source
  • Lack of excellent database / full context
• **Goal of open-source:** should be chips, not just papers
  • → read industry PDKs and design data; tapeout-capable; analysis in “ballpark”

• **Wishlists/Gaps:**
  • DRC, PDKs → blocker for validations, regressions
  • Restrictions on commercial use → solved by permissive open-source license
  • Parsers (.sdc, .v, …) → solved by [https://github.com/abk-openroad/OpenSTA](https://github.com/abk-openroad/OpenSTA)
  • Lots of “contest binaries” in P&R space, very little high-quality open source → but see following slide
  • Lack of excellent database / full context → true that
“Almost Almost There” poster

**PDN / Floorplan**
- MACRO placement guided by timing-aware mixed-size placement from RePLAce
- Power delivery network (PDN) to all standard cells, MACROS and peripheral IO cells
- Delivered as DEF to RePLAce that localizes standard cell locations with fixed-macro placement and PDN

**Clock Tree Synthesis**
- Based on the "Generalized H-tree" method
- Deliver modified Verilog and buffer placements
  - RePLAce incrementally localizes
- Support for 28/16nm
  - PDK characterization
  - Algorithm tuning

**Placement (RePLAce)**
- Based on the analogy between placement and electrostatic system
  - Nestrov's method to solve the nonlinear placement problem with runtime step length prediction to resolve runtime bottleneck
  - Estimated SPEF feedback to timer to make placer timing aware / driven

**Global Routing**
- Lack of industry standard format of GR solution
- Interoperability
  - ISPD 2018 Contest Format
  - Back out route guides from commercial detailed router solution

**Sizer (TritonSizer)**
- UCSD sizer for leakage / dynamic power recovery, timing recovery
- Commercial timers are used for correlation by using TID socket interface
  - Primed Time, Tempo, OpenSTA can be used as a golden timer

**Detailed Routing (TritonRoute)**
- Parallel, MILP-based panel routing
- Inter-layer sequential routing
  - From bottom to top, layer by layer
  - Down via assignment in upper-layer routing
- Intra-layer parallel routing
  - Non-overlapping, unit-width panel along preferred direction
  - Parallel routing for alternative panels

- OpenROAD WIP
  - theopenroadproject.org
- "Almost" ???
  - Calls ILP solvers
    - One-time setup per PDK (PDN, CTS...) → a user must TOFTT
  - Brittle, limited field of use
- "There" ???
  - 16FFC
    - Small SOC
    - Tapeout capable
      - well taps, antennas, fill, sealring, GDS merge …
  - Open source
  - Not "There" yet!
  - Progress
  - Working hard

A. B. Kahng, 181108 WOSET
Worth Recalling … (DAC-2018 B-o-F) [digital]

- Goal of open-source: should be chips, not just papers
  - read industry PDKs and design data; tapeout-capable;

- Wishlists/Gaps:
  - DRC, PDKs → blocker for validation
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  - Parsers (.sdc, .v, …)
  - Lots of “contest binaries” in P&R space, very little high-quality open source
    - but see following slide
  - Lack of excellent database / full context

- Three doable things by November’s WOSET?
  - Open-source flow(s): e.g., RTL through detailed route in […] PDK
  - […] / subsystem benchmark [top-500, calibration, …]
  - Clean / complete “inventory” [clarifying “gaps”?]
Goal of open-source: should be chips, not just papers
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Wishlists/Gaps:
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Three doable things by November’s WOSET?
- Open-source flow(s): e.g., RTL through detailed route in [... PDK]
  - [consistent / uniform interfaces]
- Open-source digital SOC / subsystem benchmark [top-500, calibration, …]
- Clean / complete “inventory” [clarifying “gaps”?]
→ How are we doing? Let’s see today!
• A **non-technical gap**: mindsets, culture, personalities

• Digital EDA research still in dark ages *e.g.*, *by construction and by agreement*, our “scientific results” are not reproducible!
  - Bookshelf, METRICS, Capo, MLPart, ORION2/3, CACTI, … RePIAce, … *TritonRoute* … → where was downside from open-sourcing?

• Do we care more about next paper, or credit, or future of the EDA field and semiconductor industry?

• Local optimizations → “tragedy of the commons”

• “OSET”: “Think globally. Act locally.”