Context: DARPA OpenROAD

- **OpenROAD = DARPA IDEA project**
  - 24 hour turnaround for RTL to GDS
  - No human intervention
  - Design guidance: floorplan, power, etc.
  - Runtime guidance: early stop for doomed runs
  - "Self-driving" flow must support modeling, prediction of tools and designs -> "machine learning"
- **Target 1: Tapeout capable in 16nm**
  - LVS and DRC clean
- **Target 2: Bounded performance, power and area (PPA) loss**
  - 10X for alpha release in 2019 (?)
  - Few X PPA compared to commercial EDA outcomes is the IDEA program

Starting Points

- **From CAD contests**
  - Sizer: ISPD 2013 Discrete Gate Sizing Contest
  - Detailed Router: ISPD 2018 Initial Detailed Routing Contest
- **From academic research**
  - Global Placer: RePlAce: Improved Solution Quality and Validation of Routable Placements
  - CTS: Optimal Generalized H-Tree Topology and Buffering for High-Performance and Low-Power Clock Distribution
- **From commercial partner**
  - Static Timer: OpenSTA from Parallax Software
  - Tools from contests / papers support contest / academic format only
  - Cannot communicate to each other or the real world!

Looking Ahead

- **Richer design space in real life**
  - Multiple power / clock domains in real designs
  - Flexible PDN / clock tree structure
- **Complex advanced-node design rules, syntax**
  - LEF/DEF reference in 2010 had 472 pages
  - LEF/DEF reference today has 858 pages!
- **Challenge: tapeout-clean design**
  - Routability is an issue in advanced node
  - Detailed placer and global router can (must) help improve routability
- **Challenge: performance of design**
  - Even "safe by construction" timing requires close interaction among timer, placer, router

Current State

- **File-based flow using industry formats**
  - No other possible flow in absence of database
  - Industry tools = "backplane" for trial integrations
  - Use industry tools, save off DB between flow steps
  - Swap in open-source tool to drive development
- **Some of our tools are open-sourced on GitHub**
  - Placer: https://github.com/abk-openroad/RePlAce
  - Timer: https://github.com/abk-openroad/OpenSTA
  - Sizer: https://github.com/abk-openroad/TritonSizer
  - "Almost Almost-There" flow exists today
  - Goes through netlist to routed def -> Not clean yet!

Getting from Here to There

- **Freedoms from Choice !**
  - Restricted methodology, e.g., templates for PDN
  - Simple, predictable heuristics
    - E.g., generalized H-tree topologies
  - Must restrict solution space for viability
    - Unidirectional, min-width routing for signal nets
    - NDR allowed for power, clock nets only
  - Limit field of use as well
    - E.g., ≤ 3 clocks

PDN / Floorplan

- **MACRO placement guided by timing-aware mixed-size placement from RePlAce**
- Power delivery network (PDN) to all standard cells, MACROS and peripheral IO cells
- Delivered as DEF to RePlAce that legalizes standard cell locations with fixed-macro placement and PDN

Placement (RePlAce)

- Based on the analogy between placement and electrostatic system
- Nesterov’s method to solve the nonlinear placement problem with runtime step length prediction to resolve runtime blowup
- Estimated SPEF feedback to timer to make placer timing aware / driven

Sizer (TritonSizer)

- UCSD sizer for leakage / dynamic power recovery, timing recovery
- Commercial timers are used for correlation by using Tcl socket interface
  - PrimeTime, Tempus. OpenSTA can be used as a golden timer

Clock Tree Synthesis

- Based on the "Generalized H-tree" method
- Deliver modified Verilog and buffer placements
  - RePlAce incrementally legalizes
  - Support for 18/16nm
    - PDK characterization
    - Algorithm tuning

Global Routing

- Lack of industry standard format of GR solution
- Interoperability
  - ISPD 2018 Contest Format
  - Back out route guides from commercial detailed router solution

Detailed Routing (TritonRoute)

- Parallel, MILP-based panel routing
- Inter-layer sequential routing
- From bottom to top, layer by layer
- Down via assignment in upper-layer routing
- Intra-layer parallel routing
- Non-overlapping, unit-width panel along preferred direction
- Parallel routing for alternative panels

Design rules supported by commercial tools

Design rules supported in restricted scope

Width routing for signal nets