Noise and Delay Estimation for Coupled RC Interconnects

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Abstract

The performance of high-speed VLSI circuits is increasingly limited by interconnect coupling noise. We provide improved, easily computable estimates of crosstalk peak noise, as well as impact of coupling on aggressor delay, for distributed RC interconnects. Our approach is based on better modeling of the distributed interconnects, as well as more detailed analyses for both the step input and ramp input regimes. We analyze both L and Π interconnect models in deriving analytic expressions for peak noise and delay. We also handle both step and ramp inputs, so that our approach is strictly more general and accurate than previous methods in the literature, notably [8] [5]. Noise estimates obtained with the Π model are within 13% of SPICE simulation results, and in practice the L model provides an upper bound and the Π model provides a lower bound on the peak noise estimation as compared to SPICE simulation results. The substantial accuracy improvements that we obtain can lead to less over-design and guard-banding in high-performance system designs.

1 Introduction

Interconnects are an important performance limiting factor in today's high-speed and high-density VLSI designs. A major reason for this is the increasing importance of crosstalk between parallel RC interconnect lines [1] [6]. This crosstalk is due to the capacitive coupling between lines (which increases as the average length of interconnects and the density of interconnect routings increase), and to the faster switching speeds of devices.

Today's timing analysis tools employ a simple technique which takes the coupling capacitance to be some multiple of grounded capacitance depending upon the switching conditions. A single effective capacitance value for the interconnect is computed for use in delay and noise estimation. This is multiplied by a *switching factor*, which is taken to be slightly more than zero for a pair of lines switching in the same direction, and slightly less than two for a pair of lines switching in the opposite direction. The downside of this simple technique is that it can lead to highly optimistic or pessimistic analyses of noise. This motivates the development of more accurate predictors of noise and coupling-induced delay based on coupling capacitance values and switching activity (slew times, offsets).

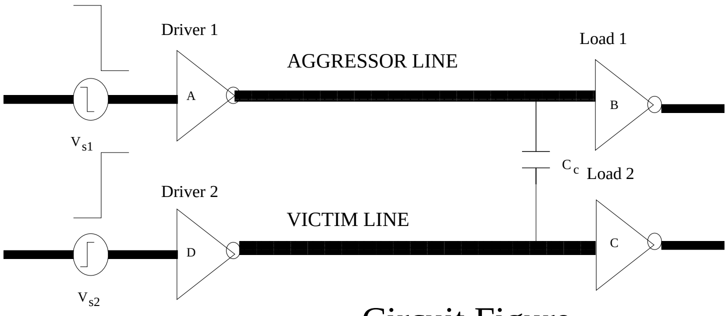
Several notable previous works model the effects of interconnect fringing and coupling capacitance on delay and crosstalk. Vittal et al. [8] use an L model for RC interconnects and obtain delay and noise bounds for the case of a step input only. Also, their model does not take into account the interconnect resistance while deriving noise expressions. Kawaguchi and Sakurai [5] use the diffusion equations for analyzing capacitively coupled interconnects, but also analyze only the case of a step input. In addition, they make several assumptions while deriving the final expressions for the noise and delay. E.g., they assume $R_{driver} << R_{int}$ and $C_{load} << C_{int}$. The results of [5] are a special case of results of [8], and the equations from [5] reduce to those of [8] when the driver resistance is made zero. Also, they evaluate different cases of possibilities of ratios of resistances, capacitances, etc. separately, and make few assumptions in each derivation. Shepard et al. [7] obtain noise estimates that are dependent on input slew, but the interconnect model is again a simple L model. Yee et al. [9] present simulation results that document the magnitude of crosstalk-induced delay. Devgan [2] presents a metric for fast estimation of noise based on electrical properties of circuits, but the estimation error increases as the rise time decreases.

In this paper, we present improved estimators for noise and delay phenomena due to coupling capacitance. We use a distributed Π model for RC interconnects, which is more accurate than the L model used in [7] [8]. We also derive expressions for ramp inputs in addition to step inputs. Our approach analyzes circuits in the frequency domain and then obtains time domain results by taking the inverse Laplace transform. For a step input waveform and an L model of the interconnect, our expressions reduce to those derived in [8]. Thus, in light of the previous literature, we are the first to provide a complete set of analytic estimators for both L and Π models of the interconnect, for both step and ramp inputs, and for both peak noise and coupling delay estimation. The improved accuracy of our estimators can (i) be useful in analyzing the sensitivity of circuit performance to various interconnect tuning parameters, and (ii) lead to less over-design and guard-banding in high-performance designs, at all stages of a performance-convergent synthesis and layout methodology.

The remainder of this paper is organized as follows. Section 2 describes the circuit model and the notation used in our analysis. Section 3 presents the analysis of noise and delay due to coupling for the L model of interconnect. Section 4 presents the analysis of noise and delay due to coupling for the Π model of interconnect. Simulation results are presented in Section 5, and Section 6 concludes with directions for future work.

2 Preliminaries and Notation

We consider two parallel coupled interconnects with drivers and loads attached, as shown in Figure 1. Equivalent circuits using L and Π models for the interconnects are shown in Figures 2 and 4, respectively. We analyze noise and delay at nodes C and B. Although for simplicity we consider just one aggressor line, our analyses extend easily to the case of more than one aggressor line for a given victim line. Our goal is to develop models to estimate peak noise on the victim line, and delay on both aggressor and victim lines, for three main cases: (i) victim line quiet, (ii) victim line active and switching in the



Circuit Figure

Figure 1: Two parallel coupled interconnects, with inverters as drivers and loads. This configuration is used for our analysis of peak noise on the victim, and delay on both aggressor and victim.

Model Type	State of Line		Switching Directions on Lines	Input Waveform	Section in Paper
	Victim	Aggressor			
L	Quiet	Active	-	step	3.1.1
	Quiet	Active		ramp	3.1.2
	Active	Active	opposite	step	3.2.1
	Active	Active	opposite	ramp	3.2.2
	Active	Active	same	step	3.3.1
	Active	Active	same	ramp	3.3.2
Π	Quiet	Active	-	step	4.1.1
	Quiet	Active		ramp	4.1.2
	Active	Active	opposite	step	4.2.1
	Active	Active	opposite	ramp	4.2.2
	Active	Active	same	step	4.3.1
	Active	Active	same	ramp	4.3.2

Table 1: Detailed outline of cases addressed in Sections 3 and 4.

opposite direction to the aggressor, and (iii) victim line active and switching in the same direction as the aggressor. These cases are addressed in Sections 3 and 4, as outlined in Table 1.

The following notation is used in our discussion (see Figures 2 and 4).

aggressor line: interconnect whose switching affects the voltage level on another interconnect parallel to it

victim line: interconnect parallel to the aggressor line and whose voltage is affected by the switching of the aggressor line

$v_B(t)$: voltage at node B in time domain

$V_B(s)$: voltage at node B in transform domain

v_0: supply voltage

v_{peak}: peak noise voltage

R_{d1}: driver on-resistance of aggressor line

R_{d2}: driver on-resistance of victim line

R_1: resistance of aggressor line

R_1': resistance of victim line

C_1: metal to ground capacitance of aggressor line in L model (includes load capacitance), or first of the two capacitances of the aggressor line in the distributed Π model

C_1': metal to ground capacitance of victim line in L model (includes load capacitance), or first of the two capacitances of the victim line in the distributed Π model
C_2: second of the two metal to ground capacitances in the Π model of the aggressor line (also includes load capacitance)
C_2': second of the two metal to ground capacitances in the Π model of the victim line (also includes load capacitance)
C_{c1}: coupling capacitance between the lines when the L model of interconnect is used, or first capacitance of the distributed Π model of interconnect
C_{c2}: second capacitance of the distributed Π model of interconnect
t_{peak}: time at which the peak noise voltage is reached
T_S^I: slew time at the input of driver
T_S^O or T_S: slew time at the output of driver[1]

3 Noise and Delay Estimation Using the L Model for Interconnect

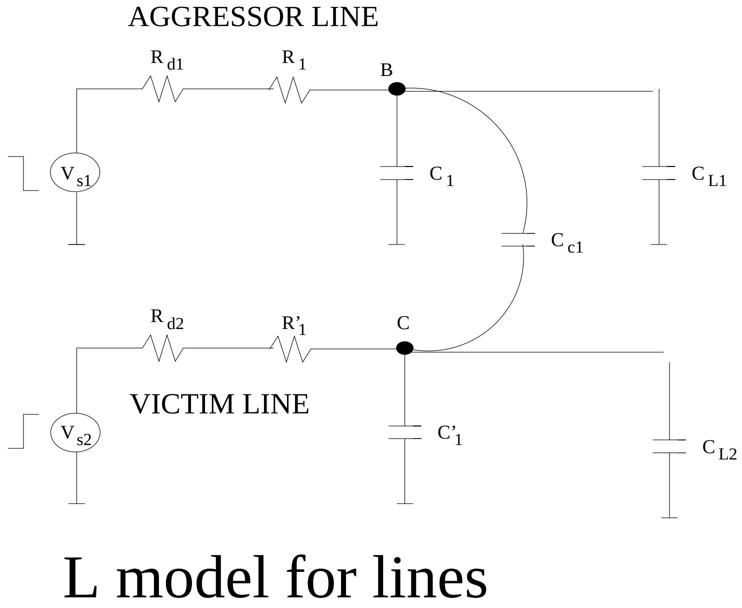


Figure 2: Equivalent circuit (using L model for interconnect) for the configuration of Figure 1.

In this section, we use the L model to represent the RC interconnect between the driver and the load as shown in Figure 2. To estimate the noise peak on the victim line due to the aggressor line, the first subsection studies the case when the victim line is quiet and the aggressor line is switching. The second subsection studies the case when both the victim and aggressor lines are switching in opposite directions; this case is used to estimate the worst-case interconnect delays on both the lines. Finally, the third subsection studies the case when both the victim and aggressor lines are switching in

[1]Note that the notation T_S is used exclusively to represent the *output* slew time of the driver.

the same direction; this case is used to estimate the best-case interconnect delays on both the lines. Our analyses address both the step and ramp input regimes, and we take driver resistance and load capacitance into account when deriving expressions for peak noise and delay. Our noise peak expression for step input reduces to the result obtained in [8] when interconnect resistance is set to zero.

3.1 Victim Quiet and Aggressor Switching

Since noise can cause false switching and incorrect functionality, it is essential to predict and correct for noise peaks. We now obtain an analytical expression for peak noise. In practice, this noise peak estimated via the L model can be taken as an upper bound when compared with SPICE simulation results.

To calculate the noise on the victim line we assume that the victim line is quiet and the aggressor line is switching as shown in Figure 3. In the circuit model of Figure 2, we compute the voltage at the aggressor line output, i.e., at node C. Using the nodal equations at B and C we obtain the following expression for voltage on aggressor and victim line in the frequency domain:[2]

$$V_B = V_{S1}\frac{1 + a_1 s}{1 + sM_1 + s^2 M_2} \tag{1}$$

$$V_C = V_{S1}\frac{a_2 s}{1 + sM_1 + s^2 M_2} \tag{2}$$

where

$$\begin{aligned} M_1 &= [(R_{d1} + R_1)(C_1 + C_{c1}) + (R_{d2} + R_1')(C_1' + C_{c1})] \\ M_2 &= (R_{d1} + R_1)(R_{d2} + R_1')(C_1 C_{c1} + C_{c1} C_1' + C_1' C_1) \\ a_1 &= (R_{d2} + R_1')(C_1' + C_{c1}) \\ a_2 &= (R_{d2} + R_1')C_{c1} \end{aligned} \tag{3}$$

We now compute the noise peak on victim line by considering step and ramp inputs at the inputs of the of aggressor line.

3.1.1 Step Input Analysis

Consider an aggressor line switching from low to high and a quiet victim line (i.e., input voltage remains constant), as shown in Figure 3(a). For the quiet line, the input voltage $V_{s2} = 0$ and for the aggressor line with step input, we have $V_{S1} = \frac{v_0}{s}$. The voltage at node B and C in time-domain is given by

$$v_B(t) = v_0\left(1 + k_1 e^{s_1 t} + k_2 e^{s_2 t}\right) \tag{4}$$

$$v_C(t) = v_0 \frac{a_2}{M_2(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right) \tag{5}$$

where $k_1 = \frac{1 + a_1 s_1}{s_1 M_2 (s_1 - s_2)}$, $k_2 = -\frac{1 + a_1 s_2}{s_2 M_2 (s_1 - s_2)}$, $s_{1,2} = \frac{-M_1/M_2 \pm \sqrt{(M_1/M_2)^2 - 4/M_2}}{2}$. The peak noise is computed by differentiating Equation (5) with respect to t and equating to zero. The time at which peak voltage is reached is given by

$$t_{peak} = \frac{1}{(s_1 - s_2)}\ln(s_2/s_1) \tag{6}$$

[2]Note that the capacitances C_1 and C_1' includes the load capacitances at the end of the line (i.e., C_{L1} or C_{L2}).

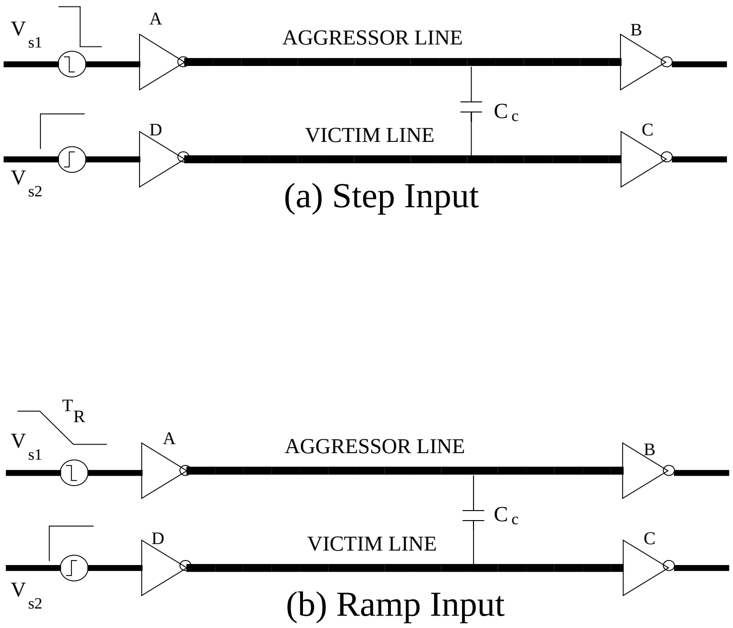


Figure 3: Case when the victim line is quiet: (a) step input, and (b) ramp input.

and the peak voltage is

$$v_{peak} = \frac{a_2 v_0}{M_2(s_1 - s_2)} \left(\frac{s_2}{s_1}^{\frac{s_1}{(s_1-s_2)}} - \frac{s_2}{s_1}^{\frac{s_2}{(s_1-s_2)}} \right) \tag{7}$$

However, by approximating the voltage at node C to first order approximation, we get $v_C(t) = \frac{v_0\,(R_{d2} + R_1')\,C_{c1}}{M_1} e^{-\frac{1}{M_1}t}$ and the approximate peak noise amplitude on the victim is

$$v_{UB} = \frac{v_0 a_2}{M_1} = \frac{v_0\,(R_{d2} + R_1')\,C_{c1}}{M_1} \tag{8}$$

Later, in the discussion we show that the above obtained peak noise expression yields an upper bound on the peak noise values when compared to SPICE results. Hence, we refer this model as L_{UB} in our discussion. Now, if we do not consider interconnect resistance, so that R_1 and R_2 are set to zero, the circuit model becomes the same as that of [8] and the peak voltage reduces to $v_{peak} = \frac{v_0}{(1 + C_1'/C_{c1} + R_{d1}/R_{d2}(1 + C_1/C_{c1}))}$. Hence, our derivation of v_{peak} by considering interconnect resistance yields a more general expression for noise peak voltage than that of [8].

3.1.2 Ramp Input Analysis

We now extend the derivation to the case of a ramp input voltage at the source of aggressor line. The ramp input voltage in the transform domain is expressed as $V_{S1} = \frac{v_0}{s^2 T_S}\left(1 - e^{-sT_S}\right)$ where T_S is slew time of the ramp input [3]. Substituting for V_{S1}, the frequency domain expression for the voltage at node C can be written as

$$V_C(s) = \frac{v_0}{s^2 T_S}\left(1 - e^{-sT_S}\right) * \frac{a_2 s}{1 + sM_1 + s^2 M_2} \tag{9}$$

The above equation can be reduced further by applying partial fractions, i.e.,

$$v_C(t) = \begin{cases} \frac{v_0 a_2}{T_S}\left[1 + \frac{1}{M_2 s_1(s_1-s_2)}e^{s_1 t} - \frac{1}{M_2 s_2(s_1-s_2)}e^{s_2 t}\right] & t \leq T_S \\ \frac{v_0 a_2}{T_S}\left[\frac{1}{M_2 s_1(s_1-s_2)}\left(e^{s_1 t} - e^{s_1(t-T_S)}\right) - \frac{1}{M_2 s_2(s_1-s_2)}\left(e^{s_2 t} - e^{s_2(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{10}$$

The time at which $v_C(t)$ reaches peaks is computed using the $v_C(t)$ expression for $t > T_S$ as $t_{peak} = \frac{1}{(s_1 - s_2)} \ln\left(\frac{1 - e^{-s_2 T_S}}{1 - e^{-s_1 T_S}}\right)$. The corresponding expression for peak voltage is

$$v_{peak} = \frac{v_0 a_2}{T_S}\left[\frac{(1 - e^{-s_1 T_S})}{M_2 s_1(s_1 - s_2)}\left(\frac{1 - e^{-s_2 T_S}}{1 - e^{-s_1 T_S}}\right)^{s_1/(s_1-s_2)} - \frac{(1 - e^{-s_2 T_S})}{M_2 s_2(s_1 - s_2)}\left(\frac{1 - e^{-s_2 T_S}}{1 - e^{-s_1 T_S}}\right)^{s_2/(s_1-s_2)}\right] \tag{11}$$

Again, we compute the upper bound on the peak noise value by approximating the voltage at node C to first moment as

$$v_{UB} = \frac{v_0\,(R_{d2} + R_1')\,C_{c1}}{T_S}\left[1 - e^{-T_S/M_1}\right] \tag{12}$$

The noise peak estimation for our L model using Equations (7) and (11) are compared with SPICE results and other approaches in the literature or various interconnect configurations (see Table 3).

To compute the interconnect delay on aggressor line we obtained the voltage expression at the node B as

$$v_B(t) = \begin{cases} \frac{v_0}{T_S}\left(k_1 + k_2 t + k_3 e^{s_2 t} + k_4 e^{s_3 t}\right) & t \leq T_S \\ \frac{v_0}{T_S}\left[k_2 T_S + k_3\left(e^{s_2 t} - e^{s_2(t-T_S)}\right) + k_4\left(e^{s_3 t} - e^{s_3(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{13}$$

where $k_1 = \frac{a_1 s_1 s_2 + s_1 + s_2}{s_1 s_2}$, $k_2 = 1$, $k_3 = \frac{(1 + a_1 s_1)}{s_1^2(s_1 - s^2)}$, $k_4 = -\frac{(1 + a_1 s_2)}{s_2^2(s_1 - s^2)}$, $s_{2,3} = \frac{-M_1/M_2 \pm \sqrt{(M_1/M_2)^2 - 4/M_2}}{2}$.

3.2 Victim and Aggressor Switching in Opposite Directions

In deep-submicron processes the interconnect coupling capacitance is a major part of total capacitance; hence, interconnect delay can vary significantly depending on switching behavior. When two neighboring lines are switching in the opposite direction then the effective coupling capacitance can be up to twice the nominal coupling capacitance, depending on the amount of overlap of input waveforms, i.e., $C_c(eff) = SF * C_c$ where the switch factor $SF \in [1.0, 2.0]$.

To estimate the worst possible interconnect delay, one approach used widely in industry is to assume a worst-case switch factor of $SF = 2.0$ and then scale the coupling capacitance by SF, distributing this effective coupling capacitance along with interconnect parallel plate capacitance in the region where the lines overlap. This approach can be too pessimistic, forcing suboptimal design decisions.

Using the circuit model of Figure 2 we now compute the voltage at the output of both victim and aggressor lines, i.e., voltage at nodes C and B. Using the nodal equations at B and C and substituting $V_{S2} = -V_{S1}$ for input voltages, we obtain the following expressions for voltage in the frequency domain (by approximating to first moment only):

$$\frac{V_B}{V_{S1}} = \frac{1+a_1 s}{1+M_1 s+s^2 M_2} \tag{14}$$

$$\frac{V_C}{V_{S1}} = -\frac{1+a_2 s}{1+M_1 s+s^2 M_2} \tag{15}$$

where M_1 and M_2 are same as in Equation (3) and

$$\begin{aligned} a_1 &= (R_{d2}+R_1')(C_1'+C_{c1}) - (R_{d1}+R_1)C_{c1} \\ a_2 &= (R_{d1}+R_1)(C_1+C_{c1}) - (R_{d2}+R_1')C_{c1} \end{aligned} \tag{16}$$

Note that the voltage expressions for nodes B and C are similar, except that they have different coefficients in the numerator.

3.2.1 Step Input Analysis

We now consider step inputs switching opposite directions at the line inputs, i.e., $V_{S1} = -V_{S2} = \frac{V_0}{s}$. Converting the frequency domain voltage expression in Equations (15) and (14) to the time domain, we get the expressions similar to (4). In (17), a_1 is used and in (18), a_2 is used for computing correct values of k_0, k_1, and k_2.

$$v_B(t) = v_0\left(k_0 + k_1 e^{s_1 t} + k_2 e^{s_2 t}\right) \tag{17}$$

$$v_C(t) = -v_0\left(k_0 + k_1 e^{s_1 t} + k_2 e^{s_2 t}\right) \tag{18}$$

3.2.2 Ramp Input Analysis

For ramp inputs switching in opposite directions at the line inputs, we have $V_{S1} = -V_{S2} = \frac{v_0}{s^2 T_S}\left(1-e^{-sT_S}\right)$. The time-domain expressions for voltage at nodes B and C are similar to Equation (13) except for different coefficients.

$$v_B(t) = \begin{cases} \frac{v_0}{M_2 T_S}\left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_3 t}\right) & t \le T_S \\ \frac{v_0}{M_2 T_S}\left[k_1 T_S + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right) + k_3\left(e^{s_3 t} - e^{s_3(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{19}$$

$$v_C(t) = \begin{cases} -\frac{v_0}{M_2 T_S}\left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_3 t}\right) & t \le T_S \\ -\frac{v_0}{M_2 T_S}\left[k_1 T_S + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right) + k_3\left(e^{s_3 t} - e^{s_3(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{20}$$

3.3 Victim and Aggressor Switching in Same Direction

When two neighboring wires are switching in the same direction then the effective coupling capacitance between the lines is $C_c(eff) = SF * C_c$, where the switch factor $SF \in [0,1]$ again depends on the amount of overlap of input waveforms. If both wires switch at exactly the same time with identical slew then the effective coupling capacitance between the lines is zero. This produces a lower bound on the interconnect delay, with corresponding best-case delay estimates computed by not considering any coupling capacitance between the lines (i.e., using only a given line's RC values).

Using the circuit model given in Figure 2 and substituting $V_{S2} = V_{S1}$ for the input voltages, we can compute the voltages on both lines. The analysis for this case is slightly different from the remaining cases. Here, we have to take the second order moment to avoid the degenerate case when the coupling is not playing any role. This would be the case when the both the interconnects have the same electrical parameters (Resistance, Capacitance, etc.), and the characteristics of the two wires are exactly similar. In that case, there is no current flowing due to the coupling capacitance and the correct solution for that case is obtained only by considering the second order moments as well. Thus the expressions for V_B and V_C for this case are given as:

$$\frac{V_B}{V_{S1}} = \frac{1 + a_1 s}{1 + M_1 s + M_2 s^2} \tag{21}$$

$$\frac{V_C}{V_{S1}} = \frac{(1 + a_2 s)}{1 + M_1 s + M_2 s^2} \tag{22}$$

where

$$\begin{aligned} a_1 &= (R_{d2} + R_1')(C_1' + C_{c1}) + (R_{d1} + R_1)C_{c1} \\ a_2 &= (R_{d1} + R_1)(C_1 + C_{c1}) + (R_{d2} + R_1')C_{c1} \end{aligned} \tag{23}$$

and M_1 and M_2 is given by Equation (3).

3.3.1 Step Input Analysis

As discussed above, the time-domain expression for voltage at nodes B and C can be obtained similar to Equation (4) except for different coefficients.

$$v_B(t) = v_0 \left(k_0 + k_1 e^{s_1 t} + k_2 e^{s_2 t} \right) \tag{24}$$

$$v_C(t) = v_0 \left(k_0 + k_1 e^{s_1 t} + k_2 e^{s_2 t} \right) \tag{25}$$

3.3.2 Ramp Input Analysis

Using the partial fractions, the time-domain expressions for voltage at nodes B and C can be obtained similar to Equation (13) (13) except for different coefficients.

$$v_B(t) = \begin{cases} \frac{v_0}{M_2 T_S} \left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_3 t} \right) & t \le T_S \\ \frac{v_0}{M_2 T_S} \left[k_1 T_S + k_2 \left(e^{s_2 t} - e^{s_2 (t - T_S)} \right) + k_3 \left(e^{s_3 t} - e^{s_3 (t - T_S)} \right) \right] & t > T_S \end{cases} \tag{26}$$

$$v_C(t) = \begin{cases} \frac{v_0}{M_2 T_S} \left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_3 t} \right) & t \le T_S \\ \frac{v_0}{M_2 T_S} \left[k_1 T_S + k_2 \left(e^{s_2 t} - e^{s_2 (t - T_S)} \right) + k_3 \left(e^{s_3 t} - e^{s_3 (t - T_S)} \right) \right] & t > T_S \end{cases} \tag{27}$$

When both lines are switching in the same direction the interconnect delay estimates corresponds to the optimistic delay for coupled lines. Hence, we can use our above derived expressions to compute delay uncertainty for various cases of input switching criteria.

4 Noise and Delay Estimation Using the Π model for Interconnect

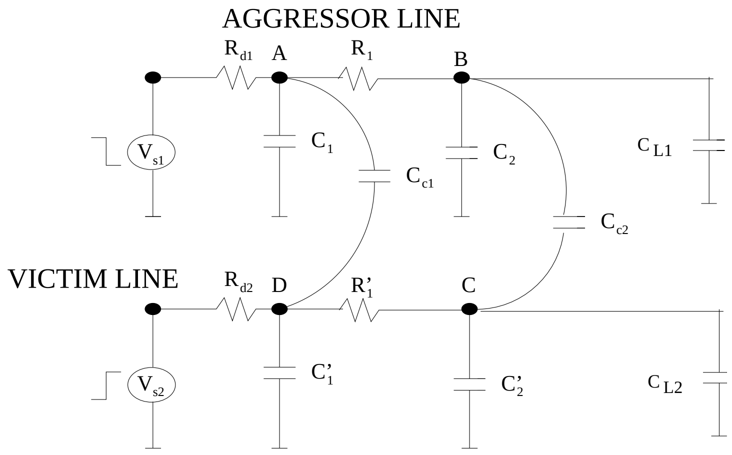


Figure 4: Equivalent circuit (using Π model for interconnect) for the configuration of Figure 1.

In this section, we apply the Π model for the interconnect and compute both the noise peak voltage and delay on the interconnects as shown in Figure 4. Our analyses address both the step and ramp input regimes. In the first subsection, we study the same case as in Section 3.1: one line switching and other line quiet. In the second and third subsections, we study the case when the lines are switching in opposite directions. For these latter cases, we also study the impact of noise on delay of the aggressor line. Our basic analysis approach is as follows:

- We use Figure 4 as the equivalent circuit for analysis purposes. Note that we have distributed the interconnect line capacitance in two parts (ground capacitance and coupled capacitance).
- We will use the same approach for analysis as we did with the L interconnect model, i.e., we transform the time domain circuit equations to frequency domain using Laplace transforms, solve the equations, then convert the results back to the time domain.
- To find the noise voltage at the end of victim line, we must solve for $v_C(t)$, while to find the impact of crosstalk on delay, we must solve for $v_B(t)$. The nodal equations at nodes A, B, C and D in Figure 1 are given in (28).

$$\begin{aligned}
V_{S1} &= V_A + R_{d1}[V_A sC_1 + (V_A - V_D)sC_{C1} + V_B sC_2 + (V_B - V_C)sC_{C2}] \\
V_A &= V_B + R_1[V_B sC_2 + (V_B - V_C)sC_{C2}] \\
V_{S2} &= V_D + R_{d2}[V_D sC_1' + (V_D - V_A)sC_{C1} + V_C sC_2' + (V_C - V_B)sC_{C2}] \\
V_D &= V_C + R_1'[V_C sC_2' + (V_C - V_B)sC_{C2}]
\end{aligned} \tag{28}$$

4.1 Victim Quiet and Aggressor Switching

For this case, the victim line is quiet at low voltage, while the aggressor line is switching from low to high. Therefore, $V_{S2} = 0$. Solving the equations (28) with $V_{S2} = 0$ yields the following transfer function in frequency domain for noise at node C and at node B (we approximate the solution to second moment only).

$$\frac{V_C}{V_{S1}} = \frac{a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2} \tag{29}$$

$$\frac{V_B}{V_{S1}} = \frac{1 + c_1 s + c_2 s^2}{1 + b_1 s + b_2 s^2} \tag{30}$$

where

$$\begin{aligned}
a_1 &= R'_1 C_{C2} + R_{d2} C_{C1} + R_{d2} C_{C2} \\
a_2 &= R_{d2} C'_1 R'_1 C_{C2} + R_{d2} C_{C1} R'_1 C_{C2} + R_{d2} C_{C1} R_1 C_2 + R_{d2} C_{C1} R_1 C_{C2} \\
b_1 &= R'_1 C_{C2} + R_{d2} C_{C2} + R_{d2} C_{C1} + R'_1 C'_2 + R_{d1} C_{C1} + R_{d1} C_{C2} + R_1 C_{C2} + R_{d2} C'_1 + \\
&\quad R_{d1} C_1 + R_{d2} C'_2 + R_1 C_2 + R_{d1} C_2 \\
b_2 &= R_{d2} C'_1 R'_1 C_{C2} + R_{d2} C_{C1} R'_1 C_{C2} + R_{d2} C_{C1} R_1 C_{C2} + R_{d2} C_{C1} R_1 C_2 + R_{d1} C_2 R'_1 C_{C2} + \\
&\quad R_{d1} C_2 R_{d2} C'_1 + R_{d1} C_2 R_{d2} C_{C1} + R_{d1} C_2 R_{d2} C'_2 + R_{d1} C_2 R_{d2} C_{C2} + R_{d1} C_1 R'_1 C'_2 + \\
&\quad R_{d1} C_1 R'_1 C_{C2} + R_{d1} C_1 R_{d2} C'_1 + R_{d1} C_1 R_{d2} C_{C1} + R_{d1} C_1 R_{d2} C'_2 + R_{d1} C_1 R_{d2} C_{C2} + \\
&\quad R_{d2} C'_1 R'_1 C'_2 + R_1 C_2 R'_1 C'_2 + R_1 C_2 R'_1 C_{C2} + R_1 C_2 R_{d2} C'_1 + R_{d2} C_{C1} R'_1 C'_2 + \\
&\quad R_{d1} C_1 R_1 C_2 + R_{d1} C_1 R_1 C_{C2} + R_{d1} C_{C1} R_1 C_2 + R_{d1} C_{C1} R_1 C_{C2} + R_{d1} C_{C1} R'_1 C'_2 + \\
&\quad R_{d1} C_{C1} R'_1 C_{C2} + R_{d1} C_{C2} R'_1 C'_2 + R_{d1} C_{C2} R_{d2} C'_1 + R_{d1} C_{C2} R_{d2} C'_2 + R_{d1} C_{C1} R_{d2} C'_1 + \\
&\quad R_{d1} C_{C1} R_{d2} C'_2 + R_1 C_2 R_{d2} C'_2 + R_1 C_2 R_{d2} C_{C2} + R_1 C_{C2} R'_1 C'_2 + R_1 C_{C2} R_{d2} C'_1 + \\
&\quad R_1 C_{C2} R_{d2} C'_2 + R_{d1} C_2 R'_1 C'_2 \\
c_1 &= R'_1 C_{C2} + R_{d2} C'_1 + R_{d2} C_{C1} + R'_1 C'_2 + R_{d2} C'_2 + R_{d2} C_{C2} \\
c_2 &= R_{d2} C'_1 R'_1 C'_2 + R_{d2} C'_1 R'_1 C_{C2} + R_{d2} C_{C1} R'_1 C'_2 + R_{d2} C_{C1} R'_1 C_{C2} + R_{d2} C_{C1} R_1 C_{C2}
\end{aligned} \tag{31}$$

We now compute the time-domain solutions voltage on both victim and aggressor lines by applying both step and ramp inputs at the input of the aggressor lines.

4.1.1 Step Input Analysis

Consider a step input at the aggressor, i.e., $V_{S1} = \frac{v_0}{s}$ in the transform domain. The voltage at node C of the victim using Equation (29) can be expressed as

$$\begin{aligned}
V_C(s) &= v_0 \frac{a_1 + a_2 s}{1 + b_1 s + b_2 s^2} \\
&= \frac{v_0}{b_2} \left[\frac{k_1}{s - s_1} + \frac{k_2}{s - s_2} \right]
\end{aligned}$$

Using partial fractions and inverse Laplace transforms the above equation can be written in time-domain as

$$v_C(t) = \frac{v_0}{b_2} \left(k_1 e^{s_1 t} + k_2 e^{s_2 t} \right) \tag{32}$$

where $k_1 = \frac{s_2 a_2 b_2 - a_1 b_2 + a_2 b_1}{2 s_2 b_2 + b_1}$, $k_2 = \frac{b_2 (s_2 a_2 + a_1)}{2 s_2 b_2 + b_1}$ $s_1 s_2 = \frac{1}{b_2}$, and $s_1 + s_2 = -\frac{b_1}{b_2}$.

Similarly, using Equation (30) the voltage at node B of the aggressor line can be expressed as

$$\begin{aligned} V_B(s) &= \frac{v_0}{s}\frac{1+c_1 s + c_2 s^2}{1+b_1 s + b_2 s^2} \\ &= \frac{v_0}{b_2}\left[\frac{k_0}{s} + \frac{k_1}{s-s_1} + \frac{k_2}{s-s_2}\right] \end{aligned}$$

Applying partial fractions and inverse Laplace transforms the corresponding time-domain expression is

$$v_B(t) = \frac{v_0}{b_2}\left(k_0 + k_1 e^{s_1 t} + k_2^{s_2 t}\right) \tag{33}$$

where $k_0 = b_2$, $k_1 = \dfrac{-s_2 b_2^2 + s_2 b_2 c_2 + c_2 b_1 - c_1 b_2}{2 s_2 b_2 + b_1}$, $k_2 = \dfrac{b_2\left(-s_2 b_2 - b_1 + s_2 c_2 + c_1\right)}{2 s_2 b_2 + b_1}$, $s_1 s_2 = \frac{1}{b_2}$, and $s_1 + s_2 = -\frac{b_1}{b_2}$. The voltage $v_B(t)$ on the aggressor line can be used to study delay uncertainty due to coupling, i.e., the change in delay due to the coupling effect with the victim line. This type of analysis – to compute delay and delay uncertainty on an aggressor line – is also very useful when the victim line is active (see next subsection).

The voltage $v_C(t)$ represents noise on victim line due to the input switching on the aggressor line. To find the peak noise for this configuration, we differentiate Equation (32) with respect to t and set the derivative to zero. The time at which peak noise is reached is

$$t_{peak} = \left(\frac{1}{s_2 - s_1}\right) \ln\left(-\frac{k_1 s_1}{k_2 s_2}\right) \tag{34}$$

with peak noise given by $v_{c,peak}(t) = v_C(t_{peak})$.

4.1.2 Ramp Input Analysis

For ramp input analysis, we use the frequency domain expression for a ramp input: $V_{S1} = \frac{v_0}{s^2 T_S}\left(1 - e^{-sT_S}\right)$ and $V_{S2} = 0$. The voltage at node C of the victim line in the transform domain can be expressed as

$$\begin{aligned} V_C(s) &= \frac{v_0(1-e^{-sT_S})}{sT_S}\frac{a_1 + a_2 s}{1+b_1 s + b_2 s^2} \\ &= \frac{v_0(1-e^{-sT_S})}{T_S b_2}\left[\frac{k_0}{s} + \frac{k_1}{s-s_1} + \frac{k_2}{s-s_2}\right] \end{aligned}$$

The corresponding time-domain expression is given by

$$v_C(t) = \begin{cases} \dfrac{v_0}{b_2 T_S}\left(k_0 + k_1 e^{s_1 t} + k_2 e^{s_2 t}\right) & t \le T_S \\ \\ \dfrac{v_0}{b_2 T_S}\left[k_1\left(e^{s_1 t} - e^{s_1(t-T_S)}\right) + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{35}$$

where $k_0 = a_1 b_2$, $k_1 = -\dfrac{b_2\left(a_2 + s_2 b_2 a_1\right)}{2 s_2 b_2 + b_1}$, $k_2 = \dfrac{b_2\left(-s_2 b_2 a_1 - a_1 b_1 + a_2\right)}{2 s_2 b_2 + b_1}$, $s_1 s_2 = \frac{1}{b_2}$, and $s_1 + s_2 = -\frac{b_1}{b_2}$, and

Again, using partial fractions and inverse Laplace transforms allows us to convert Equation (30) into a time-domain expression for the ramp input configuration:

$$v_B(t) = \begin{cases} \frac{v_0}{b_2 T_S}\left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_1 t}\right) & t \leq T_S \\ \frac{v_0}{b_2 T_S}\left[k_1 T_S + k_2\left(e^{s_2 t} - e^{s_2 (t-T_S)}\right) + k_3\left(e^{s_1 t} - e^{s_1(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{36}$$

where $k_0 = (-b_1 + c_1)\, b_2,\ k_1 = b_2,\ k_2 = \frac{b_2\left(b_2 s_2 b_1 + b_1^2 - c_1 b_2 s_2 - c_1 b_1 - b_2 + c_2\right)}{2 b_2 s_2 + b_1}$, $k_3 = -\frac{b_2\left(-b_2 + c_2 - b_2 s_2 b_1 + c_1 b_2 s_2\right)}{2 b_2 s_2 + b_1}$, $s_2 s_1 = \frac{1}{b_2}$, and $s_2 + s_1 = -\frac{b_1}{b_2}$.

To find the peak noise, we differentiate Equation (35) and set the result to zero. The expression for peak time is thus

$$\begin{aligned} t_{peak1} &= \left(\frac{1}{s_2 - s_1}\right) \ln\left(-\frac{k_1 s_1}{k_2 s_2}\right) & 0 \leq t_{peak1} \leq T_S \\ t_{peak2} &= \left(\frac{1}{s_2 - s_1}\right) \ln\left\{\left(-\frac{k_1 s_1}{k_2 s_2}\right)\left(\frac{1 - e^{-s_1 T_S}}{1 - e^{-s_2 T_S}}\right)\right\} & t_{peak2} > T_S \end{aligned} \tag{37}$$

from which peak noise voltage can be computed by substituting t_{peak} values into Equation (35), with $v_C(t_{peak}) = \max\{v_C(t_{peak1}), v_C(t_{peak2})\}$.

4.2 Victim and Aggressor Switching in Opposite Directions

When aggressor and victim are switching simultaneously in opposite directions, we have $V_{S2} = -V_{S1}$. Solving the set of Equations (28) with $V_{S2} = -V_{S1}$ yields the following transfer function in the frequency domain (after retaining terms with up to power of two in s):

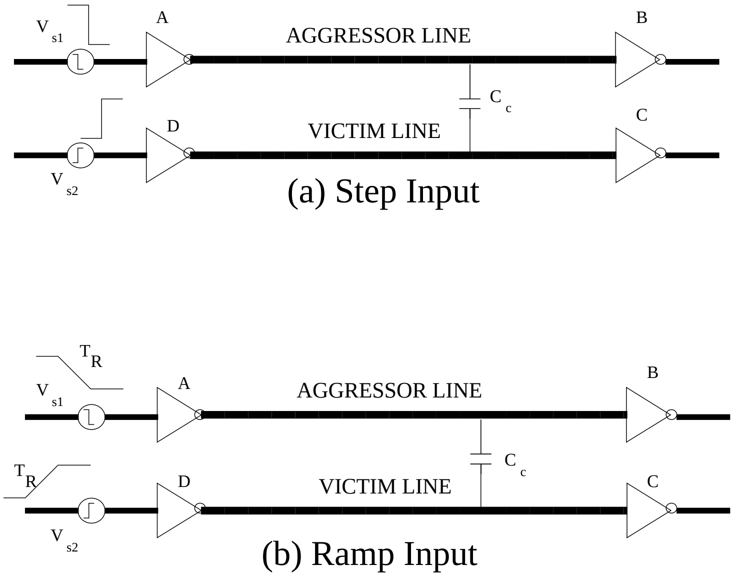


Figure 5: Circuit for the case when the victim is switching in opposite direction to the aggressor: (a) step input, and (b) ramp input.

$$\frac{V_C}{V_{S1}} = \frac{-1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2} \tag{38}$$

$$\frac{V_B}{V_{S1}} = \frac{1 + c_1 s + c_2 s^2}{1 + b_1 s + b_2 s^2} \tag{39}$$

where

$$\begin{aligned}
a_1 &= -(R_1 C_2 + R_1 C_{C2} + R_{d1} C_1 - R_{d2} C_{C2} + R_{d1} C_{C1} + R_{d1} C_2 + R_{d1} C_{C2} - R_1' C_{C2} \\
&\quad - R_{d2} C_{C1}) \\
a_2 &= -(R_{d1} C_1 R_1 C_2 - R_{d2} C_{C1} R_1' C_{C2} - R_{d2} C_{C1} R_1 C_2 - R_{d2} C_{C1} R_1 C_{C2} + R_{d1} C_1 R_1 C_{C2} + \\
&\quad R_{d1} C_{C1} R_1 C_2 + R_{d1} C_{C1} R_1 C_{C2} + R_{d1} C_{C1} R_1' C_{C2} - R_{d2} C_1' R_1' C_{C2}) \\
c_1 &= -(R_1 C_{C2} - R_{d2} C_{C1} + R_{d1} C_{C1} - R_{d2} C_1' - R_{d2} C_2' - R_{d2} C_{C2} - R_1' C_{C2} - R_1' C_2' + \\
&\quad R_{d1} C_{C2}) \\
c_2 &= R_{d2} C_{C1} R_1 C_{C2} - R_{d1} C_{C1} R_1 C_{C2} - R_{d1} C_1 R_1 C_{C2} + R_{d2} C_{C1} R_1' C_2' + R_{d2} C_{C1} R_1' C_{C2} - \\
&\quad R_{d1} C_{C1} R_1' C_{C2} - R_{d1} C_{C1} R_1' C_2' + R_{d2} C_1' R_1' C_2' + R_{d2} C_1' R_1' C_{C2}
\end{aligned} \tag{40}$$

and the denominator terms b_1 and b_2 are the same as in Equation (31).

As before, we these analytical equations for voltage on victim and aggressor lines are useful in computing delay and delay uncertainty with respect to input slew time, coupling capacitance, etc. With the above derivations, we can obtain a complete set of analytical tools to estimate noise peaks and delay uncertainty effects.

4.2.1 Step Input Analysis

With a step input for the aggressor, $V_{S1} = \frac{v_0}{s}$. Using Equation (38), the voltage at node C of the victim can be expressed as

$$\begin{aligned}
V_C(s) &= \frac{v_0}{s} \frac{-1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2} \\
&= \frac{v_0}{b_2} \left[\frac{k_0}{s} + \frac{k_1}{s - s_1} + \frac{k_2}{s - s_2} \right]
\end{aligned}$$

Applying partial fractions and inverse Laplace transforms the corresponding time-domain expression is given by

$$v_C(t) = \frac{v_0}{b_2} \left(k_0 + k_1 e^{s_1 t} + k_2^{s_2 t} \right) \tag{41}$$

where $k_0 = -b_2$, $k_1 = \frac{s_2 b_2^2 + s_2 b_2 a_2 + a_2 b_1 - a_1 b_2}{2 s_2 b_2 + b_1}$, $k_2 = \frac{b_2 (s_2 b_2 + b_1 + s_2 a_2 + a_1)}{2 s_2 b_2 + b_1}$, $s_1 s_2 = \frac{1}{b_2}$, and $s_1 + s_2 = -\frac{b_1}{b_2}$.

Note that the $V_B(s)$ expression in Equation (39) is similar to the Equation (30) for the case when the victim line is quiet; the only difference is that one must substitute correct values of c_1 and c_2 as derived in Equation (40) in the expressions for k_1, k_2, s_1, and s_2 given below the Equation (33). Hence, for the sake of completeness the time-domain expression for voltage on aggressor line is

$$v_B(t) = \frac{v_0}{b_2} \left(k_0 + k_1 e^{s_1 t} + k_2^{s_2 t} \right) \tag{42}$$

4.2.2 Ramp Input Analysis

Now we consider a ramp input at the input of the aggressor line, i.e., $V_{S1} = \frac{v_0}{s^2 T_S}\left(1 - e^{-sT_S}\right)$ [3]. As discussed before using partial fractions and inverse Laplace transforms the time-domain expression for $v_C(t)$ is given by

$$v_C(t) = \begin{cases} \frac{v_0}{b_2 T_S}\left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_1 t}\right) & t \le T_S \\ \frac{v_0}{b_2 T_S}\left[k_1 T_S + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right) + k_3\left(e^{s_1 t} - e^{s_1(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{43}$$

where $k_0 = (b_1 + a_1)\, b_2$, $k_1 = -b_2$, $k_2 = \frac{b_2\left(-b_2 s_2 b_1 - b_1^2 - a_1 b_2 s_2 - a_1 b_1 + b_2 + a_2\right)}{2b_2 s_2 + b_1}$, $k_3 = -\frac{b_2\left(b_2 + a_2 + b_2 s_2 b_1 + a_1 b_2 s_2\right)}{2b_2 s_2 + b_1}$, $s_2 s_1 = \frac{1}{b_2}$, and $s_2 + s_1 = -\frac{b_1}{b_2}$.

As above, since the $V_B(s)$ expression is the same for "victim line is quiet" as it is for "victim line is active", the time-domain expression is the same as in Equation (36), i.e.,

$$v_B(t) = \begin{cases} \frac{v_0}{b_2 T_S}\left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_1 t}\right) & t \le T_S \\ \frac{v_0}{b_2 T_S}\left[k_1 T_S + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right) + k_3\left(e^{s_1 t} - e^{s_1(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{44}$$

where the expressions for k_1, k_2, s_1, and s_2 are identical to those presented in Equation (36), and values of c_1 and c_2 are substituted according to Equation (40).

4.3 Victim and Aggressor Switching in Same Direction

Finally, when the aggressor and victim are switching simultaneously in the same direction we have $V_{S2} = V_{S1}$. Solving the set of Equations (28) with $V_{S2} = V_{S1}$ yields the the following transfer function in the frequency domain (after retaining terms with up to power of two in s):

$$\frac{V_C}{V_{S1}} = \frac{1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2} \tag{45}$$

$$\frac{V_B}{V_{S1}} = \frac{1 + c_1 s + c_2 s^2}{1 + b_1 s + b_2 s^2} \tag{46}$$

where

$$\begin{aligned} a_1 &= R_1C_2 + R_1C_{C2} + R_{d1}C_1 + R_{d2}C_{C2} + R_{d1}C_{C1} + R_{d1}C_2 + R_{d1}C_{C2} + R_1'C_{C2} \\ &\quad + R_{d2}C_{C1} \\ a_2 &= R_{d1}C_1R_1C_{C2} + R_{d1}C_1R_1C_2 + R_{d1}C_{C1}R_1C_2 + R_{d1}C_{C1}R_1C_{C2} + R_{d1}C_{C1}R_1'C_{C2} + \\ &\quad R_{d2}C_1'R_1'C_{C2} + R_{d2}C_{C1}R_1'C_{C2} + R_{d2}C_{C1}R_1C_2 + R_{d2}C_{C1}R_1C_{C2} \\ c_1 &= R_1'C_2' + R_1'C_{C2} + R_{d2}C_1' + R_{d1}C_{C2} + R_{d2}C_{C1} + R_{d2}C_2' + R_{d2}C_{C2} + R_1C_{C2} \\ &\quad + R_{d1}C_{C1} \\ c_2 &= R_{d2}C_1'R_1'C_{C2} + R_{d2}C_1'R_1'C_2' + R_{d2}C_{C1}R_1'C_2' + R_{d2}C_{C1}R_1'C_{C2} + R_{d2}C_{C1}R_1C_{C2} + \\ &\quad R_{d1}C_1R_1C_{C2} + R_{d2}C_{C1}R_1C_{C2} + R_{d1}C_{C1}R_1'C_2' + R_{d1}C_{C1}R_1'C_{C2} \end{aligned} \tag{47}$$

and the denominator terms b_1 and b_2 are the same as in Equation (31).

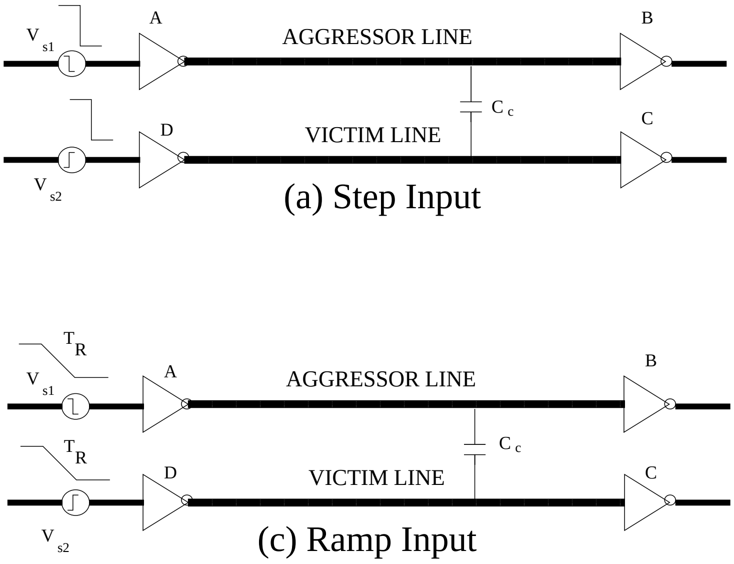


Figure 6: Circuit for the case when the victim is switching in same direction to the aggressor: (a) step input, and (b) ramp input.

4.3.1 Step Input Analysis

Note that the $V_C(s)$ expression in Equation (45) is similar to the Equation (30) for the case when the victim line is quiet; the only difference is that one must substitute a_1 and a_2 from Equation (47) instead of c_1 and c_2 respectively in the expressions for k_1, k_2, s_1, and s_2 given below in the Equation (48). Hence, for the sake of completeness the time-domain expression for voltage on aggressor line is

$$v_C(t) = \frac{v_0}{b_2}\left(k_0 + k_1 e^{s_1 t} + k_2^{s_2 t}\right) \tag{48}$$

Again, note that the $V_B(s)$ expression in Equation (46) is similar to the Equation (30) for the case when the victim line is quiet; the only difference is that one must substitute correct values of c_1 and c_2 as derived in Equation (47) in the expressions for k_1, k_2, s_1, and s_2 given below the Equation (49). Hence, for the sake of completeness the time-domain expression for voltage on aggressor line is

$$v_B(t) = \frac{v_0}{b_2}\left(k_0 + k_1 e^{s_1 t} + k_2^{s_2 t}\right) \tag{49}$$

4.3.2 Ramp Input Analysis

Since the $V_C(s)$ expression is similar to Equation (30), the time-domain expression is again similar to Equation (36), i.e.,

$$v_C(t) = \begin{cases} \frac{v_0}{b_2 T_S}\left(k_0 + k_1 t + k_2 e^{s_2 t} + k_3 e^{s_1 t}\right) & t \leq T_S \\ \\ \frac{v_0}{b_2 T_S}\left[k_1 T_S + k_2\left(e^{s_2 t} - e^{s_2(t-T_S)}\right) + k_3\left(e^{s_1 t} - e^{s_1(t-T_S)}\right)\right] & t > T_S \end{cases} \tag{50}$$

where the expressions for k_1, k_2, s_1, and s_2 are same as those presented in the Equation (36) and one must substitute the values of a_1 and a_2 instead of c_1 and c_2 as given in Equation (47).

5 Experimental Results

To validate our new analyses, we have considered two adjacent M3 interconnects used in a real microprocessor design for 0.25 μm CMOS technology. We assume identical interconnects are driven by identical inverters of size (56,23) μm, and also assume that the loads at the end of the lines are identically sized inverters. We study various configurations of interconnect length, width, and spacing as shown in Table 2. The context for this experimentation is to discover how close our proposed L and Π models compare to SPICE simulations for both noise peak and delay estimation.

We now express the resistance and capacitance circuit parameters in Figure 2 and Figure 4 in terms of the interconnect parameters given in Table 2. For the L interconnect model, we consider $C_1' = C_1 = C_{gnd} + C_L$ and $C_{c1} = C_{coup}$, while for the Π interconnect model, $C_1' = C_1 = C_{gnd}/2$, $C_2' = C_2 = C_{gnd}/2 + C_L$ and $C_{c1} = Cc2 = C_{coup}/2$. The load capacitance due to the inverter gate capacitance is $C_{L1} = C_{L2} = 153\ fF$.

Cases	width (in μm)	spacing (in μm)	length (in μm)	R_{int} (in Ω)	C_{gnd} (in fF)	C_{coup} (in fF)
1	0.49	0.46	1000	122.9	63.2	115.02
2	0.49	0.46	5000	614.32	315.77	575.03
3	1.00	0.46	10000	605.63	983.97	1187.03
4	0.49	1.30	1000	122.9	109.3	46.2

Table 2: Interconnect parameters used in various SPICE simulations (C_L = 153 fF due to inverter gate capacitance for all cases).

We simulate the coupled interconnects by using different input slew times ranging from 0ps to 400ps for the driving inverters. We first compute the noise peaks for all four test cases under different slew times using SPICE simulation and our estimation values for L and Π models as shown in Table 3. In the table, L_{UB} is the upper bound of peak noise when we use the formulas given by Equations (8) and (12) and L_{Our} for peak noise when we use the formulas given by Equations (7) and (11) for the L model of the interconnect for the step and ramp input cases (Section 3.1). For the Π model the noise peak (Π_{Our}) is computed using Equations (34) and (37)) for the step and ramp input cases (Section 4.1). In Table 3, the noise values are normalized to the supply voltage value, i.e., $\frac{\Delta v_C(t)}{V_0}$. Peak normalized noise values in Tables 3 and 4 are also compared with the two existing models of [5] and [8], as well as with SPICE simulation results. The $L_{[8]}$ values are the peak noise values obtained using the formula of [8]. For $\Pi_{[5]}$, we take the noise formula of Kawaguchi and Sakurai [5] for the 2-line case when both the victim and aggressor lines are switching in opposite directions, and divide it by two to obtain the noise peak when only the aggressor is switching.

Our results for the Π interconnect model as shown in Tables 3 and 4 are within 13% of the values derived by SPICE results for peak noise. Also, our new noise estimators are substantially more accurate than previous models of [8] [5]; in terms of design impact, we believe that less over-design and guard-banding will be necessary if our new approximations are adopted. Since in the L model all the interconnect resistance (R_1)is loaded with the total interconnect capacitance (C_1), the noise peak estimated in this model is an upper bound as compared to SPICE result. Similarly, since in the Π the interconnect resistance (R_1)is loaded with the half the interconnect capacitance ($C_1/2$), the noise peak estimated in this model is an lower bound as compared to SPICE result. To make this clear we have plotted the noise peaks in Tables 3 and 4 for all four cases graphically in Figure 7. Hence, our L and Π models can in practice be used as an upper and lower bound estimators for the noise peaks in VLSI interconnects.

Finally, Table 5 shows a comparison of interconnect delays on the aggressor line computed using SPICE and our Π model for the case when the aggressor line is switching and the victim line is quiet. We use the 50% threshold to compute the interconnect delay from the output of the driver to the next inverter input. Similarly, Table 6 gives a comparison of interconnect delays on the aggressor line for the case when both victim and aggressor line are switching in opposite directions. This case yields pessimistic or worst-case interconnect delay values between the two coupled interconnects. From Table 6 we see that our Π model delays are – again, in practice – a lower bound and our L model delays are an upper bound for the SPICE-computed values. Finally, Table 7 gives a comparison of interconnect delay on the aggressor line for the case when victim and aggressor are switching in same direction. This case yields optimistic or best-case interconnect delay values between the two coupled interconnects. From Tables 6 and 7, we can get the delay uncertainty results (Table 8 and Figures 8 and 9). The results shown in above tables indicate that our improved modeling methodology can be used to accurately predict the delay for coupled interconnects.

Cases	$T_S = 0\ ps$					
	SPICE	$L_{[8]}$	[5]	L_{Our}	L_{UB}	Π_{Our}
1	0.080	0.174	0.174	0.130	0.163	0.088
2	0.210	0.275	0.275	0.214	0.274	0.184
3	0.221	0.255	0.255	0.197	0.255	0.183
4	0.037	0.075	0.075	0.055	0.070	0.037

Table 3: Normalized peak noise values under step input ($T_S = 0$) for two coupled interconnect configuration under various models. Our L_{UB} gives upper bound on noise peak values and our Π_{Our} generate values close to SPICE results.

Cases	$T_S = 100\ ps$				$T_S = 200\ ps$				$T_S = 400\ ps$			
	SPICE	L_{Our}	L_{UB}	Π_{Our}	SPICE	L_{Our}	L_{UB}	Π_{Our}	SPICE	L_{Our}	L_{UB}	Π_{Our}
1	0.060	0.103	0.099	0.060	0.035	0.067	0.065	0.035	0.018	0.035	0.035	0.017
2	0.209	0.214	0.265	0.183	0.200	0.213	0.255	0.181	0.198	0.209	0.237	0.173
3	0.210	0.197	0.250	0.183	0.202	0.196	0.247	0.183	0.199	0.196	0.238	0.181
4	0.026	0.043	0.041	0.024	0.012	0.019	0.019	0.010	0.007	0.014	0.014	0.007

Table 4: Normalized peak noise values for different input slew times for the two coupled interconnect configuration under various models.

Cases	$T_S = 0\ ps$ SPICE	Π_{Our}	L_{Our}	$T_S = 100\ ps$ SPICE	Π_{Our}	L_{Our}
1	22	19	25	24	27	35
2	233	215	349	238	216	351
3	487	437	799	491	439	799
4	20	19	25	25	27	33
	$T_S = 200\ ps$			$T_S = 400\ ps$		
1	25	28	39	26	29	41
2	241	221	355	249	239	367
3	495	441	801	500	451	807
4	27	29	37	29	29	37

Table 5: Comparison of aggressor line interconnect delay for 50% threshold delay (in ps) using SPICE and our Π model for the case when the victim line is quiet. Note that interconnect delay is same for both rise and fall switching.

Cases	$T_S = 0\ ps$ SPICE	Π_{Our}	L_{Our}	$T_S = 100\ ps$ SPICE	Π_{Our}	L_{Our}
1	24	25	39	32	33	45
2	405	377	689	408	379	689
3	835	769	1473	839	769	1475
4	22	21	31	30	29	37
	$T_S = 200\ ps$			$T_S = 400\ ps$		
1	35	35	51	38	37	55
2	411	381	691	422	389	697
3	842	771	1475	847	775	1477
4	32	31	43	33	31	43

Table 6: Comparison of aggressor line interconnect delay for 50% threshold delay (in ps) using SPICE and our Π model and L model for the case when the victim line switching opposite to the aggressor. We assume Line1 is switching from 0 to 1 and Line2 is switching from 1 to 0. Note that delay values are same for both Line1 and Line2 as they are identical in this case.

6 Conclusions and Future Work

In conclusion, we have derived improved noise and delay estimates using more accurate circuit modeling techniques. Specifically, we have derived analytical expressions

Cases	$T_S = 0\ ps$ SPICE	Π_{Our}	L_{Our}	$T_S = 100\ ps$ SPICE	Π_{Our}	L_{Our}
1	16	15	19	20	21	25
2	138	133	199	142	135	201
3	293	271	477	296	272	477
4	18	17	23	24	25	29
	$T_S = 200\ ps$			$T_S = 400\ ps$		
1	23	23	26	25	23	27
2	149	141	205	169	163	223
3	300	276	479	314	287	487
4	25	25	33	26	25	33

Table 7: Comparison of aggressor line interconnect delay for 50% threshold delay (in ps) using SPICE and our Π model and L model for the case when the victim line switching in the same direction as the aggressor. We assume both Line1 and Line2 are switching from 0 to 1.

Cases	$T_S = 0\ ps$			$T_S = 100\ ps$		
	SPICE	Π_{Our}	L_{Our}	SPICE	Π_{Our}	L_{Our}
1	8	10	20	12	12	20
2	267	244	490	266	244	488
3	542	498	996	543	497	998
4	4	4	8	6	4	8
	$T_S = 200\ ps$			$T_S = 400\ ps$		
1	12	12	25	13	14	28
2	262	240	486	253	226	474
3	542	495	996	533	488	990
4	7	6	10	7	6	10

Table 8: Delay Uncertainty table for 50% threshold delay (in ps) using SPICE and our Π model and L model.

for noise on a victim interconnect and calculated the impact on delay for the aggressor interconnect, for both the step input and ramp input regimes. The approach extends easily to other modes of simultaneous switching, phase offsets, etc. Our results include easily evaluatable expressions for crosstalk amplitude and delay for coupled RC interconnects. These expressions are demonstrated to be more general and accurate than previous methods in the literature, notably those of [8] and [5], and are for the Π interconnect model within 13% of SPICE simulation results. We plan to extend our validation experiments to a wider range of data from current microprocessor design projects.

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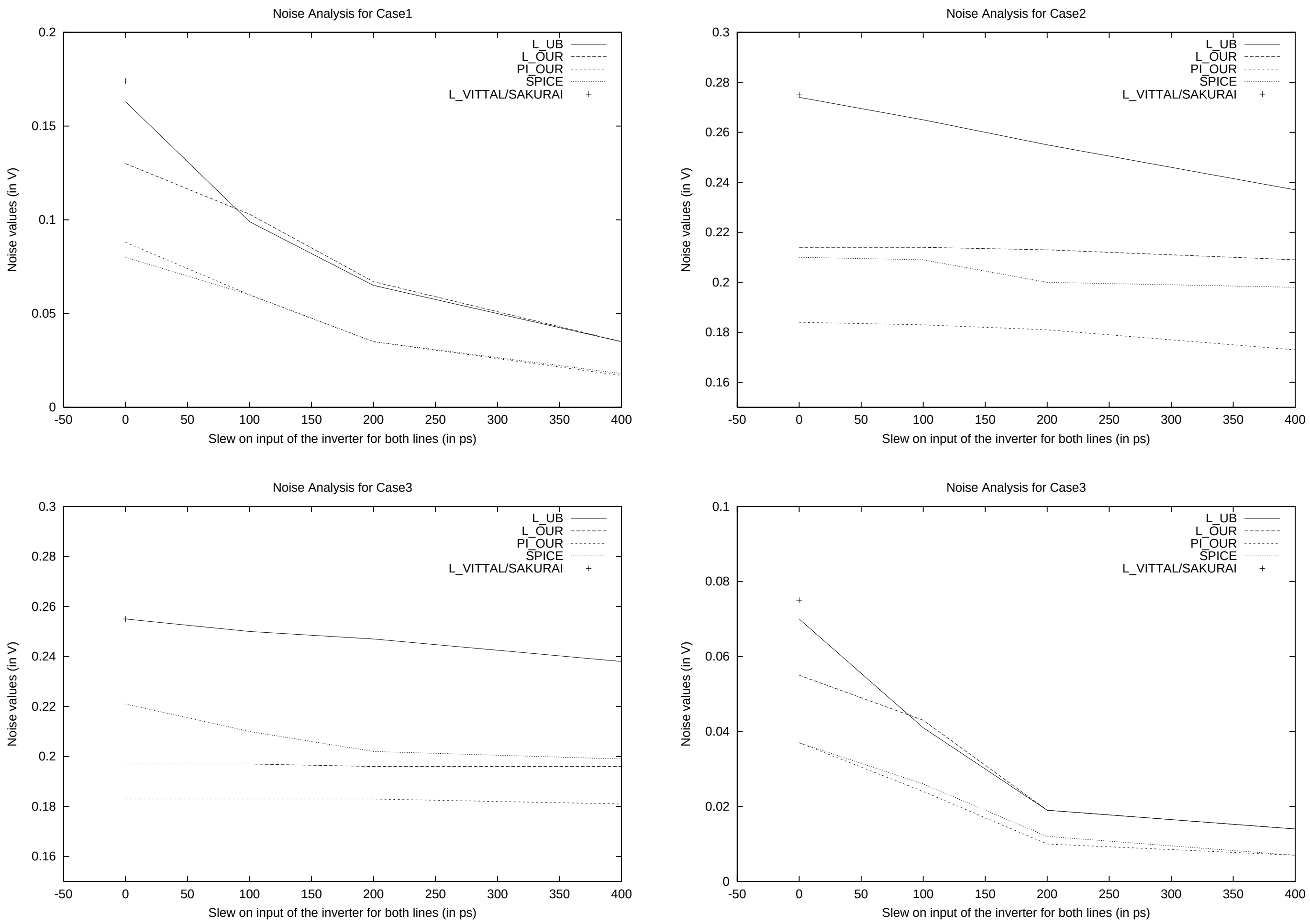

Figure 7: Plot of peak noise values as given in Table 3 and 4 for different input slew times for case1. (Note that we have only one sampling point for other approaches in literature.)

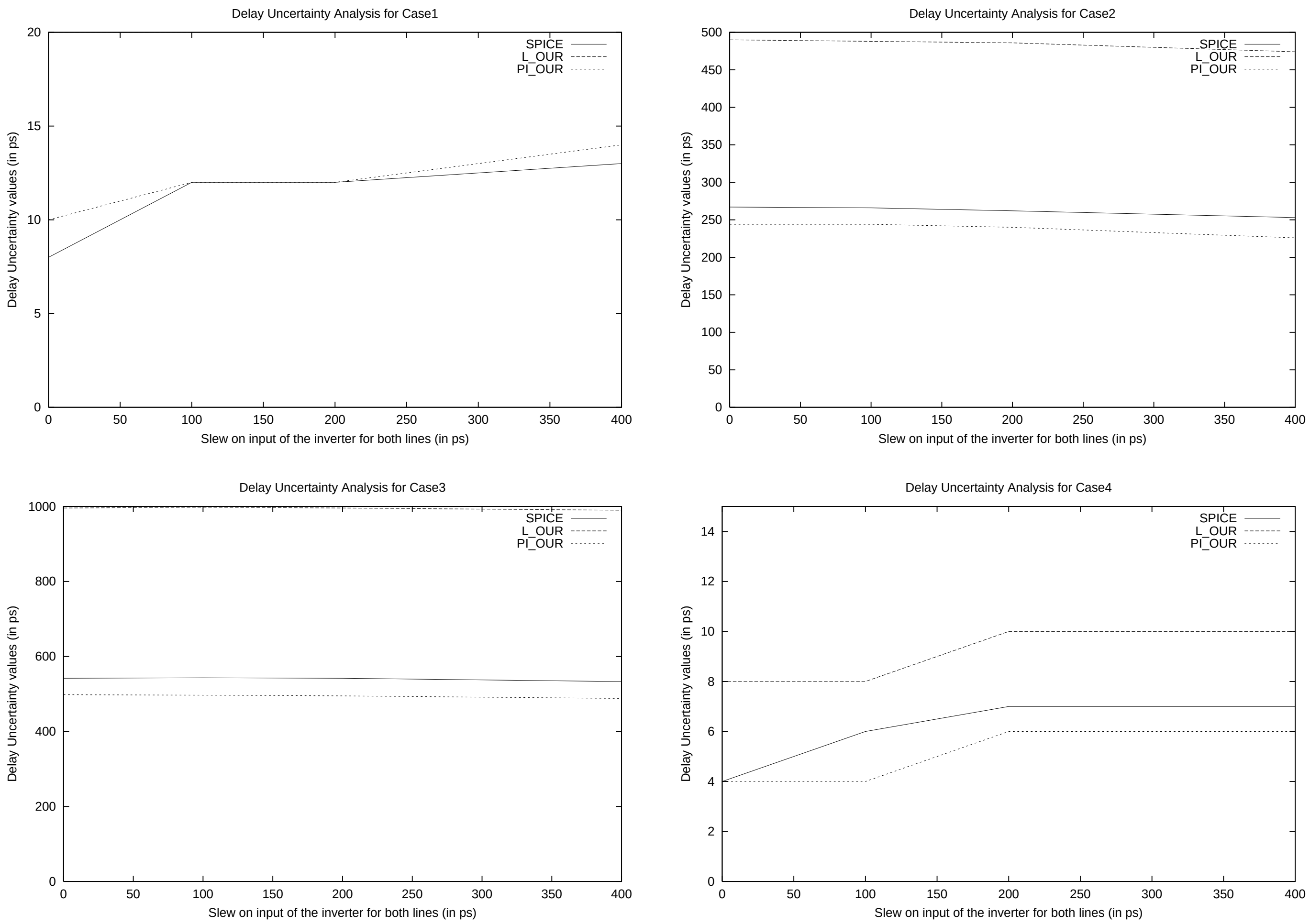

Figure 8: Plot of delay uncertainty values as given in Table 8 for different input slew times for all cases.

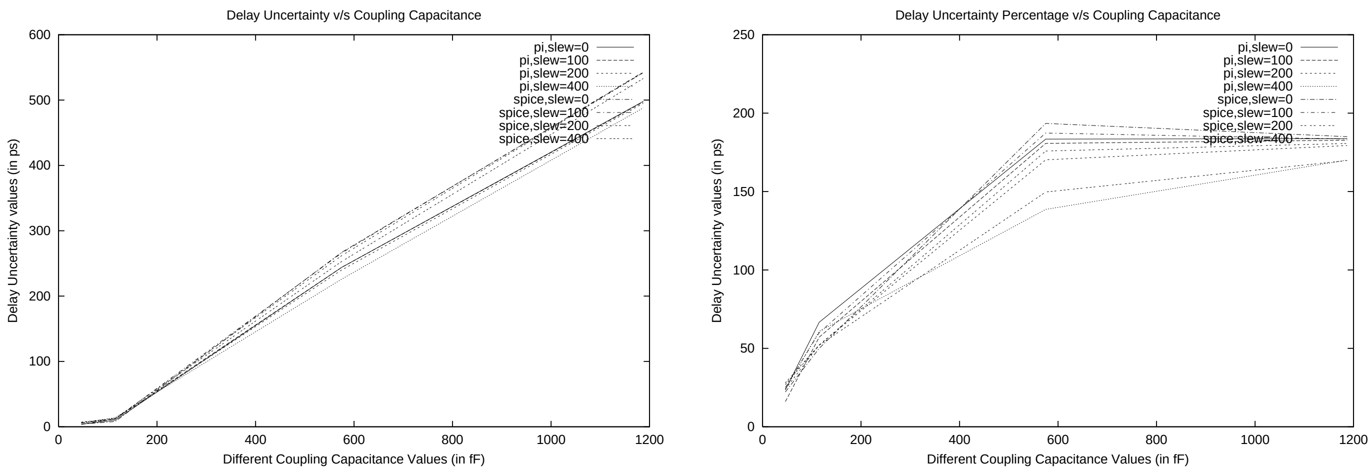

Figure 9: Plot of delay uncertainty values as obtained from Table 8 for different coupling capacitances for Pi-Model and Spice simulations.