age power reduction continue to be among the most critical design concerns. We propose to exploit the recent availability of fine-grain exposure dose control in the step-and-scan tool to achieve both design-time (placement) and manufacturing-time (yield-aware dose mapping) optimizations of timing yield and leakage power. Our placement and dose map co-optimization can improve both timing yield and leakage power of a given design. We formulate the placement-aware dose map optimization as quadratic and quadratic constraint programs which are solved using efficient quadratic program solvers. In this paper, we mainly focus on the placement-aware dose map optimization problem; in the Appendix, we describe a complementary but less impactful dose map-aware placement optimization based on an efficient cell swapping heuristic. Experimental results show noticeable improvements in minimum cycle time without leakage power increase, or in leakage power reduction without degradation of circuit performance.

***Index Terms*—Dose map, leakage power reduction, placement, timing yield.**

I. Introduction

CONTINUED scaling of feature sizes in integrated circuits (ICs) drives improvements of integration complexity and device speed with each successive technology node. In sub-

Manuscript received June 3, 2009, revised November 10, 2009. Date of current version June 18, 2010. A preliminary version of this paper appeared in [1]. Extensions beyond [1] include discussion and experiments on granularities of the partitioned exposure field for dose tuning, new problem formulations for dose map optimization either for improved leakage under timing constraint or for improved circuit performance under leakage constraint, dose map optimization on poly and active layers simultaneously, and improved cell swapping strategy for further timing improvement after dose map optimization. We also test our algorithms using a set of new 65 nm testcases besides the 90 nm testcases used in [1]. This paper was recommended by Associate Editor, J. Hu.

K. Jeong is with the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla, CA 92093 USA (e-mail: kjeong@vlsicad.ucsd.edu).

A. B. Kahng is with the Department of Computer Science and Engineering and the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla, CA 92093 USA (e-mail: abk@ucsd.edu).

C.-H. Park is with the Semiconductor Research and Development Center, Samsung Electronics, Seoul 137-857, Korea (e-mail: chul.h.park@samsung.com).

H. Yao was with the Department of Computer Science and Engineering, University of California at San Diego (UCSD), La Jolla, CA 92093 USA. He is now with the Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China (e-mail: hailongyao@tsinghua.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCAD.2010.2048397

mary sources of design performance variability yield loss. To minimize the impact of manufactu on performance variability, the manufacturing can be improved, and/or designs can be m variations. Improvements to the manufacturing p most prominently, advanced techniques in re ment, mask making, and optical lithographic e of which increase the manufacturing cost and su design cost. As a result, so-called design for ma techniques [2] have received great attention w tronic design and electronic design automation

Critical dimension (CD) variation is a dom the variation of delay and leakage current of t in integrated circuits. With advanced manufactu CD variation is worsening due to a variety variation sources at both within-die and reticle the latter sources include radial bias of spin- thickness, etcher bias, reticle bending, unifor starting materials, and so on [17]. A statistical mization method is proposed in [3], which obt improvement in total leakage reduction by varying the threshold voltage, gate sizes and Gupta *et al.* [4] proposed to apply gate-length only on the devices in non-critical paths for control without negative effects on timing.

A recent technology from ASML, called *Do* [9], allows for minimization of across-chip li tion (ACLV) and across-wafer linewidth varia using an exposure dose (or, simply, dose) corr DoseMapper in the ASML tool parlance exercis of control, *Unicom-XL* and *Dosicom* [6], whi change dose profiles along the lens slit and the of the step-and-scan exposure tool.

Today, the DoseMapper technique is used sol effectively, e.g., [7]) to reduce ACLV or AWL a given integrated circuit during the manufac However, to achieve optimum device performan frequency) or parametric yield (e.g., total chip l not all transistor gate CD values should nece same. For devices on setup timing-critical pa design, a larger than nominal dose on poly la

[1]ACLV is primarily caused by the mask and scanner affected by the track and etcher [10].

0278-0070/$26.00 © 2010 IEEE

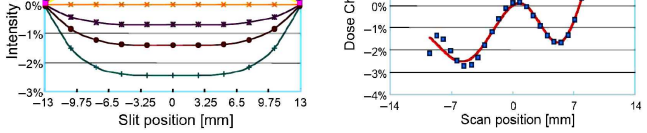

Fig. 1. Unicom-XL and Dosicom, which change dose profiles in slit and scan-directions, respectively. Source: [5].

smaller than nominal gate CD) will be desirable, since this creates a faster-switching transistor. On the other hand, for devices that are on hold timing-critical paths, or in general that are not setup-critical, a smaller than nominal dose on poly layer (causing a larger than nominal gate CD) will be desirable, since this creates a less leaky (although slower-switching) transistor. What has been missing, up to now, is any connection of such "design awareness"—that is, the knowledge of which transistors in the integrated-circuit product are setup or hold timing-critical—with the calculation of the DoseMapper solution.[2] The Zeiss/Pixer Critical Dimension Control (CDC) technology [16] also enables adaptivity in the manufacturing flow to meet the required CD specifications. The CDC technology modifies the local mask transmissivity (which translates into local CD changes on the wafer during the lithography process) without removing the pellicle, thus allowing for tool installations either at the mask manufacturing site, or at the fab line. In this paper, we focus on the DoseMapper technology for tuning of transistor gate dimensions.

We propose a novel method to enhance timing yield as well as reduce leakage power by combined dose map and placement optimizations. The contributions of this paper are as follows.

1) A novel method of enhancing circuit performance and parametric yield based on the dose map technology.
2) A new design-aware and equipment-aware dose map optimization (*DMopt*) method that uses dose to modulate gate CD (for poly layer) and/or gate width (for active layer) across the exposure field, so as to either optimize timing under the constraint of leakage power or reduce leakage power under the constraint of timing.
3) A new dose map-aware placement optimization (*dosePl*) heuristic that considers systematic gate CD changes at different areas within a given dose map, and seeks to

[2]Optimization of gate CDs according to setup or hold timing (non-)criticality has been used by [4]. What we propose below uses a coarser knob (i.e., the dose map) for design-aware gate CD control, but has the advantage of not requiring any change to the mask or OPC flows.

flow, and experimental results are presented
In Section VI, the conclusion is drawn and fu
directions are presented.

II. Preliminaries of Dose Map Optim Problem

A. *DoseMapper Fundamentals*

Fig. 1 shows the intrafield DoseMapper conc
the slit exposure correction is performed by Un
actuator is a variable-profile gray filter inserte
path. The default filter has a second-order (qua
and ASML [11] recommends use of a quadratic
model data in the slit direction. It is also possib
customized profile: lithography systems with Un
the XT:1700i machine) support a slit profile r
polynomials of up to the 6^{th} order in the dose r
a correction range of ±5% can be obtained wit
for the full field size of 26 mm in the X-directi

Scan exposure correction is realized by mean
which changes the dose profile along the scan
dose generally varies only gradually during sca
dose profile can contain higher-order corrections
the exposure settings. The dose set, $D_{\text{set}}(y)$, is
parameters for a dose recipe formed of Legendr
(Legendre functions of the first kind) as

$$D_{\text{set}}(y) = \sum_{n=1}^{8} L_n P_n(y)$$

where y is a floating variable ($|y| \leq 1$) relate
position, L_n are Legendre coefficients, and $P_n(y$
polynomials of variable y. Up to eight Legend
can be supported. The correction range for the
is ±5% (10% full range) from the nominal
laser. When the requested X-slit and Y-scan prof
the lithography system, they are converted to sy
settings (one Unicom-XL shift for all fields, and
and pulse energy profile per field).

Dose sensitivity is the relation between dos
dimension, measured as CD (nm) per percentag
in dose. Increasing dose decreases CD as sho
i.e., the dose sensitivity has negative value. To
dose sensitivity [$\triangle$CD/$\triangle E$, (nm/%)], a focus-ex
(FEM) must be exposed on a product wafer for

Fig. 2. Dose sensitivity: Increasing dose (red color) decreases the CD. Source: [11].

layer using standard production settings [e.g., reticle (6% attPSM), resist, and illumination settings].

B. Dose Map Optimization Problem

The design-aware dose map problem, for the objective of timing yield and leakage power, can be stated as follows. *Given placement P with timing analysis results, determine the dose map to improve timing yield as well as reduce total device leakage.* Specifically, there are two dose map optimization problems with different objectives: one is to minimize total leakage power under a clock period upper bound constraint, and the other is to minimize clock period under a leakage power upper bound constraint. These two dose map optimizations may be formulated using quadratic program (QP) and quadratically constrained program (QCP) (see Section III), and solved using efficient commercial solvers [13].

In the following, for simplicity of exposition we assume that the reticle area taken up by a single copy of the integrated circuit is the same as the area of the exposure field. In practice, the exposure field will contain one or more copies of the integrated circuit(s) being manufactured. It is simple to extend our proposed algorithms to the case where the exposure field contains multiple copies of the integrated circuit(s) being manufactured: smoothness or gradient constraints are scaled, and multiple copies of the dose map solution are tiled horizontally and vertically.

For the dose map optimization problem, we partition the exposure field into a set of rectangular grids $R = |r_{i,j}|_{M\times N}$ on both active and poly layers, where the (uniform) width and height of rectangular grid $r_{i,j}$ are both less than or equal to a user-specified parameter G. G controls the granularity of the dissected rectangular grids: a smaller value of G corresponds to a larger number of rectangular grids, along with a more precisely specified new dose map and better timing yield and/or leakage power improvement. However, G cannot be set too small, due to the DoseMapper equipment limitations. In general, G can be determined so as to balance between DoseMapper equipment constraints and timing yield and/or leakage power improvement, and different values of G may be

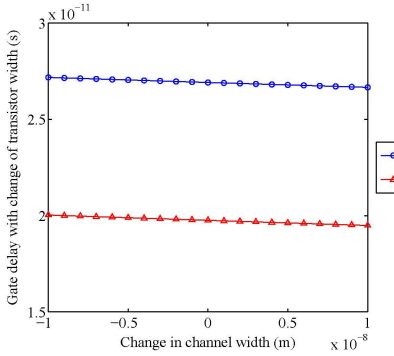

Fig. 4. Delay of an inverter versus change in gate width.

used for different layers. In the discussion belo
that the same G values are used for both active a

Dose map optimization using different gran
partitioned rectangular grids is tested and disc
tion V.

In this paper, we mainly focus on dose ma
on the poly layer, i.e., for modulation of ga
have also tried dose map optimization on both
poly layers to simultaneously modulate gate wi
when optimizing timing and leakage power. F
of exposition, in the following sections we st
delay and leakage power estimation equations,
problem formulations, considering both gate w
length variations.

C. Circuit Delay and Leakage Power Calculat

We assume the dose sensitivity D_s to have th
of -2 nm/% [7] in our experimental evaluation
and gate width change linearly with dose tunir
$D_s \times d^P_{i,j}(p)$ and $\Delta W_p = D_s \times d^A_{i,j}(p)$, where ΔL
in gate length of gate p, ΔW_p is the change in
gate p, and $d^P_{i,j}(p)$ and $d^A_{i,j}(p)$ are percentage
specify the relative changes of dose for poly ar
in the rectangular grid $r_{i,j}$ wherein gate p is lo

Fig. 3 shows SPICE-calculated delay values
are varied in an inverter that is implemented
nology with equal channel lengths of the PMO
devices. Fig. 4 shows SPICE-calculated inverte
as gate widths of the PMOS and NMOS devic

delay decreases linearly as the gate width increases, and increases linearly as the gate length increases. Since gate length (width) changes linearly when the dose on the gate for poly (active) layer varies, there is a linear relationship between the change of gate delay and the change of exposure dose on the gate for both poly and active layers, i.e., $\Delta t_p = t'_p - t_p = A_p \times \Delta L_p + B_p \times \Delta W_p = A_p \times D_s \times d^P_{i,j}(p) + B_p \times D_s \times d^A_{i,j}(p)$. Here, t_p and t'_p are the delay values of gate p before and after the percentage dose changes $d^P_{i,j}(p)$ and $d^A_{i,j}(p)$ on poly and active layers in the rectangular grid $r_{i,j}$ where gate p is located, ΔL_p and ΔW_p are the changes in gate length and gate width of gate p, and A_p and B_p are fitted parameters that are dependent on input slew and load capacitance of each gate. In other words, for each distinct standard cell, and for each combination of input slew and load capacitance, different values of A_p and B_p are obtained from processing of Liberty nonlinear delay model tables. Total runtime of this procedure for the 65 nm production standard-cell library (36 combinational cells and nine sequential cells) is less than 1 min on a single processor using our Liberty processing and curve fitting tool. The fitted parameters can also be used to compute the change in gate delay when only the dose on poly layer changes (i.e., only for gate length modulation), in which case the dose change on active layer [$d^A_{i,j}(p)$] is 0.

For circuit delay calculation, without loss of generality we consider a combinational circuit with n gates as in [12]. Sequential circuits may be addressed similarly, e.g., by "unrolling" them, using standard techniques, into combinational circuits that traverse from primary inputs and sequential cell outputs, to sequential cell inputs and primary outputs. For a given combinational circuit, we add to the corresponding circuit graph one fictitious source node, which connects to all primary inputs, and one fictitious sink node, which connects from all primary outputs. Nodes are indexed by a reverse topological ordering of the circuit graph, with the source and sink nodes indexed as $n + 1$ and 0, respectively.

Fig. 5 shows SPICE-calculated average transistor leakage values with simulation condition (VDD = +1.0-V, temperature = +25 °C, process = TT) as gate lengths are varied in a minimum-size inverter that is implemented in 65 nm technol-

[3]We recognize that off-path loading, slew propagation, and crosstalk timing windows can all change, and will be eventually accounted for precisely by golden signoff analysis. However, we assume in our optimization framework—as is fairly standard in the sizing literature—that these effects are negligible, and we validate our results with golden signoff analysis.

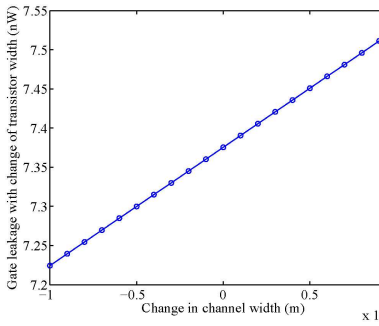

Fig. 6. Average leakage of a 1X inverter (INVX1) versus t
width (VDD = +1.0-V, temperature = +25 °C, process = TT

ogy, where channel lengths of the PMOS and N
are equal. Fig. 6 shows SPICE-calculated aver
leakage values with the same inverter and sim
tion, as all channel widths of the PMOS and N
are changed by the same delta value. From Fig
gate leakage varies exponentially with gate leng
with the change in gate width around the no
size (i.e., 65 nm) and the original transistor wi
performed background experiments on Liberty l
of 36 different standard cell masters, and co
exponential (linear) relationships between gat
gate length (width). Similar analyses for the 90 n
node can be found in [1]. In our optimizatio
that the change of leakage power of a gate
function of the change in gate length[4] and a l
of the change in gate width, i.e., $\Delta Leakage(\cdot$
$\alpha_p \times (\Delta L_p)^2 + \beta_p \times \Delta L_p + \gamma_p \times \Delta W_p$ for gate p. T
of the change in total leakage power of the gate
is given by (2). Note that the parameters α_p, β
gate-specific, i.e., different values of the param
for different types of gates. Similar to the comp
delay, the fitted parameters can also be used to
change in leakage power when only the dose
changes, in which case there is no dose change

[4]We recognize that leakage power is exponential in gat
a quadratic approximation to facilitate the problem formula
method.

wire layout patterns, and thus will not affect golden wire parasitics. In our implementation, wire delay is obtained from golden static timing analysis reports and added in between gates. Assume that the original dose in the chip area is uniform. The goal of the design-aware dose map optimization (*DMopt*) is to tune the dose maps on poly and active layers simultaneously to adjust the channel lengths and widths of the gates and thereby optimize circuit delay and/or total leakage power, subject to upper and lower bounds on delta dose values per grid, and a dose map smoothness bound to reflect the fact that exposure dose must change gradually between adjacent grids. In the following problem formulations, we use delta leakage instead of total leakage power to facilitate the computation. By minimizing/constraining delta leakage, i.e., the change in total leakage power, the total leakage power will be minimized/constrained. For computing delta leakage power, three fitted parameters (i.e., α_p, β_p, and γ_p) are needed as in (2). However, for computing the total leakage power, four fitted parameters are needed (i.e., a constant item is needed besides coefficients α_p, β_p, and γ_p) because we assume a quadratic relation between the change in leakage power and the change in doses on active and poly layers. Since delta leakage is enough for the following problem formulations, we use delta leakage rather than total leakage power to avoid the constant item in the estimation.

A. Design-Aware Dose Map Optimization on Poly Layer

The design-aware dose map optimization for poly layer can be formulated into two different problems, i.e., the quadratic program and the quadratic constraint program based on different types of constraints (i.e., either linear or quadratic).

1) *Dose Map Optimization for Improved Leakage Under Timing Constraint:* The optimization problem on poly layer is formulated as a quadratic program as follows.

- *Objective:* Minimize $\Delta Leakage$.
- *Subject to:*

$$L \leq d^P_{i,j} \leq U \quad \forall\, i \in [1, M] \quad j \in [1, N] \tag{3}$$

$$\begin{cases} |d^P_{i,j} - d^P_{i+1,j+1}| \leq \delta \;\forall\, i \in [1, M-1] \quad j \in [1, N-1] \\ |d^P_{i,j} - d^P_{i,j+1}| \leq \delta \quad \forall\, i \in [1, M] \quad j \in [1, N-1] \\ |d^P_{i,j} - d^P_{i+1,j}| \leq \delta \quad \forall\, i \in [1, M-1] \quad j \in [1, N] \end{cases} \tag{4}$$

specifies smoothness constraints on the dose for
i.e., that the doses in neighboring rectangula
differ by a bounded amount.[5] Equation (5) spe
constraint when the delays of the gates are
the dose adjustment process. In (5), a_p repres
time at node p, which is the maximum dela
node $n+1$ to node p; $d^P_{i,j}(p)$ is the change in
dose in rectangular grid $r_{i,j}$ on the poly layer
p is located. The parameter A_p is gate-specific
values of the parameters are used for different
as well as for gates of the same type that
input slews and load capacitances. Equation (
user-specified upper bound (i.e., τ_L) on the
longest path in the circuit. The calculation
in total leakage power of the gates $\Delta Leakage$
is given by (2), where only poly layer related
$\alpha_p \times D_s^2 \times d^P_{i,j}(p)^2 + \beta_p \times D_s \times d^P_{i,j}(p)]$ is comp
constraints are linear and the objective is quadr
an instance of quadratic program.

2) *Dose Map Optimization for Improve
der Leakage Constraint:* The optimization pr
layer is formulated as a quadratically constrain
follows.

- *Objective:* Minimize T.
- *Subject to:* Equations (3), (4), (5), and

$$\Delta Leakage \leq \xi_L.$$

Equations (3), (4), and (5) are as discussed
problem formulation. Equation (7) specifies th
the change in the total leakage power of all
where ξ_L is a user-specified parameter for the c
the constraint in (7) is quadratic and the objectiv
yields an instance of quadratically constrained

B. Design-Aware Dose Map Optimization on
Active Layers

1) *Dose Map Optimization for Improved L
Timing Constraint:* The optimization problem
and active layers is formulated as a quadrat
follows.

- *Objective:* Minimize $\Delta Leakage$.

[5]As stated in Section II-A, the dose generally varies gr
the gradual property of dose profiles, the smoothness cons

$$\begin{cases} 0 \le a_{n+1} \\ t'_p = t_p + A_p \times D_s \times d^P_{i,j}(p) \\ \qquad + B_p \times D_s \times d^A_{i,j}(p) \qquad (p = 1, \cdots, n) \end{cases} \tag{10}$$

$$T \le \tau_{WL}. \tag{11}$$

Similar to (4) for the poly layer, (8) specify the correction ranges on the dose for the active layer. Equation (9) specifies smoothness constraints on the dose for the active layer, and (10) specifies the delay constraint when the delays of the gates are scaled during the dose adjustment process on both poly and active layers. a_p and $d^P_{i,j}(p)$ are defined as in (5), and $d^A_{i,j}(p)$ is the change in percentage of dose in grid $r_{i,j}$ on the active layer wherein gate p is located. The parameter B_p is gate-specific, similar to A_p used in (5). Equation (11) specifies the constraint on the delay of the longest path in the circuit, where τ_{WL} is a user-specified parameter for the constraint. The calculation of the change in total leakage power of the gates $\Delta Leakage$ in the circuit is given by (2) which considers the impact of both gate length and gate width variations on leakage power.

2) *Dose Map Optimization for Improved Timing Under Leakage Constraint:* The optimization problem on both poly and active layers is formulated as a quadratically constrained program as follows.

- *Objective:* Minimize T.
- *Subject to:* Equations (3), (4), (8), (9), (10), and

$$\Delta Leakage \le \xi_{WL}. \tag{12}$$

Equations (3), (4), (8), (9), and (10) are as discussed in previous problem formulations. Equation (12) specifies the constraint on the change in the total leakage power of all cell instances, where ξ_{WL} is a user-specified parameter for the constraint. Again, since the constraint in (12) is quadratic and the objective is linear, we have an instance of quadratically constrained program.

The above problem formulations[6] are either quadratic program or quadratically constrained program, which can be solved using classic quadratic programming methods. In particular, we use CPLEX [13] in the experimental platform described below.

[6]The optimization result is feasible for the equipment, as a consequence of the constraints (3), (4), (8), and (9).

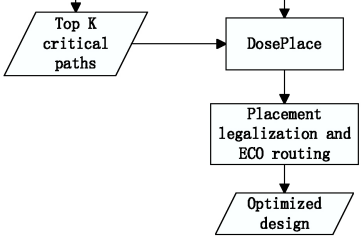

Fig. 7. Flow of the timing and leakage power optimizatio *DMopt* and *dosePl* (in the Appendix).

IV. Timing and Leakage Power Optimiz

A. Overall Optimization Flow

Fig. 7 shows our whole flow integrating *D* with *dosePl* (discussed in the Appendix) for tim age optimization. Note that the timing and leak tion flow is carried out after V_{th} and V_{dd} assignm For the timing and leakage related dose map problem, the input consists of: (1) the original d those calculated to minimize ACLV and AWLV on in-line metrology) for both poly and active characterized standard-cell timing libraries (or models that comprehend the impact of dose on lengths and widths) for different gate lengths an and (3) the circuit with placement and routing in "placement and routing information," we also in information that is necessary for timing and po e.g., extracted wiring parasitics. With the nomin cell timing and power libraries, and the circu its placement, routing and parasitic data, timing be performed to generate the input slews an capacitances of all the cell instances. With the in output load capacitances of all the cell instance dose maps, and characterized cell libraries of lengths and gate widths, the dose map optimizati to determine doses that adjust gate lengths an of the cells for timing and leakage optimizati dose map constraints. Finally, the optimized desi maps on both layers are generated.

According to the optimized design-aware c both poly and active layers, the cell instance grids of the dose maps will have different gat widths as well as different cell masters in the

Fig. 8. Detailed view of design-aware dose map optimization flow.

cell libraries.[7] Thus, the design's netlist representation must be updated according to the dose maps. Using the characterized cell libraries, timing analysis is performed on the new design with the updated cell masters to identify the top-K (e.g., $K = 10,000$) critical paths for the complementary *dosePl* (see the Appendix) process to optimize. The *dosePl* process is based on a cell swapping strategy, which may introduce an illegal placement result. Therefore, a legalization process is invoked to legalize the swapped cells. ECO routing is then executed for the affected wires to refine the design with optimized timing yield.

B. Summary of the Dose Map Optimization Flow

The dose map optimization in Fig. 8 is summarized as follows. The input consists of the original dose maps on both layers, the characterized cell libraries of different gate lengths and widths, and the input slews and output capacitances of all the cells in the circuit. From the characterized 65 nm cell libraries of different gate lengths and widths and 90 nm cell libraries of different gate lengths,[8] the coefficients in the linear function of delay and quadratic function of leakage power are calibrated. Note that when gate delay calculation in the cell libraries adopts a lookup table method, where the entries are indexed by input slews and output capacitances, the coefficients of the delay functions may be calibrated for each entry in each delay table. Then, according to the input slew and output capacitance values that were obtained for each cell in the previous step, the coefficients associated with the nearest entry (or, entries with interpolation) in the table will be applied to calculate the delay of the cell.

The exposure fields on both poly and active layers are then partitioned into rectangular grids. For each grid on poly (active) layer, a variable $d^P_{i,j}$ ($d^A_{i,j}$) represents the amount of dose change in the grid. Maximum circuit delay is captured using variable a_p that represents the arrival time at the output

[7]When the gate lengths and widths are computed from the optimized dose maps, it is possible that the computed values do not exactly match the available drive strengths of the cell masters in the characterized cell libraries. Thus, a rounding step is needed to snap the computed gate lengths and widths to the cell masters with nearest drive strengths.

[8]We focus on the dose map optimization methods for 65 nm testcases. However, 90 nm testcases are also used in dose map optimization for gate length modulation to provide extra supporting experimental data.

delay constraints, as well as the objective of m
total leakage power of all the cells under tim
(resp. minimizing the timing of the circuit
constraint). Finally, a quadratic program (resp
constrained program) solver finds the optimal c
each grid based on the original dose maps; t
optimal design-aware dose maps.

V. Experimental Results

To assess the effectiveness of the propos
optimization algorithms, we first sweep the d
poly layer from −5% to +5% for all the
in the 65 nm design AES-65 and the 90 nm
90 (shown in Table I) and perform timing
Synopsys PrimeTime (version Z-2006.12) [14
power estimation using *Cadence SoC Encounter*
The timing analysis and leakage power estima
on pre-characterized 65 nm and 90 nm cell libr
length and gate width variants. Delay and l
results are given in Tables II and III, where "M
minimum cycle time and "Leakage" refers to th
power of all the cells. From the tables, in the
the dose changes on poly layer correspond to
timing yield improvement or leakage power
$d^P_{i,j} = +5$ and $d^P_{i,j} = -5$). The results show tha
improvement can be obtained at the cost of
increase, whereas leakage power reduction can
the cost of timing yield degradation. Uniform c
all the cell instances cannot obtain timing yield
without leakage power increase. However, our
map optimization algorithms can obtain sub
yield improvement without increase in total lea
well as leakage power reduction without degrad
yield.

The timing and leakage optimization flow i
in C++ and tested on industrial testcases as give
Table I, there are two different classes of test
and JPEG-65 are 65 nm designs, and AES-90
are 90 nm designs. In the experiments, the d
D_s is −2 nm/%. The parameters A_p, B_p, α
are calibrated using PrimeTime and SoC En
on the pre-characterized cell timing and lea
Since different libraries (i.e., 90 nm and 65 nm
different designs, two sets of parameters are c

TABLE III

DELAY AND LEAKAGE VALUES OF 90 NM DESIGN AES-90 WHEN DOSE CHANGE $d^P_{i,j}$ IS SWEPT FROM 0% TO −5% AND FROM 0%
POLY LAYER

Dose change	$d^P_{i,j}=0$	$d^P_{i,j}=-0.5$	$d^P_{i,j}=-1$	$d^P_{i,j}=-1.5$	$d^P_{i,j}=-2$	$d^P_{i,j}=-2.5$	$d^P_{i,j}=-3$	$d^P_{i,j}=-3.5$	$d^P_{i,j}=-4$	$d^P_{i,j}=-4$
MCT (ns)	1.990	2.011	2.031	2.057	2.078	2.093	2.115	2.135	2.155	2.172
imp. (%)	–	−1.031	−2.076	−3.359	−4.401	−5.155	−6.296	−7.257	−8.283	−9.142
$P_{leakage}$ (μW)	2430.214	2324.525	2225.130	2135.234	2054.458	1980.457	1914.474	1850.809	1796.545	1746.50
imp. (%)	–	4.349	8.439	12.138	15.462	18.507	21.222	23.842	26.075	28.134
Dose change	$d^P_{i,j}=0$	$d^P_{i,j}=+0.5$	$d^P_{i,j}=+1$	$d^P_{i,j}=+1.5$	$d^P_{i,j}=+2$	$d^P_{i,j}=+2.5$	$d^P_{i,j}=+3$	$d^P_{i,j}=+3.5$	$d^P_{i,j}=+4$	$d^P_{i,j}=+4$
MCT (ns)	1.990	1.971	1.950	1.932	1.905	1.893	1.868	1.845	1.818	1.791
imp. (%)	–	0.964	2.029	2.915	4.257	4.906	6.161	7.302	8.652	10.012
$P_{leakage}$ (μW)	2430.214	2546.756	2678.096	2824.598	2994.978	3180.969	3404.057	3654.222	3939.749	4253.778
imp. (%)	–	−4.796	−10.200	−16.228	−23.239	−30.893	−40.072	−50.366	−62.115	−75.037

Straightforward way of increasing dose cannot obtain delay improvement without incurring leakage increase.

TABLE IV

RESULTS OF DOSE MAP OPTIMIZATION ON POLY LAYER, I.E., GATE LENGTH (L_{gate}) MODULATION WITH SMOOTHNESS BOUND δ =
CORRECTION RANGE ±5%

AES-65	Nom	$5\times5\,\mu m^2$ grids				$10\times10\,\mu m^2$ grids				$30\times30\,\mu m^2$ gri		
	L_{gate}	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QC*
MCT (ns)	1.638	1.631	0.44	1.607	1.89	1.632	0.35	1.626	0.71	1.637	0.07	1.63
Leakage (μW)	448.0	409.7	8.54	441.3	1.49	434.3	3.05	445.4	0.57	447.9	0.01	447.
Runtime (s)	–	72	–	108	–	18	–	335	–	9	–	46
JPEG-65	Nom	$5\times5\,\mu m^2$ grids				$10\times10\,\mu m^2$ grids				$30\times30\,\mu m^2$ gri		
	L_{gate}	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QC*
MCT (ns)	2.179	2.174	0.25	2.081	4.52	2.178	0.04	2.102	3.54	2.172	0.31	2.15
Leakage (μW)	2915.5	2312.7	20.67	2922.3	−0.23	2480.9	14.91	2913.4	0.07	2843.1	2.48	2909
Runtime (s)	–	490	–	891	–	292	–	558	–	61	–	929
AES-90	Nom	$5\times5\,\mu m^2$ grids				$10\times10\,\mu m^2$ grids				$50\times50\,\mu m^2$ gri		
	L_{gate}	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QC*
MCT (ns)	1.990	1.975	0.75	1.861	6.47	1.981	0.44	1.872	5.91	1.989	0.05	1.92
Leakage (μW)	2430.2	1823.2	24.98	2386.1	1.82	1901.6	21.75	2370.2	2.47	2172.4	10.61	2406
Runtime (s)	–	176	–	227	–	85	–	145	–	16	–	92
JPEG-90	Nom	$5\times5\,\mu m^2$ grids				$10\times10\,\mu m^2$ grids				$50\times50\,\mu m^2$ gri		
	L_{gate}	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QCP*	imp. (%)	*QP*	imp. (%)	*QC*
MCT (ns)	2.906	2.894	0.41	2.667	8.23	2.901	0.16	2.689	7.45	2.887	0.65	2.75
Leakage (μW)	4354.2	3422.5	21.40	4244.4	2.52	3453.6	20.68	4273.5	1.85	3822.2	12.22	4308
Runtime (s)	–	2157	–	3644	–	1194	–	2068	–	243	–	254

TABLE V

RESULTS OF DOSE MAP OPTIMIZATION ON BOTH POLY AND ACTIVE LAYERS USING QUADRATICALLY CONSTRAINED PROGRAM F
TIMING, I.E., GATE LENGTH (L_{gate}) AND GATE WIDTH (W_{gate}) MODULATION, WITH SMOOTHNESS BOUND δ = 2 AND DOSE CORRECTI

AES-65	Nom	$5\times5\,\mu m^2$ grids				$10\times10\,\mu m^2$ grids				$30\times30\,\mu m^2$		
	$L_{gate}\&W_{gate}$	L_{gate}	imp. (%)	Both	imp. (%)	L_{gate}	imp. (%)	Both	imp. (%)	L_{gate}	imp. (%)	B
MCT (ns)	1.638	1.601	1.89	1.586	3.17	1.626	0.10	1.610	1.71	1.647	0.07	1.
Leakage (μW)	448.0	441.3	1.49	447.0	0.22	445.4	0.57	447.7	0.06	447.9	0.01	4
Runtime (s)	–	108	–	179	–	335	–	548	–	46	–	
JPEG-65	Nom	$5\times5\,\mu m^2$ grids				$10\times10\,\mu m^2$ grids				$30\times30\,\mu m^2$		
	$L_{gate}\&W_{gate}$	L_{gate}	imp. (%)	Both	imp. (%)	L_{gate}	imp. (%)	Both	imp. (%)	L_{gate}	imp. (%)	B
MCT (ns)	2.179	2.081	4.52	2.090	4.10	2.102	3.54	2.093	3.93	2.159	0.91	2.
Leakage (μW)	2915.5	2922.3	−0.23	2922.0	−0.22	2913.4	0.07	2915.5	0.00	2909.8	0.19	29
Runtime (s)	–	891	–	1561	–	558	–	747	–	929	–	3

the different libraries and used in the dose map optimization for the corresponding testcases. Table IV shows the dose map optimization results on poly layer. In Table IV, QP refers to the quadratic program for improved total leakage under timing constraint, and QCP refers to the quadratically constrained program for improved timing under leakage constraint. Different sizes of rectangular grids are used in the dose map optimization, i.e., $5 \times 5\,\mu m^2$, $10 \times 10\,\mu m^2$, and either $30 \times 30\,\mu m^2$ (for 65 nm cases) or $50 \times 50\,\mu m^2$ (for 90 nm cases). The dose smoothness bound is $\delta = 2$,[9] and the dose correction range is $\pm 5\%$. From the results, the finer the rectangular grids, the greater the improvement in the timing of the circuit or in the total leakage power. We observe different optimization quality between 90 nm testcases (AES-90 and JPEG-90) and 65 nm testcases (AES-65 and JPEG-65). Average leakage reduction for 90 nm testcases under timing constraints for $5 \times 5\,\mu m^2$ grids is 23.2% but that of 65 nm testcases shows 14.6%. Average MCT reduction for 90 nm testcases under leakage constraints for $5 \times 5\,\mu m^2$ grids is more than 7.4%, but that of 65 nm testcases shows 3.4%. There are two reasons for the above optimization discrepancy between 90 nm and 65 nm designs. The first reason is that $5 \times 5\,\mu m^2$ grids have different granularities for the different designs. From Table I, the average number of cell instances in a grid of $5 \times 5\,\mu m^2$ is 2.2 for the 90 nm testcases and 6.3 for the 65 nm testcases. As discussed above, the finer the rectangular grids, i.e., the fewer cell instances in one grid, the better the optimization quality. The smaller average number of cell instances per grid for the 90 nm testcases permits larger improvements. The second reason is the difference in timing criticality (slack distribution) of the testcases before optimization. Table VII shows the timing criticality of each testcase as the number of critical paths within a specific range of timing. More paths in the 65 nm testcases have delay values near the MCT, which makes it difficult for the dose map optimization to remove all those paths to improve timing. However, in the 90 nm testcases, the number of such critical paths is small, making it easier for the dose map optimization to improve timing. For these reasons, more substantial leakage and timing improvements are observed for the 90 nm testcases.

Table V shows the dose map optimization results using the quadratically constrained program for improved timing

[9]Different smoothness bounds in different directions, i.e., slit and scan directions (see Section II), may be specified, respectively. Here, we use an average example value for both directions.

TABLE VII

PERCENTAGE OF CRITICAL TIMING PATHS IN TI

Design	95–100% MCT (%)	90–100% MCT (%)	80
AES-65	16.54	28.98	
JPEG-65	4.80	9.89	
AES-90	0.91	4.54	
JPEG-90	0.12	0.35	

on both poly and active layers for 65 nm desi results, slightly better timing improvement is simultaneous modulation in both gate length a Table VI shows the dose map optimization the quadratic program for improved leakage poly and active layers. Again, only the 65 n tested. From the results, slightly better leakag is obtained using simultaneous modulation and gate width than only using gate length m maximum change in gate width is 10 nm accord sensitivity -2 nm/% and dose correction range relatively small compared with the transistor wi the 65 nm standard cell library (the minimum t in 65 nm cells is around 200 nm, while the max more than 650 nm). As a result, there is only of gate width modulation on the cell's delay and the related timing and/or leakage improve significant.

In one case (JPEG-65 with $5 \times 5\,\mu m^2$ grids i dose map optimization using simultaneous gate length modulation obtains slightly worse resu only gate length modulation. We attribute this more fitted parameters (i.e., B_p and γ_p for gat delay and leakage) in estimation of cell delay which can introduce more estimation errors. Fr delay model tables of 36 different 65 nm standar for all the arcs (i.e., rise and fall) with all combinations, we perform curve fitting for ce gate length using the least square method. W length changes, 21 different characterized libra corresponding to the 21 different dose values in Table II. In this case, the maximum sum the residuals for all the fitted curves is 0.000 gate length and gate width change, total 441 characterized libraries are needed, which is a 21 different dose values for the poly layer (i.e. gate length) and 21 different dose values for t

different sizes of the rectangular grids, the smoothness bounds are also elaborated, i.e., the effective smoothness bound of a given smoothness value is different for different rectangular grids. For example, the effective smoothness bound of smoothness value $\delta = 2$ over $50 \times 50\,\mu\text{m}^2$ grids (i.e., 2%/50 μm) is tighter than that over $10 \times 10\,\mu\text{m}^2$ grids (i.e., 2%/10 μm). As mentioned in the Introduction, the Zeiss/Pixer CDC technology also enables adaptivity in the manufacturing flow to meet the required CD specifications. We note that our methods can be used for any emerging technology that enables the fine-grain tuning of CD (i.e., along with relaxed effective smoothness bound) during manufacturing. Moreover, the sizes of our testcases (Table I) are very small, with the largest area (90 nm JPEG-90) being only a little over 1mm^2. For designs of larger sizes, we anticipate that our methods will obtain better timing and leakage improvements.

VI. Conclusion

We have proposed a novel method to improve the timing yield of the circuit as well as reduce total leakage power, using design-aware dose map and dose map-aware placement optimization. We focus mainly on the placement-aware dose map optimization. The dose map-aware placement optimization is also attempted on a placement-aware timing and leakage optimized dose map. The proposed method is based on the fact that the exposure dose in the exposure field can change the gate/transistor lengths and widths of the cells in the circuit, which is useful for optimization of gate delay and gate leakage power. Our ongoing work includes extension of the dose map optimization methodology to minimize the delay variation of different chips across the wafer or the exposure field.

Appendix
Dose Map-Aware Placement

A. Cell-Swapping Based Optimization

After a placement-specific dose map has been calculated, it is natural to ask whether a dose map-specific placement can further improve the result. In this Appendix, we describe a simple cell swapping-based dose map-aware placement (*dosePl*) optimization. The *dosePl* problem can be stated as follows. Given the original placement result and a timing and leakage-aware dose map, determine cell pairs to swap for timing yield improvement.

critical cells to low-dose regions, to further enha
performance under leakage constraint.

We define the *bounding box of a cell* as
box of all the cell's fanin cells and all of its
as well as the cell itself. Fig. 9 shows the bou
a (NAND3) cell, denoted by the dashed line.
is that moving a cell within its bounding box
likelihood of increasing total wire length or tim
moving it outside the bounding box. Thus, we
cells $cell_l$ with bounding box b_l and $cell_m$ with
b_m in different dose regions, such that $cell_l$ is in
is in b_l. With this restriction, we filter out candid
that are too disruptive to wirelength and timing

(1) *Additional Heuristics to Avoid Wireler*
When two cells satisfy the condition that the
in each other's bounding boxes, it is still pos
wirelength to increase. We thus adopt the follow
to further filter out unpromising cell pairs.

- Distance between the two cells to be swap
distance between two cells is very large,
cell swapping on total wirelength is pot
Therefore, we avoid considering swaps of
far apart.[10]
- Half-perimeter Wire Length (HPWL)-base
comparison We may also filter cell swaps
updated HPWL-based wirelength estimate
estimated wirelength increase for all incid
the four nets incident to the "NAND" cell i
low a predefined threshold (e.g., 20% in ou
reported below) will the cell swap be atter

(2) *On the Number of Swaps and Cell Priorit*
critical path, several cell swaps may suffice to r
delay, and further cell swapping will introduc
wirelength and leakage increase. So, an upper
number of cells swapped for each critical pat
in our heuristic's implementation (e.g., one ce
path in the experiments below). The priority for
during swapping is decided according to the
factors.

- Number of critical paths that pass through
more critical paths that pass through a given

[10]In the experimental results below, this threshold is chos
to the gate pitch, which is computed as the chip dimensi
square root of gate count in the chip.

most timing-critical to least critical. Therefore, cells on more-critical paths always have higher priorities than cells on less-critical paths. Cells in the same critical path are sorted in non-increasing order of weights that are computed as

$$W(cell_l) = \sum_{cell_l \in C_l} e^{-slack(C_l)}. \quad (13)$$

(3) *On the Leakage Power Increase:* When $cell_l$ and $cell_m$ are to be swapped, the increase in their combined leakage power $\Delta Leak_{l,m}$ may be estimated beforehand. If $\Delta Leak_{l,m}$ is less than a given fraction γ_4 (e.g., 10%) of the original leakage power $Leak_{l,m}$ of the two cells, they will be swapped. Otherwise, no swapping will be performed, so as to avoid large leakage increase. Because one cell is swapped to a higher dose region (i.e., leakage increases) and the other one is swapped to a lower dose region (i.e., leakage decreases), it is not always the case that cell swapping will result in leakage power increase.

(4) *Pseudocode of the Cell Swapping Heuristic:* The pseudocode of one round of our cell swapping heuristic is given as Algorithm 1. In each round of cell swapping, a maximum of γ_5 swaps are allowed (e.g., one swap for each round of cell swapping in our experiments). The cell swapping process is based on the critical paths, which are first sorted in non-increasing order according to their slacks. Cells of a given path are then swapped. Since it is not necessary to swap all the cells in a critical path to improve its timing, the swapping process for a path is terminated when the number of swapped cells reaches a user-defined parameter γ_1 (in our experiments, up to one cell is swapped on each path). For a given candidate swapping pair, the swapping process checks the bounding box constraint, the dose constraint, and distance, then computes HPWL-based wirelength increase and leakage increase when the pair is swapped. If a candidate pair passes all the checks, its cells are swapped and we update the number of swapped cells for the corresponding critical paths. The cell swapping process continues until all critical paths are processed or the number of swaps reaches γ_5. When one round of the swapping process finishes, the perturbed placement is legalized and routed by an engineering change order (ECO) placement and routing process. After final (ECO) routing, golden timing analysis is performed with updated parasitics to evaluate the circuit delay improvement. If the circuit delay is improved, the swapping is accepted. Otherwise, the swapped cell instances are rolled

16. **for all** $cell_m \in NC$ **do**
17. **if** $dist(cell_l, cell_m) > \gamma_2$ **then break**; **end if**
18. **if** $cell_l \in b_m$ and $cell_m \in b_l$ and ΔHPW
$\Delta HPWL(cell_m) < \gamma_3$ and $\Delta Leak_{l,m} < Leak_{l,m} \cdot$
19. Swap ($cell_l$, $cell_m$);
20. Update the number of swapped cells $n(c_s)$ fo
such that $cell_l \in c_s$;
21. Set $flag \leftarrow$ **true**;
22. $numSwaps$ ++;
23. **if** $numSwaps \geq \gamma_5$ **then return**; **end if**
24. **break**;
25. **end if**
26. **end for**
27. **if** $flag$ = **true then break**; **end if**
28. **end for**
29. **end for**
30. **end for**

TABLE VIII

EXPERIMENTAL RESULTS OF DOSE MAP OPTIMIZATION
USING QUADRATICALLY CONSTRAINED PROGRAM F
TIMING, FOLLOWED BY INCREMENTAL PLACEMEN

Testcase	AES-65			J
	Nom L_{gate}	*QCP*	*dosePl*	Nom L_{gate}
MCT (ns)	1.638	1.607	1.601	2.179
Leakage (μW)	448.0	441.4	441.4	2915.5
Runtime (s)	–	108	40	–

The chip is partitioned into rectangular grids of size 5 ×
correction range is ±5%, and dose smoothness bound is δ

back to their previous cell masters and anc
cell swapping is performed with those swappe
as fixed (i.e., those cells cannot be swapped
following cell swapping process). The total nu
of cell swapping in our experiments is 10. A
of swapping rounds can obtain better timing
However, the improvement cannot be guarantee
swapping cells on minimum-slack critical path
timing yield, but those cells may not be swapp
swapping constraints, e.g., distance, leakage in

B. Experimental Results

The experimental results of dose map-p
optimization are given in Table VIII. From the
(*QCP*) first improves the timing yield under
constraint. Cell-swapping based *dosePl* further
results.

Fig. 10 shows four slack profiles of design A
ing: (1) the original design (*Orig*); (2) the de
after dose map optimization on poly layer for in

dosePl, and the biased design when all the gates in the top 10 000 critical paths receive maximum possible exposure dose (+5%).

(dose correction range is $\pm 5\%$, smoothness bound is $\delta = 2$, and rectangular grids are of sizes $5 \times 5\,\mu\text{m}^2$); (3) the design (*dosePl*) after placement optimization, and (4) the design (*Bias*) when all the gates in the top 10000 critical paths are enforced using maximum possible dose (i.e., +5% on the original dose). The purpose of enforcing the maximum possible exposure dose on the critical gates is to find out the optimization headroom left after *DMopt* process. From Fig. 10, the worst slack of the original design is first improved by dose map optimization process, and then further improved by placement optimization process. However, it is difficult for the dose map and placement optimization to improve the slacks for all the paths on the "hill" around the critical slack value of 0 ns. Besides, as shown by Table II, though there is seeming headroom left between the optimized design and the "optimal" (*Bias*) design, it is impossible to reach the "optimal" design without dramatically increasing the total leakage power.[11]

REFERENCES

[1] K. Jeong, A. B. Kahng, C.-H. Park, and H. Yao, "Dose map and placement co-optimization for timing yield enhancement and leakage power reduction," in *Proc. IEEE/Assoc. Comput. Mach. Design Autom. Conf.*, 2008, pp. 516–521.

[2] P. Gupta and A. B. Kahng, "Manufacturing-aware physical design," in *Proc. IEEE/Assoc. Comput. Mach. Int. Conf. Comput.-Aided Design*, 2003, pp. 681–687.

[3] S. Bhardwaj, Y. Cao, and S. Vrudhula, "Statistical leakage minimization through joint selection of gate sizes, gate lengths and threshold voltage," in *Proc. Asia South Pacific Design Autom. Conf.*, 2006, pp. 953–958.

[4] P. Gupta, A. B. Kahng, P. Sharma, and D. Sylvester, "Gate-length biasing for runtime-leakage control," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 25, no. 8. 2006, pp. 1475–1485.

[5] [Online]. Available: http://wps2a.semi.org/cms/groups/public/documents/membersonly/van_schoot_presentation.pdf

[6] I. Pollentier, S. Y. Cheng, B. Baudemprez, *et al.*, "In-line lithography cluster monitoring and control using integrated scatterometry," in *Proc. Int. Soc. Opt. Engineers Data Anal. Modeling Process Control*, vol. 5378. 2004, pp. 105–115.

[7] J. B. van Schoot, O. Noordman, P. Vanoppen, *et al.*, "CD uniformity improvement by active scanner corrections," in *Proc. Int. Soc. Opt. Engineers Symp. Opt. Microlithography*, vol. 4691. 2002, pp. 304–314.

[14] *Synopsys PrimeTime* [Online]. Available: http://www.

[15] *Cadence SOC Encounter* [Online]. Available: http://w

[16] [Online]. Available: http://www.smt.zeiss.com

[17] A. B. Kahng, "Key directions and a roadmap for ele manufacturability," in *Proc. Eur. Solid-State Circuits* 83–88.

[11] We have also tried to follow the dose map-specific placement ECO with a second dose map optimization, i.e., applying the *DMopt* and *dosePl* optimizations in alternation. However, this did not result in any further improvement.

Kwangok Jeong (S'07) received degrees in electrical engineering fr versity, Seoul, Korea, in 1997 and Since 2006, he has been pursui gree from the VLSI CAD Laborat California, San Diego.

He was with the Computer-A Team, Samsung Electronics, Se 1999 to 2006. His current researc physical design and very large design-manufacturing interface.

Mr. Jeong received three Best Paper Awards at the Sa Conference, in 2001, 2002, and 2004, respectively, durin Samsung Electronics, and the Honorable Outstanding Res 2005.

Andrew B. Kahng (F'10) recei gree in applied mathematics (phys College, Cambridge, MA, and th degrees in computer science from California at San Diego (UCSD),

He was an Assistant Professor sociate Professor in 1994, and a 1998, with the Department of C University of California, Los Ang was a Professor with the Departm Science and Engineering (CSE) a of Electrical and Computer Engineering, UCSD, La Jolla founded Blaze DFM, Inc., Sunnyvale, CA, and was the CT until resuming his duties with UCSD in 2006. He has pu journal and conference papers. Since 1997, his research in design for manufacturability has pioneered methods for the shift mask layout, variability-aware analyses and optimizatio chanical polishing fill synthesis, and parametric yield-d methodologies for chip implementation.

Dr. Kahng was an Associate Chair with the UCSD CSE 2003 to 2004. He was the Founding General Chair of the for Computing Machinery (ACM)/IEEE International Symp Design, a Co-Founder of the ACM Workshop on System-L Prediction, and defined the physical design roadmap as Design Tools and Test Technology Working Group (TWG) i 1999 renewals of the International Technology Roadmap fo From 2000 to 2003, he was the Chair of both the U.S. D Working Group and the Design International Technology W he continues to serve as a Co-Chair of the Design Inform Working Group. He has been an Executive Committee MARCO Gigascale Systems Research Center since its i He has received the National Science Foundation Resea Young Investigator Awards, three Best Paper Nominations, a Awards.

Semiconductor Research Corporation Inventor Recognition Award.