DOE-Based Extraction of CMP, Active and Via Fill Impact on Capacitances

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***Abstract*—Chemical–mechanical polishing (CMP), active and via fills have become indispensable aspects of semiconductor manufacturing. CMP fills are used to reduce metal thickness variations due to chemical–mechanical polishing. Via fills are used to improve neighboring via printability and reliability of low-k and ultra low-k dielectrics. Active region fills are used for STI CMP uniformity and stress optimization. Although modern parasitic extraction tools accurately handle grounded fills and regular interconnects, such tools use only rough approximations to assess the capacitance impact of floating fills, such as assuming that floating fills are grounded or that each fill is merged with neighboring ones. To reduce such inaccuracies, we provide a design of experiments (DOE) which complements what is possible with existing extraction tools. Through the proposed DOE set, a design or mask house can generate *normalized fill tables* to correct for the inaccuracies of existing extraction tools when floating fills are present. Golden interconnect capacitance values can be updated using these normalized fill tables. Our proposed DOE enables extensive analyses of fill impacts on coupling capacitances. We show through 3-D field solver simulations that the assumptions used in extractors result in significant inaccuracies. We present analyses of fill impacts for an example technology and also provide analyses using the normalized fill tables to be used in the extraction flow for three different standard fill algorithms. We also extend our analyses and methodology to via fills and active region fills, which have more recently been introduced into semiconductor design-manufacturing methodologies and for which sufficient understanding is still lacking.**

***Index Terms*—Active region fill, chemical–mechanical polishing (CMP) fill, coupling capacitance, RC extraction, via fill.**

I. Introduction

CHEMICAL–mechanical polishing (CMP) (dummy) fills are inserted into the layout of metal layers to reduce metal height variations within a die. Ideally, such fill shapes should not alter the capacitances of or between interconnects. On the other hand, if the capacitances are going be altered by a nonnegligible amount, they should be correctly accounted for in the RC extraction. Design rules help reduce the increase in capacitances due to fill, but are by no means sufficient to eliminate the capacitance impact of CMP fills.[1] Furthermore, current extraction tools are inaccurate when it comes to extraction of floating fills.

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[1]For example, second neighboring-layer coupling can be significant, yet there are no explicit design rules to restrict such a coupling component.

The semiconductor and design industries must accurately incorporate the impact of fills during extraction. In this paper, we present a parameterized design-of-experiment (DOE)-based methodology to improve the accuracy of extraction in the presence of fills. The addition of fills can be handled by either the design house, the mask house, or the foundry. In the latter two cases, while there is limited control of capacitance increases due to lack of design information (timing constraints and critical paths, functionality and stimuli, etc.), the capacitance impact analyses enabled by our DOE are still useful. When the design house inserts fills, some or all of the fills can be included in the RC extraction flow. In this case, our proposed DOE enables an accurate analysis of the impact.

Our paper is organized as follows. In Section II, we briefly review relevant previous work. Then, following motivations (Section III), where we identify inaccuracies in current extraction tools, we present in Section IV our proposed DOE methodology. In Section V, we provide details of the simulation structures for our DOEs and show how the DOE algorithms are implemented. In Section VI, we provide an insight on the keep-off distance, which is a key design rule related to CMP fills. We then provide a means to include the height variations due to CMP. In the experimental results section, we provide exhaustive simulation results for our experimental design for three types of fill algorithms: standard (traditional), staggered, and two-pass. We show how much inaccuracy we would have observed, had we used approximations such as merged fills or grounded fills.

This paper extends [1] with more detailed explanations of our methodology and with new DOEs for via fills and active fills. Via fills are typically used between CMP fills of two neighboring layers to improve close-proximity via printability and dielectric reliability. With increasing use of via fills in 65 nm and below process nodes, their impact on capacitances needs to be characterized more accurately. Active region fills are used in stress optimization and to control shallow trench isolation (STI) height variations due to STI CMP.[2] We provide a corresponding DOE which targets the impact of active region (AR) fills on capacitances. Since via and active region fills are relatively recent introductions to standard methodologies, our resulting observations open new grounds for designers and the design-manufacturing interface.

II. Previous Work

Stine *et al.* have proposed CMP models in [2]. Lakshminarayanan *et al.* [3] have proposed electrical rules to reduce resistance variations due to CMP and proposed width-dependent

[2]If uncontrolled, STI step height variations can lead to, e.g., increased threshold voltage variability.

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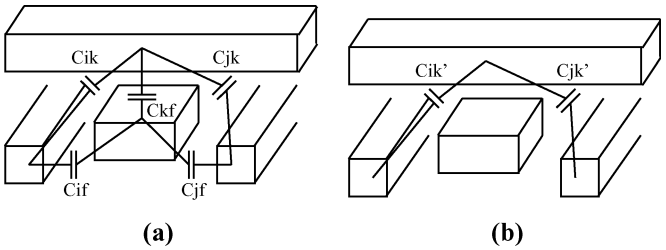

Fig. 1. Graph-based capacitance reduction. (a) Initially, capacitances between all metals are computed. (b) Capacitances to fills eliminated one by one.

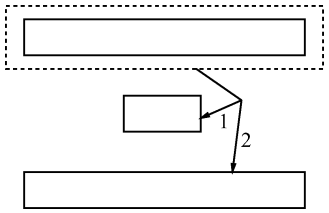

Fig. 2. Random walk-based methods.

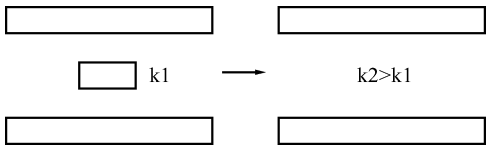

Fig. 3. Effective k fill elimination method.

spacing rules to be used. Zarkesh-Ha *et al.* [4] have linked the interconnect density to CMP models and circuit delay. Cueto *et al.* [5] have provided an algorithm to extract the floating fills. Yu *et al.* [6] have introduced a field solver which can take into account floating fills by using floating fill conditions in the direct boundary element equations. Wang *et al.* [7] have used a minimum variance iterative method for density assignment. Nelson *et al.* [8] have determined fill size, shape, and proximity to reduce parasitic capacitances using a 2-D analysis. Batterywala *et al.* [9] have presented an extraction method, where fills are eliminated one by one using a graph-based random walk algorithm while updating the coupling capacitances. Kurokawa *et al.* [10] have shown that interlayer coupling can be more important than intralayer coupling. Lee *et al.* [11] have analyzed the impact of intralayer fills on capacitances. Kahng *et al.* [12] have provided design guidelines to reduce coupling. In [13], Kurokawa *et al.* have provided fill patterns to reduce interconnect coupling. Park *et al.* [14] have presented an exhaustive method to generate capacitance tables for fills. Chang *et al.* [15] have presented a charge-based capacitance measurement method to analyze the impact of fills. In [16], Lee *et al.* have analyzed the impacts of fills using an effective permittivity model. Kim *et al.* [17] have proposed compact models for the impacts of fills.

A graph node reduction-based technique was proposed in [9] where, initially, capacitances between all metals are computed. Fig. 1 shows such a graph node reduction-based technique. Metals are represented by the nodes of a graph and the capacitances by the edges. For the capacitance computation, voltages of floating metals are first estimated by interpolation. Coupling capacitances are then computed assuming charge on a floating fill is zero. In the next step, capacitances between interconnects and fills, and between two fills, are eliminated using the following formulas:

$$Cik' = Cik + \frac{Cif \cdot Ckf}{Cff} \tag{1}$$

$$Cjk' = Cjk + \frac{Cjf \cdot Ckf}{Cff}. \tag{2}$$

Following the reduction, fill nodes are eliminated one by one. This is a very slow process as the number of fills is large.

There also exist random walk-based methods which can account for floating fills. These methods are used by tools such as Magma Quickcap and Synopsys Raphael NXT. Electrostatic equations are solved using Gauss' Law. A random walk starts at a Gaussian surface and ends at the same or another interconnect, yielding a coupling capacitance estimate. A random walk is illustrated in Fig. 2. The potential of fills is estimated using an integration over their surface. Results can be limited to small layouts for a reasonable runtime.

Another popular method is using an effective dielectric constant and eliminating the fill. Such a method is described in [18]. An effective dielectric constant method is illustrated in Fig. 3. Fills are dropped and the effective dielectric constant is increased in return. This approach can be considered as a compact modeling approach. Due to multilayer interactions, compact models usually are not sufficient unless for very restrictive configurations.

There is still a need for public DOEs for analyzing fills, generating efficient DOEs, and incorporating the resultant data into extraction. In this paper, we try to achieve this and provide practical methods and parameterized DOEs for any design house or foundry to use on their technology to understand, analyze, and characterize the impact of fills in their flow.

III. Motivation

Current extraction, tools have known inaccuracies for inclusion of floating fill impact on final coupling and total capacitances.[3] Most tools use simplifications to account for effects of fills. In the following, we present simplifications used by extraction tools. Along with each simplification, we also indicate how much error can be introduced for a typical structure.

Assuming Floating Fills as Grounded: Some extractors assume that the floating fills are grounded. These extractors use the same capacitance tables, which are also used to extract the regular interconnect capacitances. This assumption introduces results in up to 2× and 10× underestimation for first and second neighboring layer coupling capacitances, respectively, as well as almost eliminating the intralayer coupling capacitances.

Merging the Fills: A popular method is to merge all the neighboring fills within a layer into one large fill. The larger fill is constructed such that it is the smallest rectangular prism which can include all neighboring fills and does not include any

[3]The type of fill of interest to this paper is floating fill, since grounded fills are not versatile due to routing and increased total capacitances, and their extraction is not a concern to current extraction tools.

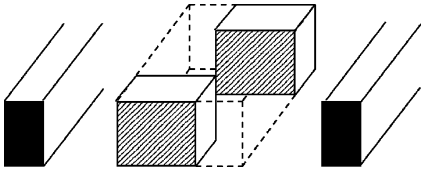

Fig. 4. Fill merging methodology. Fills are patterned and interconnects are represented by dark lines. Dashed box shows merged fill, resulting from convex hull of intralayer neighboring fills.

part of an interconnect. This approach is illustrated in Fig. 4, where fills are replaced by the larger fill indicated by the dashed block.

Merging the fills results in up to 23× average overestimation of the intralayer for small keep-off distances and underestimation of second neighboring-layer coupling capacitances up to 4×, depending on the fill algorithm. The first neighboring-layer coupling capacitance can be over or underestimated up to 2×. Another extension of this assumption is accounting for fill density only. Some extraction tools take density of fills as input to their models. In this case, different fill patterns yielding the same density are assumed to yield the same results. However, different patterns yielding the same fill density are known to yield different coupling capacitances.

Other Inaccuracies for Floating Fill Consideration of Extraction Tools: Another important inaccuracy is related to the first and second neighboring interlayer coupling, i.e., coupling between layers M and $M+1$, and between $M-1$ and $M+1$, respectively. Patterns on M and $M+1$ impact the coupling between the interconnects in these layers. As fills on layer M are introduced, the coupling between interconnects on layers $M-1$ and $M+1$ are impacted according to the pattern in M. So, assumptions such as merged or grounded fills will result in inaccuracies.

IV. Methodology

Current extraction tools do not contain accurate DOEs for floating fills, although the DOEs for regular interconnects are sufficient. We provide an extensive DOE set for the floating fills. Our proposed method consists of a parameterized field solver DOE and normalization of results to enable a normalization-based extraction methodology for fills. In the traditional flow, after interconnects are designed and fills are automatically or manually inserted into the design, the extraction tool is run over the layout. As the extraction tools use one of the methods analyzed in the previous section, the results will not be very accurate.

Our proposed flow is illustrated in Fig. 5. Essentially, we propose to run an extraction tool over the interconnects with no fills first. This step is accurately handled by the current extraction tools. Then, using the fill DOE, we propose to update the impact of fills on coupling and total capacitances using a normalization step. The normalization is done with respect to the same structure and interconnect parameters without any fills in between interconnects. The capacitances with the fills are normalized with respect to capacitances without the fills. This results in normalized values close to and higher than one, whenever the

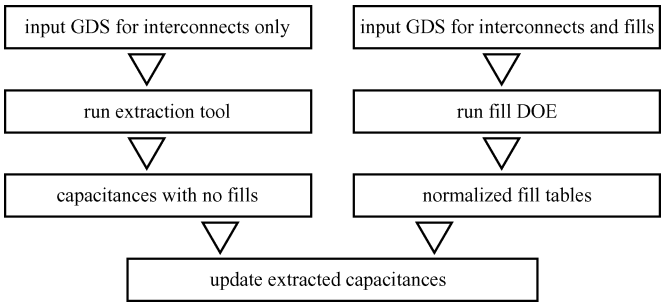

Fig. 5. Proposed flow to incorporate floating fill impact.

capacitance increases due to fills. The normalized couplings are mostly expected to be larger than one, as fills usually increase coupling. The normalized data in the capacitance tables are then used to convert the result of extraction with no fills to accurate results accounting for the presence of floating fills. We use 3-D field solutions for our DOE and hence the results will be much more accurate than known approximations. Furthermore, this flow makes it possible to compare the impact of different fill algorithms using results of the same extraction for interconnects with no fills in between.

Integration with Extraction Tools: Extractors use a DOE for regular interconnects. They may use an additional DOE for floating fills, for which the users have restricted inputs. With the proposed method, the DOE for the regular interconnects should still be used and the parasitics with no fills generated through the extractor. The extractor DOE for floating fills can be replaced by the proposed DOE through wrapper scripts which utilize the normalized look-up tables generated through the field solver using the proposed fill DOE, the input netlist, input layout, and the parasitics file generated by the extractor. Alternatively, the proposed DOE may be integrated into the extractor through the tool provider.

V. Fill DOEs

Basic CMP Fill DOE Structure: In this section, we propose our parameterized DOEs. These DOEs can both be used for analysis and characterization of a process, as well as generating capacitance tables.

For runtime to be manageable, we have designed one structure for all DOEs, as shown in Fig. 6.[4] We propose a five-layer structure, with top and bottom plates grounded. Each layer consists of two parallel interconnects facing each other. Parallel interconnects rotated 90° to each other are used in layers $M-1$, M, and $M+1$. Here, layer M refers to the layer in the middle. In layers $M-1$, M, and $M+1$, two parallel interconnects are present, with fills in between placed according to parameters and a selected fill algorithm, the end results of which may look like the ones in [10, Fig. 1], i.e., standard, staggered, two-pass, etc. Layers $M+1$ and $M-1$ include orthogonally oriented interconnects with respect to layer M. Interconnects on layers $M-1$ and $M+1$ overlap with each other, though an additional parameter can be used to introduce shifting of the overlapped

[4]The exception is the parallel neighboring layers DOE (Section V-C), which uses a version where interconnects are parallel in each layer instead of orthogonal.

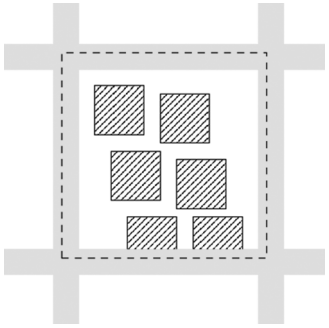

Fig. 6. Basic DOE structure. Structure consists of five layers. Top and bottom are ground planes. Three layers consist of parallel interconnects orthogonal to others across each layer. Structure enables observation of intralayer and first and second neighboring layer couplings in one simulation. Fills are patterned and interconnects are represented by solid gray lines.

interconnects. The simulated structures are parameterized according to the particular fill pattern (algorithm) of interest.

In the figure, interconnects on layer M are drawn vertically, whereas interconnects on layer $M+1$ or $M-1$ are drawn horizontally as solid gray rectangles. We have included in the simulation window, indicated by dashed lines, the half width of each interconnect to account for the reflective boundary conditions. These boundary conditions enable the mirroring of each structure along the dashed lines. Hence, essentially part of a large regular pattern is simulated.[5,6]

The DOE structure is able to provide all the coupling capacitances of interest. For intralayer coupling, capacitances between lines on layer M are used in the proposed structure. For neighboring-layer coupling, capacitances between one line on layer M and $M+1$ each are used in the proposed structure. For second neighboring-layer coupling, capacitances between lines on layers $M+1$ and $M-1$ are used in the proposed structure. For neighboring layer parallel line capacitances, the structure has been modified such that there are two parallel lines on neighboring three layers.

A. Basic CMP Fill Algorithm for Intralayer Coupling

Our fill DOE is given below. Assuming there are four parameters of interest, the algorithm looks like the following:

1) **for each** $w_f = w_f^{\min} : w_f^{\text{inc}} : w_f^{\max}$ {
2) **for each** $w_s = w_s^{\min} : w_s^{\text{inc}} : w_s^{\max}$ {
3) **for each** $c_f = c_f^{\min} : c_f^{\text{inc}} : c_f^{\max}$ {
4) **for each** $w_m = w_m^{\min} : w_m^{\text{inc}} : w_m^{\max}$ {
5) *Run field solver over parameterized structure and add result to a table*}}}}

In this algorithm, w_f and w_s refer to fill width and spacing between fills, respectively. c_f is the number of fill columns between two parallel interconnects for each of the layers $M-1$, M, and $M+1$. w_m refers to metal width. w_f^{inc} corresponds to the increment and is equal to $(w_f^{\max}-w_f^{\min})/(\text{num. of data points})$. Usually, four data points is sufficient to come up with reasonable data tables or compact models. $\min$ and $\max$ for the fill parameters refer to the minimum and maximum values for a parameter, which usually can be decided using the design manual.

In order to enable updating of interconnect coupling and total capacitances with fills added, the fill capacitance models need to be normalized with respect to the same configuration including no fills. Hence, the same DOE structures are run with no fills present between the interconnects and the results with fills are normalized with respect to the results without fills. During extraction, when interconnects are seen in design, coupling capacitances between interconnects are multiplied by the normalized DOE results.

The runtime complexity of the algorithm is a function of the number of parameters and number of data points for each parameter. So, it is highly recommended to look for ways to reduce these. Herein, we provide a couple of guidelines. If a relationship between a parameter and the impact is known to be linear, then only two data points for that parameter should be selected. Certain parameters change at the same time as other parameters. For example, dielectric height changes with the dielectric constant. These kinds of parameters need to be tied to each other so that only one loop is executed for both. If sensitivity of coupling to a parameter is known to be low, then this parameter can be thrown out by setting it to a constant. Similar to field solver setups with current extraction tools, a careful selection at this step will be highly rewarding in terms of runtime.

B. CMP Fill DOE for Neighboring Layer

There are two types of interlayer couplings. The first one is first-neighboring-layer coupling. For an interconnect on layer M, a neighboring layer refers to interconnects on layers $M-1$ and $M+1$. On the other hand, second-neighboring layer refers to coupling between interconnect on layer $M+1$ and interconnects on layers $M-1$. Neighboring coupling is mainly of the fringing type, whereas second-neighboring coupling is of area overlap type, as the interconnects surfaces face each other.

Neighboring-layer interconnects are most of the time orthogonal to each other to reduce coupling. A crossover structure in 3-D simulation yields exact coupling between the interconnects. However, the addition of fills around the interconnects increases this coupling.

There are two extreme cases for the location of these fills. For worst case coupling, the fill can be overlapping the next layer interconnect from the top view. This situation is shown in Fig. 7(b). In the figure, the shaded rectangles are the fills on layer M. The least coupling occurs when the fills on layer M are shifted. This is shown in Fig. 7(a).[7] Similarly, fills on layers $M+1$ or $M-1$ also have worst and best case coupling positions. The corresponding DOE consists of evaluating all incremental configurations between these worst and best cases for neighboring layers. Hence, one parameter is added to evaluate the fill shifts.

[5]While implementing the DOE structures, interconnect lengths are selected long enough to enable a repetitive pattern according to reflective boundaries. The given parameters otherwise define the simulation structure unambiguously.

[6]While constructing the fill tables, the capacitances are normalized with respect to the interconnect length if the coupling is between parallel interconnects. If orthogonal, we have recorded the capacitance without normalization.

[7]The shifting will impact coupling even with staggered fill patterns, especially if fill widths are large.

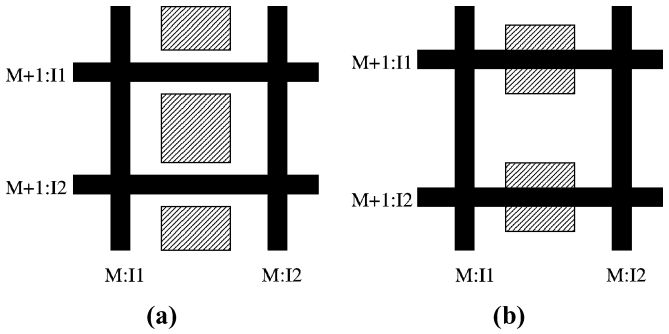

Fig. 7. Interlayer coupling for neighboring layers. (a) Fills on layer M (vertical) intersect minimally with interconnects on layers $M-1$ and $M+1$ (horizontal, overlapping). (b) Fills on layer M shifted and intersect maximally with interconnects on layers $M-1$ and $M+1$.

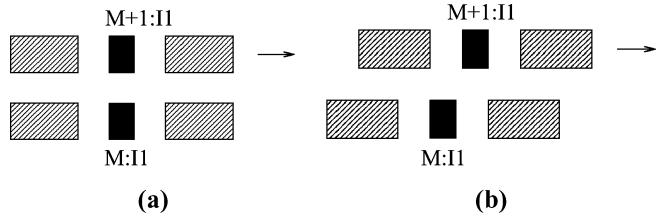

Fig. 8. Interlayer coupling for parallel neighboring lines. (a) Layer M and $M+1$ interconnects intersect. (b) Layer $M+1$ shifted.

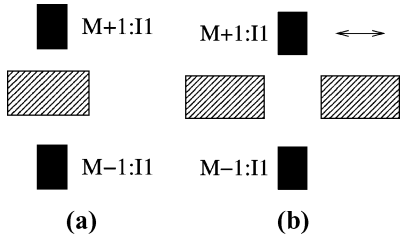

Fig. 9. Interlayer coupling for second neighboring layers. (a) Fills on layer M intersect maximally with interconnects on layers $M-1$ and $M+1$. (b) Fills on layer M shifted and intersect minimally with interconnects on layers $M-1$ and $M+1$.

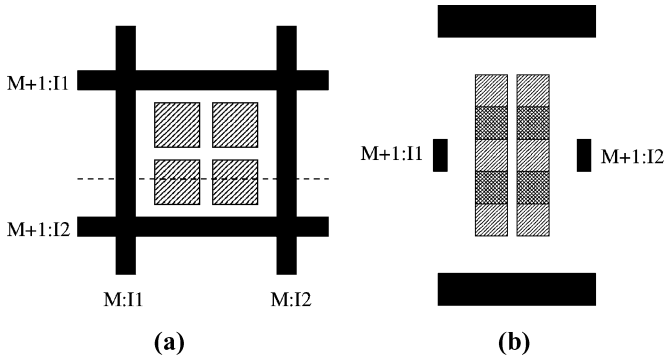

Fig. 10. Via fill DOE simulation structure. (a) Top view. CMP fills laid out in traditional pattern shown. $M+1$ and $M-1$ layer interconnects are overlapping. Top and bottom ground planes not shown. (b) Side view along dashed line. Via fills connecting CMP fills on neighboring layers indicated by darker patterns.

With respect to the originally defined DOE, we can change the DOE by adding the following line:

for each $\mathrm{shift}M = \mathrm{shift}M^{\min} : \mathrm{shift}M^{\mathrm{inc}} : \mathrm{shift}M^{\max}$. {}

Here, $\mathrm{shift}M$ denotes the amount of shift for layer M fills.

C. CMP Fill DOE for Parallel Neighboring-Layer Coupling

It is possible that two consecutive layers have parallel lines. This condition is especially possible in lower layers as well as layers close to clock networks. To handle such a configuration, we have used a modified simulation structure as described previously and illustrated in Fig. 8 from a side view. Worst and best case shifts again need to be implemented. The same DOE presented in the previous section is used with the configuration in Fig. 8.

D. CMP Fill DOE for Second Neighboring Layer Coupling

To analyze the layer M fill impact on $M-1$ and $M+1$ coupling capacitances, the structure shown in Fig. 9 is used. Practically, we have used the same structure from Fig. 7 to reduce the number of simulations and hence handle both DOEs in one simulation. Similar to the previous DOE, positions for fills for best and worst case couplings should be identified.[8] Also, lines in $M-1$ and $M+1$ may not be overlapping. To account for these shifts, $M+1$ lines should be shifted by up to half the allowed pitch. In our DOEs, we have only shifted the fills.

E. Implementation of Other Fill Patterns

The proposed DOE can be extended to other common fill patterns, such as staggered, two-pass, or alternating rectangles. In this section, we briefly describe how we have implemented the DOE for staggered and two-pass methods.

Staggered Fill Algorithm: The staggered fill algorithm produces a shape similar to the standard fill algorithm, except that each row and column is *staggered* by a fixed distance.

Two-Pass Algorithm: Two- or three-pass algorithms insert rectangles of two or three different sizes. Largest rectangles are inserted first and are placed in the middle of two interconnects. Smaller fills are then inserted in the following steps.

F. Via Fill DOE

For the via fill DOE, we have used the simulation structure shown in Fig. 10. Overlapping fills, which are laid out in a traditional pattern, are inserted between parallel interconnects in neighboring layers. On the top and bottom layers, the structure is covered by ground planes representative of dense lines in an actual design. Via fills are inserted between neighboring layer vias to connect them.

[8]For staggered patterns, these shifts are only important for line lengths on the order of the fill width.

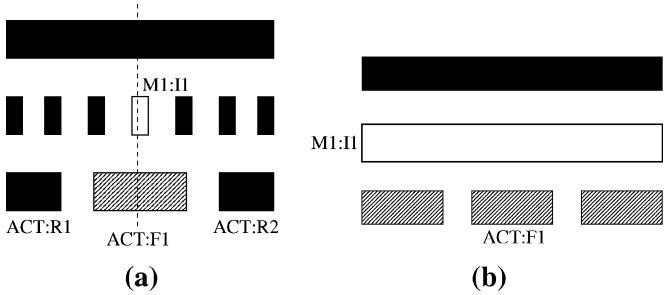

Fig. 11. Active fill DOE simulation structure. (a) Side view. (b) Side view along dashed line. Active regions fills are shown as patterned. Control interconnect is light colored.

TABLE I
PARAMETERS USED IN KEEP-OFF DISTANCE EXPERIMENTS

metal height	dielectric height	dielectric constant	
$0.3\mu m$	$0.3\mu m$	3.1	
keep-off distance	metal width	fill spacing	fill width
0.1-0.9μm	$0.1\mu m$	$0.1\mu m$	$0.5\mu m$

G. Active Fill DOE

The simulation structure for the active fill DOE is shown in Fig. 11. We have, in particular, monitored the coupling between the control interconnect and an active region in the same layer as the AR fills, as well as the coupling between two active regions. The reflective simulation boundary is selected such that an AR fill and two half active region widths can fit into the window from both sides. Hence, the width of the simulation window is given as $\mathrm{wact} + 2 * \mathrm{act2act} + \mathrm{wf}$, where wact is the active region width, act2act is active to active spacing, and wf is the fill width.[9] For the upper layer, as many interconnects as can be fit are included into the window after placing the control interconnect in the middle of the simulation window.

We have used a shift parameter which shifts the interconnects in the layer for the control interconnect altogether as a fraction of the pitch. We have monitored the coupling to the control interconnect during these shifts.

Three AR fills have been used in the orthogonal direction as shown in Fig. 11(b). Three similarly sized and spaced active regions are used. This orthogonal direction corresponds to the widths of transistors formed by the active regions. The reason for using same-sized regions spaced out from each other is the fact that in standard cell designs, transistor rows of equal widths are used.

VI. EXTENSIONS FOR KEEP-OFF RULE AND CMP IMPACTS

A. Keep-Off Design Rule

One of the design rules most relevant to floating fills is the keep-off, or exclusion, distance. This distance is defined as the minimum distance that a fill must be away from an interconnect. In this section, we provide some intuition about this design rule.

This design rule is usually selected such that the coupling capacitance to an intralayer neighbor is negligible as compared to the total capacitance of a line. We have conducted an experiment on a layer with the values in Table I. We have changed the keep-off distance from 0.1 to 0.9 μm and observed the change in coupling capacitance over the total capacitance. This plot is shown in Fig. 12.

[9]Spacing between an active region and active region fill may be chosen larger than the spacing between two active regions to reduce coupling effects.

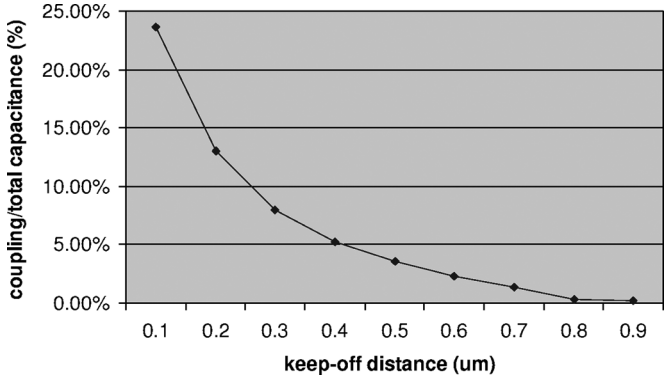

Fig. 12. Intralayer impact of keep-off distance.

The coupling over the total capacitance is practically negligible (3%) around 0.5 μm, hence 0.5 μm is likely to be selected as the keep-off distance for the layer for which this experiment has been conducted. As the fills are allowed to be closer to interconnects, corresponding to a lower keep-off distance, the coupling increases.

Having a large keep-off distance, although advantageous in terms of reducing intralayer coupling, has other issues. It becomes difficult to insert fills into certain regions to satisfy a density constraint, as the distance between two parallel interconnects has to be larger than two times the keep-off distance for fill insertion. Consequently, CMP results in more variations. A second issue is increased coupling of interconnects to neighboring layers. As keep-off distance is increased, less electric flux is present between interconnects of the same layer. However, this flux is directed to interconnects on neighboring layers.

It is possible to have an edge over the design rule if accurate extraction is available. Historically, design rules appear before any analysis and optimization technique. With aggressive technologies, there is an unavoidable need to be able to analyze the effects of each interaction. In the context of the keep-off design rule, as accurate extraction has not been possible, the solution has been to restrict the proximity of fills to interconnects.

With the basic elements of an accurate extraction flow presented in this paper, it is possible to analyze the impact of reduced keep-off distances on coupling and total capacitances as well. This permits greater flexibility of fill algorithms in regions where coupling between lines is not critical. Reducing the keep-off distance enables tighter metal density uniformity, as well as reduced interlayer coupling capacitances.

B. Incorporation of CMP Impacts

CMP is known to result in variations of copper height and hence dielectric height. CMP models exist which give metal heights in a tile within a layer. It is then necessary to tie these heights to the final capacitance values. We have run a set of experiments to evaluate the effect of height variations on the coupling and total capacitances. One such analysis is shown in Fig. 13. The x axis gives the multiplication factor we have used for the height. Values on the y axis are coupling capacitances.

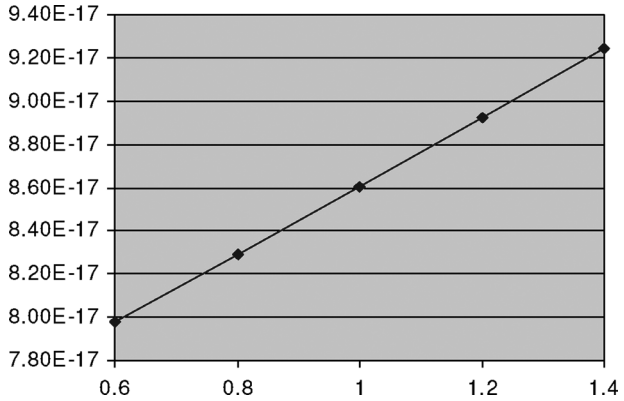

Fig. 13. CMP-induced height impact on coupling capacitance shows linear change. Nominal coupling capacitance in Farads as a function of normalized metal height shown.

TABLE II
PARAMETERS FOR STANDARD FILL ALGORITHM

metal width	$0.1, 0.2, 0.3, 0.4\ (\mu m)$
fill width	$0.4, 0.45, 0.5, 0.55\ (\mu m)$
fill spacing	$0.1, 0.25, 0.4, 0.55\ (\mu m)$
fill shift	$0.25, 0.5, 0.75, 1\ (x)$
metal height*	$0.3, 0.4\ (\mu m)$
dielectric height*	$0.3, 0.4\ (\mu m)$
dielectric constant*	$3.1, 2.8$
number of fill columns	$1, 2, 3$
keep-off distance	$0.3, 0.5, 0.7\ (\mu m)$

We have observed a linear relationship between height and both coupling and total capacitances. The implication is that by just running simulations for two different heights followed by linear interpolation or extrapolation, one can find the CMP-impacted capacitance.

VII. EXPERIMENTAL RESULTS: DOE ANALYSES

Using the proposed DOE, we provide an analysis of relationships we have observed. We have used three different fill algorithms. For each algorithm, we have repeated the simulations for merged fills and grounded assumptions for comparison. We have also simulated the structures with no fills for normalization. Each simulation takes between 10 to 120 s, depending on the selected parameters. All the DOEs take roughly 24–48 hours on a 2.4-GHz 2 processor dual-core server with 2 GB of memory, using the 3-D field-solver Raphael. We have used a minimum grid size of 100 000 nodes per each structure. We have used up to ten licenses and five machines to further reduce the simulation time. The standard fill algorithm is parameterized using the values shown in Table II. Here, dielectric constant, metal, and dielectric heights, changed at the same time, enable simulation of local, intermediate, and global interconnects in the interconnect stack. Parameter names appended by a star sign are changed simultaneously to reduce the number of simulations as described above.

A. Analysis of Intralayer Coupling DOE for Standard Fills

Intralayer coupling exists, e.g., between same-layer interconnects such as $M:I1$ and $M:I2$ in Fig. 7. As fill width increases or fill spacing decreases, intralayer coupling increases as shown in Fig. 14. The increase is more pronounced if there are more columns, i.e., impact due to fills increases from 4.1× to 7.2× as the fill width is increased from 0.4 to 0.6 μm for three fill columns [12]. With one column of fills only, the increase stays around 1.8×. As the fill-to-fill spacing is increased from 0.1 to 0.7 μm, as shown in Fig. 15, the impact decreases from 4.1× to 1.7× for three columns, and from 1.7× to 1.4× for one column.

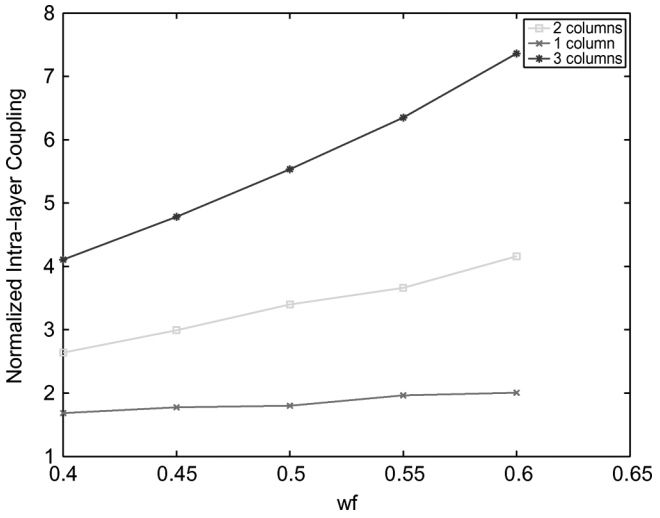

Fig. 14. Fill width dependency of intralayer coupling for different number of fill columns.

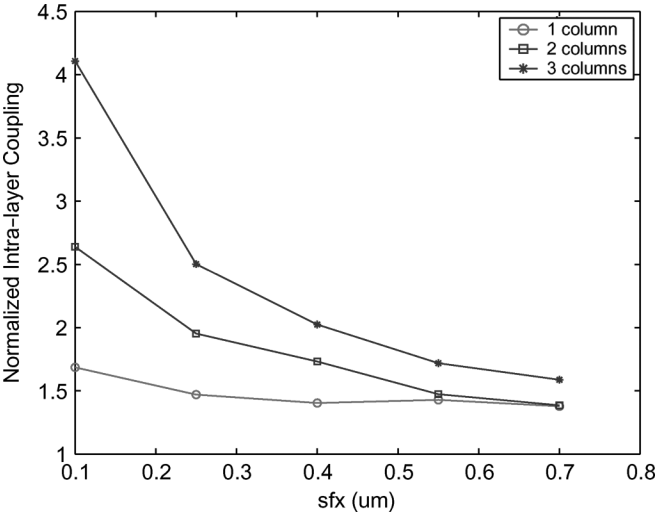

Fig. 15. Fill spacing dependency of intralayer coupling for different number of fill columns.

B. Analysis of First Neighboring-Interlayer Coupling

To illustrate how much the shift can impact the coupling, we have used the representation as shown in Fig. 16. In the figure, each sample corresponds to a set of six simulations, where the shift parameter is changed from 0 to 1 in increments of 0.2. These numbers are multiplicative constants, which are multiplied by half the pitch. One-hundred twenty-five samples are

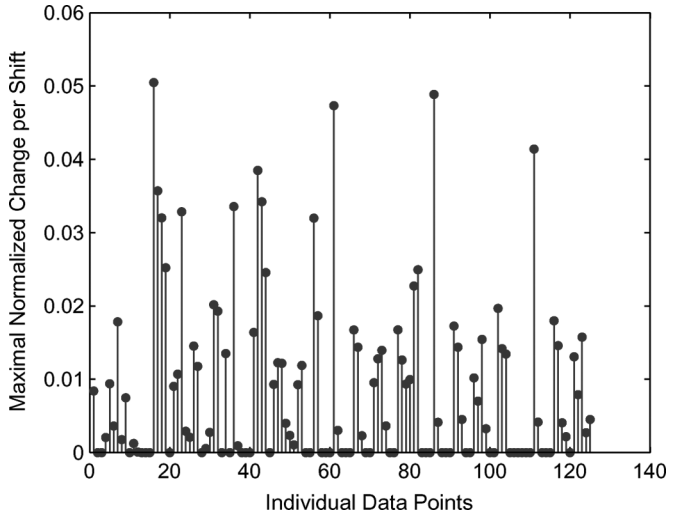

Fig. 16. Normalized data showing maximal change in coupling of neighboring lines.

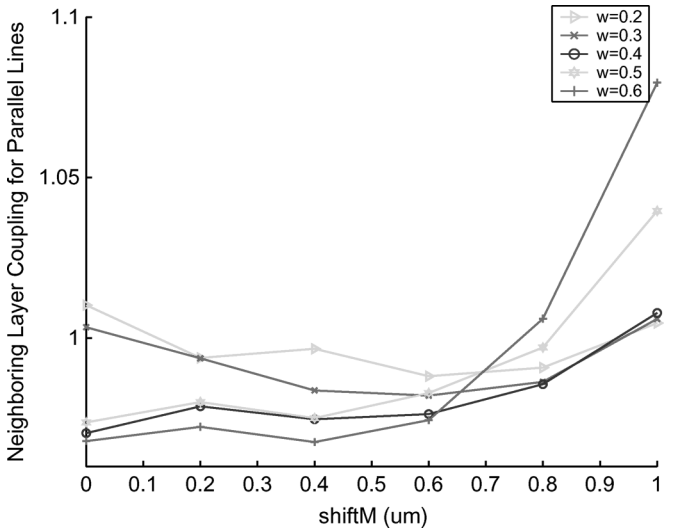

Fig. 17. Neighboring-layer parallel line coupling dependency on amount of M layer shift for various metal widths.

shown, corresponding to 750 field solver simulations. The corresponding sample is computed as follows:

$$s_I = \max(v_i)/\min(v_j) - 1 : \forall v_{i,j} \epsilon v_I. \tag{3}$$

Here, I is a set of six experiments where the shift parameter is changed while keeping other parameters fixed; s_I is the corresponding sample value; and v_i and v_j are values of the experiments in set I. Essentially, the maximum over the minimum of the values of a set gives the maximal change due to the shift operation. A one is subtracted to indicate change.

Interlayer coupling exists between neighboring layer interconnects such as $M : I1$ and $M + 1 : I1$ in Fig. 7. We observe that the maximum of all the samples corresponds to a 5% change due to the shift of fills on layer M only. We consider this amount negligible, considering that we have used an almost best case choice of a 300-nm keep-off distance for this analysis. The data set with largest impact corresponds to fill width, fill spacing, and metal widths of 0.6, 0.4, and 0.4 μm, respectively, in our technology.

C. Analysis of First Neighboring-Layer Parallel Line Coupling

Parallel coupling exists between neighboring layer parallel interconnects, such as $M : I1$ and $M : I+1$ in Fig. 8. The data set with the largest impact corresponds to fill width, fill spacing, and metal widths of 0.4, 0.55, and 0.2 μm, respectively.

We observe that the neighboring layer coupling increases quadratically as a function of the shift parameter for this DOE up to 8% from no shift to half-pitch shift, as shown in Fig. 17. For small shifts, there is negligible impact. As shift is increased, field lines between interconnects on neighboring layers are blocked by a larger fill, which increases the coupling. Larger metal widths usually increase parallel coupling.

D. Analysis of Second Neighboring-Interlayer Coupling

Second-layer coupling observes the coupling between interconnects such as $M - 1 : I1$ and $M + 1 : I1$ in Fig. 9.

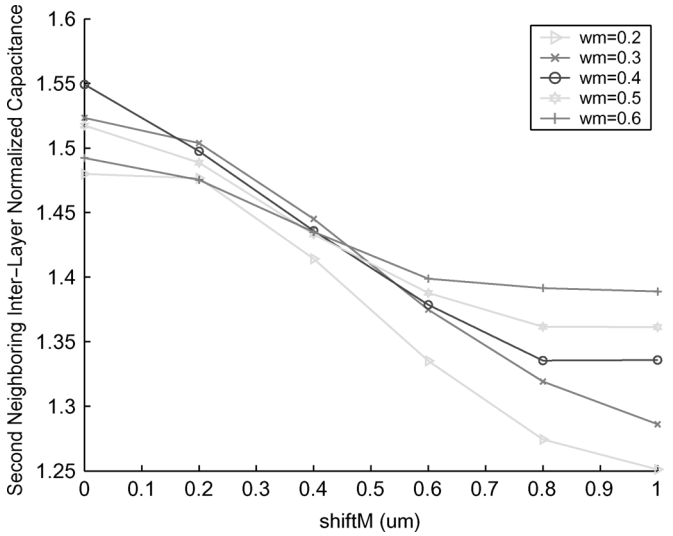

Fig. 18. Fill shift dependency of second neighboring-layer coupling for different metal widths.

Keeping fill width and spacing at 0.4 μm, which corresponds to around 25% density, we have observed the fill shift dependency in Fig. 18.[10] At $\mathrm{shift}M = 0$, there is maximum overlap between interconnects of layers $M - 1$ and $M + 1$, and up to 1.55 times the coupling is seen with respect to no fills. Shifting the layer M fills by changing the $\mathrm{shift}M$ parameter reduces the coupling around 20%. When fill width is small, there is negligible change due to the shift of fills, as field lines between larger interconnects on layers $M + 1$ and $M - 1$ can find a direct path without going through the fills. Changing the fill spacing and keeping fill and metal widths at 0.4 and 0.2 μm as in Fig. 19, we have observed that when the spacing between fills is small, the change in coupling due to the shift in layer M fills is negligible. On the other hand, increasing the spacing between fills (decreasing the metal density from 65% down to 25%) on layer

[10]Exact density depends on the window in which the density is calculated.

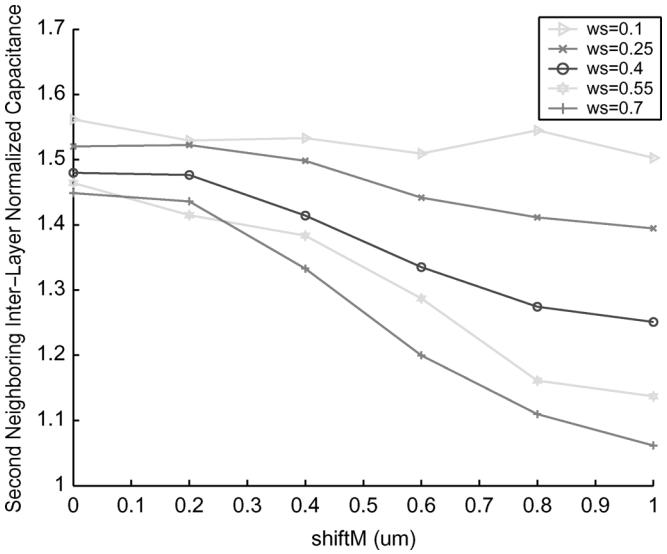

Fig. 19. Fill shift dependency of second neighboring-layer coupling for different fill-to-fill spacings.

TABLE III
PARAMETERS FOR VIA FILL DOE

metal width	$0.2, 0.35, 0.5\ (\mu m)$
fill width	$0.4, 0.5\ (\mu m)$
fill spacing	$0.1, 0.25, 0.4, 0.55\ (\mu m)$
number of rows	$2, 3$
number of columns	$2, 3$
metal height	$0.3\ (\mu m)$
dielectric height	$0.3\ (\mu m)$
dielectric constant	3.1
keep-off distance	$0.3, 0.5\ (\mu m)$

TABLE IV
PARAMETERS FOR ACTIVE FILL DOE

active region width	$0.2, 0.3\ (\mu m)$
active to active spacing	$0.15, 0.3, 0.45, 0.6\ (\mu m)$
active fill width	$0.4, 0.6\ (\mu m)$
metal spacing	$0.2, 0.35, 0.5\ (\mu m)$
metal height	$0.3\ (\mu m)$
shift factor	$0, 0.25, 0.5$
dielectric height	$0.3\ (\mu m)$
dielectric constant	3.1

M results in a 35% change, which is significant and needs to be extracted.

E. Analysis of Other Fill Patterns

We have parameterized the staggered fill algorithm by adding a parameter to define the stagger amount as 0.2, 0.25, or 0.275 μm in addition to the parameters for the standard fill algorithm. For the two-pass algorithm, we have used the two-pass ratio parameter as 2 or 3 to define the larger fill width in this algorithm with respect to the narrower width, which is inserted in the second step.

We have parameterized the via fill DOE using the variables in Table III. We have parameterized the AR fill DOE using the variables in Table IV.

F. Comparison of CMP Fill DOE Results

Table V contains a summary of all the simulations for standard, staggered, and two-pass algorithms. In order to compare the results, we have repeated the field solver simulations for the merged and grounded fills in addition to the proposed DOE. For merged fills, all same-layer neighboring fills are lumped into one, using the convex hull of the fills. For the grounded fills, the same fill pattern as the DOE is used, except each floating fill is connected to ground. In the table, the columns from left to right are the means of normalized DOE, merged, and grounded fill results. These columns indicate the normalized increase in coupling capacitances due to fills. The normalization is with respect to the original interconnect structure with no fills. The last two columns indicate the magnitude of each coupling term as a percentage of the total capacitance.[11] We have included both the maximum and minimum for this ratio. This ratio shows the importance of the given coupling capacitance.

The rows of Table V show intralayer, first-layer neighboring, and second layer-neighboring coupling, respectively, for each fill algorithm. Using the data from the two-pass algorithm as an example, looking at the last two columns, we can say that the intralayer coupling shows less impact as compared to second-layer and first-layer couplings. In terms of accuracy, we can see that the increase in intralayer coupling due to fills can be 10.05 times greater using merged fill as compared to the DOE results, whereas this ratio can be almost negligible for the grounded fills.[12] The DOE results are closer to "actual results" than to the outputs of approximate methods such as merged fill or grounded fill. Merged fills result in an overestimation of coupling capacitances, whereas grounded fills result in a significant underestimation. Although overestimation could be thought of as being advantageous, there are two reasons why we believe it is not an advantage. The first reason is that the overestimation is significantly high. The second reason is that, as we observe the next two rows, we see that the overestimation for the intralayer coupling has resulted in an underestimation for both first and second neighboring-layer couplings due to the fact that merged fills attract most of the flux which would otherwise go to the interconnects on the neighboring layers. Observing the first-layer coupling row, although we would expect an increase in coupling capacitances due to the insertion of fills, we see a reduction for the merged and grounded fills as indicated by normalized values lower than one. This happens due to the flux reasoning above. Considering the fact that these coupling capacitances are large portions of the total capacitance, inaccuracies will be highly important. Standard and staggered algorithms also have shown similar inaccuracies, especially for the intralayer and second-layer couplings. As the proposed DOE uses accurate field solutions which take into consideration the pattern shapes and parameters, the results will be highly accurate with respect to known approximations.

Asymmetric Configurations: Although the simulations have been provided for symmetric parameters for neighboring

[11]The default settings for most extractors cause the tool to neglect coupling capacitances below 1%.

[12]Some of the high increase is due to allowing small keep-off distances, which can be helpful in achieving high-density fills.

TABLE V
COMPARISON OF DOE, MERGED, AND GROUNDED EXTRACTION FOR STANDARD, STAGGERED, AND TWO-PASS ALGORITHMS

STANDARD	DOE	Merged	Grounded	Max. Coupling/Total	Min. Coupling/Total
intra-layer	2.377	10.336	0.002	15.91%	0%
first-layer	1.083	1.123	0.492	22.25%	17.11%
second-layer	1.126	0.726	0.094	6.84%	2.38%
STAGGERED	DOE	Merged	Grounded	Max. Coupling/Total	Min. Coupling/Total
intra-layer	2.579	25.9308	0.0021	23.33%	0%
first-layer	1.131	1.155	0.578	20%	16.32%
second-layer	1.153	0.559	0.107	6.870%	0%
2-PASS	DOE	Merged	Grounded	Max. Coupling/Total	Min. Coupling/Total
intra-layer	5.308	34.607	5.998e-6	3.607%	0.909%
first-layer	1.110	0.531	0.546	19.562%	15.913%
second-layer	1.0160	0.284	0.147	7.776%	3.566%

TABLE VI
ANALYSIS OF VIA FILL DOE FOR Keep-Off $= 0.5\ \mu$m

0.5μm keep-off	mean	max
intra-layer	1.17	1.37
first-layer	1.00	1.02
second-layer	0.99	1.00

TABLE VII
ANALYSIS OF ACTIVE FILL DOE

	min	mean	max
first-layer	0.99	1.28	1.92
intra-layer	0.8	1.00	1.17

layers, it is possible to find nonsymmetric configurations in real designs. For example, the metal width, fill width, and spacing can be different between layers. Our simulations with asymmetric parameters indicate that it is common to see differences up to 40% with respect to the symmetric case. If two layers have similar parameters but the third layer has different ones, the difference may reduce down to 10%. As a general guideline, asymmetric design practices should be avoided as much as possible, as it would make the CMP process optimization harder. All local, intermediate, and global interconnects should have a common set of fill width and spacing sizes within themselves for design uniformity. Even though it is possible to reduce the asymmetry in design using such guidelines, there will still be an asymmetry between transition metal layers, i.e., local to intermediate, or intermediate to global transitions. Such cases, and cases when design has known asymmetries, can be integrated easily into the proposed DOEs. The possible increase in the number of parameters should be controlled by restricting the number of parameters, possibly through considering best and worst case parameter combinations only.

Via Fill DOE: For the via fill DOE, Table VI shows the average normalized change in intralayer, first and second neighboring-layer capacitances. These correspond to $M:I1$ to $M:I2$, $M+1:I1$ to $M:I1$, and $M+1:I1$ to $M-1:I1$ in Fig. 10, respectively. When the keep-off distance is 0.5 μm for the parameters values given in Table III, the latter two change negligibly; however, a 17% increase on the average is expected for intralayer capacitances using the parameters given in Table III. The same experiment for the case when the keep-off distance is reduced to 0.3 μm has not shown a significant change. Hence, we can conclude that keep-off distance has less control over the intralayer capacitance increases unlike the case for CMP fills.

AR Fill DOE: For the AR fill DOE, Table VII shows the average normalized change in first neighboring layer and intralayer capacitances for the parameters values given in Table IV. An average of 28% increase is expected for the first neighboring-layer coupling between the control line $(M1:I1)$ and one of the active regions in the middle $(\mathrm{ACT}:R1)$ in Fig. 11(b). This is not a negligible amount and needs to be incorporated using our DOE. The intralayer coupling between two middle active regions on either side of an AR fill ($\mathrm{ACT}:R1$ to $\mathrm{ACT}:R2$) though can reduce by 20% and increase by 17% depending on the parameters we have used. For example, when the active to active spacing and fill width are increased to 0.6 μm and the upper layer interconnects are dense with minimum widths, a 20% reduction is seen as the field lines between the active region and the control interconnect are pulled away towards the farther away active region with the help of the AR fill. Hence, fills may be utilized to reduce certain couplings at the expense of others. Some coupling capacitances can be reduced by up to 20%, but other couplings from the same line will increase, which may overcome the benefit as the increase can be larger than 20%. Furthermore, for many configurations, couplings cannot be reduced by more than 2%. Meanwhile, total capacitance usually increases. Although it is not possible to reduce the total capacitance, it is possible to control the capacitance increase.

VIII. CONCLUSION

We have proposed a DOE set for extraction tools to generate normalized fill tables which can be used on top of existing extraction tools for accurate extraction of capacitances in the presence of floating fills. We have provided a parameterized design of experiments, in which each design or mask house can implement a flow to analyze and extract capacitances in the presence of fills. This field solver DOE set will complete the DOE set that comes with the extractors, which is not optimal for floating fills. We have shown that the proposed field solver-based DOEs provide significant accuracy improvements over methods and assumptions used by current extraction tools. We have shown that the keep-off distance may not be used as a controlling factor for via fills. Finally, we have found that active region fills results in nonnegligible capacitance change. We believe that our present work will enable a better overall analysis and extraction of the

impact of fills on capacitances in interconnect technologies by virtue of its extensive and parameterized nature.

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REFERENCES

[1] A. B. Kahng and R. O. Topaloglu, "A DOE set for normalization-based extraction of fill impact on capacitances," in *Proc. ISQED*, 2007, pp. 467–474.

[2] B. Stine, D. Boning, and J. Chung, "Modeling pattern dependent variation in CMP processes: Process, consumable, and tool comparison methodologies, metal fill patterning practices, and other issues," CMP User's Group (CMPUG) 1996.

[3] S. Lakshminarayanan, P. J. Wright, and J. Pallinti, "Electrical characterization of the copper CMP process and derivation of metal layout rules," *IEEE Trans. Semiconduct. Manuf.*, vol. 16, no. 4, pp. 668–676, Nov. 2003.

[4] P. Zarkesh-Ha, S. Lakshminarayann, K. Doniger, W. Loh, and P. Wright, "Impact of interconnect pattern density information on a 90 nm technology ASIC design flow," in *Proc. ISQED*, 2003, pp. 405–409.

[5] O. Cueto, F. Charlet, and A. Farcy, "An efficient algorithm for 3D interconnect capacitance extraction considering floating conductors," in *Proc. SISPAD*, Sep. 2002, pp. 107–110.

[6] W. Yu, M. Zhang, and Z. Wang, "Efficient 3-D extraction of interconnect capacitance considering floating metal fills with boundary element method," *Trans. Comput.-Aided Design IC Syst.*, vol. 25, no. 1, pp. 12–18, Jan. 2006.

[7] X. Wang, C. C. Chiang, J. Kawa, and Q. Su, "A min-variance iterative method for fast smart dummy feature density assignment in chemical-mechanical polishing," in *Proc. ISQED*, 2005, pp. 258–263.

[8] M. Nelson, B. Williams, C. Belisle, S. Aytes, D. Beasterfield, J. Liu, S. Donaldson, and J. Prasad, "Optimizing pattern fill for planarity and parasitic capacitance," in *Proc. Int. Semiconductor Device Research Symp.*, 2003, pp. 428–429.

[9] S. Batterywala, R. Ananthakrishna, Y. Luo, and A. Gyure, "A statistical method for fast and accurate capacitance extraction in the presence of floating dummy fills," in *Proc. VLSI Design*, 2006, pp. 129–134.

[10] A. Kurokawa, T. Kanamoto, A. Kasebe, Y. Inoue, and H. Masuda, "Efficient capacitance extraction method for interconnects with dummy fills," in *Proc. CICC*, 2004, pp. 485–488.

[11] K.-H. Lee, J.-K. Park, Y.-N. Yoon, D.-H. Jung, J.-P. Shin, Y.-K. Park, and J.-T. Kong, "Analyzing the effects of floating dummy-fills: From feature scale analysis to full-chip RC extraction," in *Proc. IEDM*, 2001, pp. 31.3.1–31.3.4.

[12] A. B. Kahng, K. Samadi, and P. Sharma, "Study of floating fill impact on interconnect capacitance," in *Proc. ISQED*, 2006, pp. 691–696.

[13] A. Kurokawa, T. Kanamoto, T. Ibe, A. Kasebe, C. W. Fong, T. Kage, Y. Inoue, and H. Masuda, "Dummy filling methods for reducing interconnect capacitance and number of fills," in *Proc. ISQED*, 2005, pp. 586–591.

[14] J.-K. Park, K.-H. Lee, J.-H. Lee, Y.-K. Park, and J.-T. Kong, "An exhaustive method for characterizing the interconnect capacitance considering the floating dummy-fills by employing an efficient field solving algorithm," in *Proc. SISPAD*, 2000, pp. 98–101.

[15] Y. W. Chang, H. W. Chang, T. C. Lu, Y. King, W. Ting, J. Ku, and C. Y. Lu, "A novel CBCM method free from charge injection induced errors: Investigation into the impact of floating dummy-fills on interconnect capacitance," in *Proc. Int. Conf. Microelectronic Test Structures*, 2005, pp. 235–238.

[16] W.-S. Lee, K.-H. Lee, J.-K. Park, T.-K. Kim, Y.-K. Park, and J.-T. Kong, "Investigation of the capacitance deviation due to metal-fills and the effective interconnect geometry modeling," in *Proc. ISQED*, 2004, pp. 373–376.

[17] Y. Kim, D. Petranovic, and D. Sylvester, "Simple and accurate models for capacitance increment due to metal fill insertion," in *Proc. ASPDAC*, 2007, pp. 456–461.

[18] P. R. Findley, "Methods and apparatus for extracting parasitic capacitance values from a physical design of an integrated circuits," U.S. Patent 6,243,653.

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