[13] M. Orshansky, J. C. Chen, and C. Hu, "Direct sampling methodology for statistical analysis of scaled CMOS technologies," *IEEE Trans. Semicond. Manuf.*, vol. 12, no. 4, pp. 403–408, Nov. 1999.
[14] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.
[15] M. Eisele *et al.*, "The impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits," *IEEE Trans. VLSI Syst.*, vol. 5, no. 4, pp. 360–368, Dec. 1997.
[16] *BSIM4.2.1 MOSFET Model—User's Manual*, 2001.
[17] K. A. Bowman *et al.*, "A physical Alpha-power law MOSFET model," in *Proc. Int. Symp. Low Power Electron. and Des.*, Aug. 1999, pp. 218–222.
[18] P. Friedberg *et al.*, "Modeling within-die spatial correlation effects for process-design co-optimization," in *Proc. Int. Symp. Quality Electron. Des.*, Mar. 2005, pp. 516–521.
[19] P. A. Stolk, F. P. Widdershoven, and D. B. M. Klaassen, "Modeling statistical dopant fluctuations in MOS transistors," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1960–1971, Sep. 1998.
[20] J. Tschanz *et al.*, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, Nov. 2002.

# Statistical Timing Analysis in the Presence of Signal-Integrity Effects

Andrew B. Kahng, Bao Liu, and Xu Xu

***Abstract*—Signal-integrity effects have significant impacts on very large-scale-integration performance variation and must be taken into account in statistical timing analysis. In this paper, we study the signal-propagation-delay variation that is induced by crosstalk aggressor signals. We establish a functional relationship between the signal propagation delay and the crosstalk aggressor signal alignment by deterministic circuit simulation and derive closed-form formulas for the statistical distributions of output signal arrival times. Our proposed method can be smoothly integrated into a static timing analyzer, wherein runtime is dominated by sampling the deterministic delay calculation, while probabilistic computation and updating take constant time. Experimental results based on the 1000-$\mu$m global interconnect structures in Berkeley Predictive Technology Model 70-nm technology and industry designs in 130-nm technology show that lack of statistical crosstalk aggressor signal alignment consideration could lead to up to 114.65% (71.26%) differences in interconnect-delay means (standard deviations) and 159.4% (147.4%) differences in gate-delay means (standard deviations). By contract, the method in our earlier work gives within 1.28% (3.38%) mismatch in interconnect output signal arrival time means (standard deviations) and within 2.57% (3.86%) mismatch in gate output signal arrival time means (standard deviations), respectively.**

***Index Terms*—Design, reliability, verification.**

## NOMENCLATURE

| | |
|---|---|
| $x_1(x_2)$ | Input signal arrival time. |
| $x' = x_2 - x_1$ | Crosstalk aggressor signal alignment. |
| $D_{\rm g}$ | Driver gate delay. |
| $y_1$ | Output signal arrival time. |
| $\mu_1(\mu_2) = \mu_{x_1}(\mu_{x_2})$ | Mean of input signal arrival time. |
| $\sigma_1(\sigma_2) = \sigma_{x_1}(\sigma_{x_2})$ | Standard deviation of input signal arrival time. |
| $\mathrm{cov}(x_1, x_2)$ | Covariance of input signal arrival times. |
| $\mu'(\sigma') = \mu_{x'}(\sigma_{x'})$ | Mean (standard deviation) of crosstalk aggressor signal alignment. |
| $P(x)$ | Probability density function (pdf) of $x$. |
| $N(\mu, 3\sigma)$ | Normal distribution of mean $\mu$ and standard deviation $\sigma$. |

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## I. INTRODUCTION

Very large-scale-integration (VLSI) designs experience an increase of system performance variation due to the increased manufacturing and system runtime variabilities, including lithographic, chemical–mechanical-planarization process related, and dopant variations during manufacturing process, and supply voltage and temperature variations during system runtime. Consequently, the VLSI performance verification moves away from the traditional overpessimistic case analysis and explicitly addresses this increased variability. Statistical static timing analysis (SSTA) computes signal arrival time distributions at each pin (in block-based SSTA [1], [22]) or along each path (in path-based SSTA [14], [15]) and provides "timing yields" or probabilities for a chip to meet its timing requirements.

Statistical-timing-analysis accuracy has been significantly improved by including more variation sources into account. For example, a gate delay undergoes significant deviation when multiple inputs of the gate are switching at the same time. Neglecting this multiple-input switching effect could underestimate the mean delay of a gate by up to 20% and overestimate the standard deviation of a gate delay by up to 26% [2].

In this paper, we propose statistical timing analysis in the presence of signal-integrity effects, by taking into account an equally significant source of variation in statistical timing analysis, i.e., the effect of crosstalk aggressor signal alignment on signal propagation delay of a victim interconnect and its driver gate (Fig. 1). A crosstalk aggressor signal transition injects a noise into a victim net and causes the following: 1) interconnect-delay variation [6] and 2) driver gate-delay variation [19]. Such signal-integrity effects have been taken into consideration in traditional deterministic timing analysis, and they must also be taken into consideration in statistical timing analysis. This paper is the first in proposing an analytical statistical delay-calculation method which takes the signal-integrity effects into account.

We organize the rest of this paper as follows. We present the statistical timing analysis in the presence of signal integrity in Section I. We discuss runtime complexity, efficiency-improvement techniques, and other implementation issues in Section II. We present our experimental results in Section III, then conclude in Section IV.

## II. THEORY

### A. Problem Formulation

Several signal-integrity effects have significant impacts on signal propagation delay in a nanometer-scale VLSI design. In this paper, we take into account the effect of crosstalk aggressor signal alignment on the interconnect and gate delays in statistical timing analysis and consider the following problem.

***Problem 1:*** *Statistical Delay Calculation in the Presence of Signal-Integrity Effects:* Find the statistical signal arrival time variations at the output of the system given the following:

1) a system of coupled interconnects with their driver gates;
2) statistical signal arrival time variations at the inputs of the driver gates;

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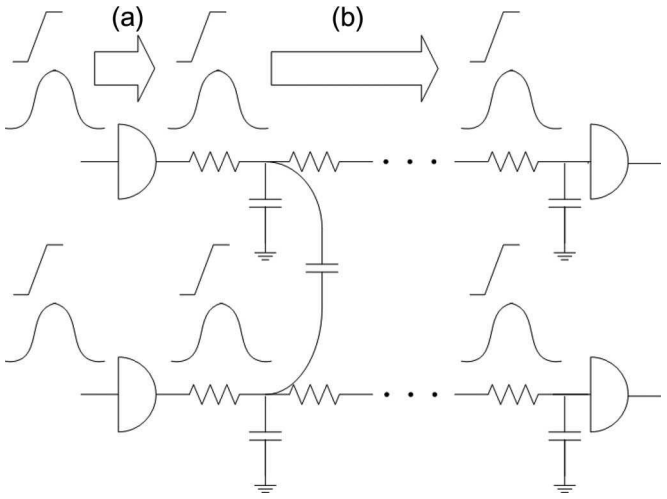


Fig. 1. Statistical timing analysis in the presence of crosstalk aggressor signal alignment effect needs to (a) compute the gate delays and the gate output signal arrival time distributions and (b) compute the interconnect delays and the interconnect output signal arrival time distributions.

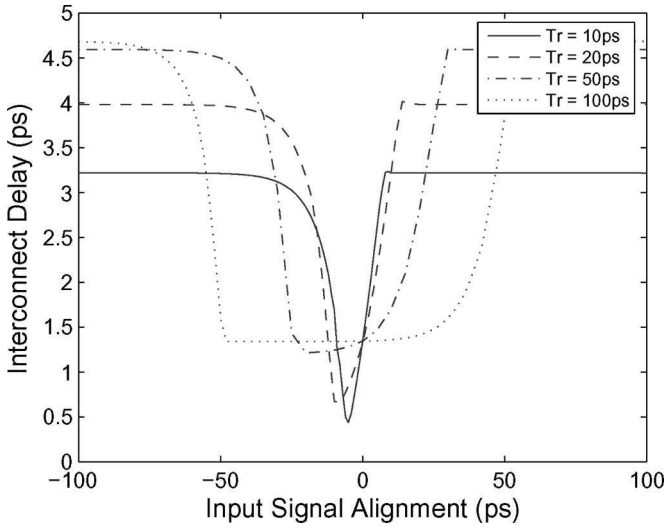


Fig. 2. Interconnect delay as a function of crosstalk aggressor signal alignment for a pair of 1000-$\mu$m-coupled global interconnects in Berkeley Predictive Technology Model (BPTM) 70-nm technology for 10-, 20-, 50-, and 100-ps input signal transition times, respectively.

3) statistical process parameter variations for the interconnects and their driver gates.

Algorithm 1 gives our proposed statistical timing analysis in the presence of signal-integrity effects. We present the details of each step as follows.

**Algorithm 1: Signal Integrity Aware Statistical Timing Analysis**

**Input:** Coupled interconnects in $R(L)C$ networks, input signal arrival time distributions, and other manufacturing/runtime variations

**Output:** Output signal arrival time distributions

1) Process variation extraction
2) Performance characterization
3) Probabilistic symbolic analysis
4) Statistical delay calculation in the presence of signal-integrity effects

### B. Process Variation Extraction

A signal arrival time in the nanometer-scale VLSI designs is affected by a number of correlated variational parameters, including interdie, intradie (location dependent), and purely random variations [12]. Such parameter variabilities can be extracted from a manufacturing process and reduced to a minimum set of uncorrelated standard Gaussian random variables by applying principle component analysis (PCA) [4], [12], [20]. A signal arrival time $x$ in a nanometer VLSI design can then be approximated in a polynomial function of such random variables [7] as follows:

$$x = f_i(r_1, r_2, \ldots)$$
$$P(r_i) = \frac{1}{\sqrt{2\pi}\sigma_{r_i}} e^{-\frac{(r_i-\mu_{r_i})^2}{2\sigma_{r_i}^2}}. \quad (1)$$

### C. Performance Characterization

To enable statistical propagation of signal arrival times across a coupled interconnect and its driver gate, we establish a functional relationship between an interconnect (its driver gate) delay and a crosstalk aggressor signal alignment. This is achieved by performing the deterministic delay calculation for a set of "sampled" crosstalk aggressor signal alignments and extracting a (piecewise polynomial) function based on the sampling data. Such a characterization method is common, e.g., in analog design analysis and optimization which is known as the "training" process to establish functional relationships among variables [21]. We apply SPICE simulation for the most accurate delay-calculation results, while the interconnect model order reduction [13] and the voltage-controlled current source-based gate modeling [5] techniques can be applied for an efficiency improvement without significant accuracy loss.

Fig. 2 shows an interconnect delay as a function of crosstalk aggressor signal alignment (similar is a gate delay). We observe that the effect of crosstalk aggressor signal alignment on an interconnect (driver gate) delay is more complex than the traditional timing-window model. A timing window is the time frame bounded by the earliest and the latest signal arrival times of a net. The traditional point of view states that crosstalk effect takes place in a timing window, i.e., the victim-net interconnect (driver gate) delay is a pulse function of the crosstalk aggressor signal alignment. Instead, we observe a more complex function, i.e., the crosstalk effect increases gradually as the crosstalk aggressor and victim signals are aligned to each other.

We apply (least mean-square) regression and approximate the victim-net interconnect (driver gate) delay as a piecewise quadratic function as follows (where $d_1 = d_2$ for the interconnect delay):

$$D_g = \begin{cases} d_2, & x' \le t_0 \\ a_0 + a_1 x' + a_2 x'^2, & t_0 \le x' \le t_1 \\ d_0, & t_1 \le x' \le t_2 \\ b_0 + b_1 x' + b_2 x'^2, & t_2 \le x' \le t_3 \\ d_1, & t_3 \le x' \end{cases}. \quad (2)$$

### D. Probabilistic Symbolic Analysis

Traditional statistical-timing-analysis approaches compute moments (e.g., means, standard deviations, skewnesses, etc.) and correlations of signal arrival times in a design. It is critical to include the correlations in these statistical-timing-analysis approaches to achieve meaningful and accurate estimation results. However, complexity arises in addressing an increasingly large degree of correlations, e.g., for $n$ random variables, $O(n^2)$ first-order correlations, and much more

higher order correlations are needed to compute the exact probabilities. Truncating higher order correlations gives accuracy-efficiency tradeoff.

Alternative to moments and correlation computation, signal arrival times in a design can be computed symbolically, e.g., in closed-form expressions of variational parameters, such that their probabilistic distributions are accessible by, e.g., Monte Carlo simulation without the need of correlation computation. Such techniques include polynomial computation [7], affine arithmetics [11], probabilistic interval analysis [17], etc., where variational delays are computed by either the derivation of closed-form formulas [11], [17] or by sampling analysis and regression [7]–[9]. We call these methods as the probabilistic symbolic analysis approaches.

Next, we present the closed-form formulas for statistical signal arrival time computation which takes constant time, giving an improved efficiency compared with the Monte Carlo simulation.

### *E. Statistical Delay Calculation in the Presence of Signal-Integrity Effects*

Given the input arrival timing variations in closed-form formulas of random variables and the functional relationship between the output and the input signal arrival times, we rewrite Problem 1 as follows.

***Problem 2:*** *PDF Propagation:* Find the probability density function (pdf) of $y_1$ given the following:

1) joint pdf of $k$ random variables $\vec{x} = \langle x_1, \ldots, x_k \rangle$;
2) a piecewise polynomial function $y_1 = f(\vec{x})$.

The output $y_1$ stands for the signal arrival time distribution at one of the outputs of the coupled interconnect system. The random variables $\vec{x}$ include variational process parameters, e.g., gate length and threshold voltage for the driver gates and interconnect widths and spacings for the load interconnects, and previous stage variations which give the input signal arrival time variations. The piecewise polynomial function combines the process variation extraction and the performance characterization results.

We partition the variable space of the function $y_1 = f(\vec{x})$ into regions $R_i \in \mathcal{R}$, in which, within each region, the output $y_1$ has a consistent polynomial representation $f_{R_i}$. We compute the conditional probabilities for the output $y_1$ for each region as follows:

$$\begin{aligned} P(y_1 = \tau) &= \sum_{R_i \in \mathcal{R}} \int_{\vec{x} \in R_i} P(\vec{x} | y_1 = \tau) d\vec{x} \\ &= \sum_{R_i \in \mathcal{R}} \int_{\vec{x} \in R_i} P(x_1) \cdot P(x_2 | x_1), \ldots \\ &\quad P\left(x_k = f_{R_i}^{-1}(y_1 = \tau, x_1, x_2, \ldots, x_{k-1})\right) \\ &\quad dx_1 dx_2, \ldots, dx_{k-1}. \end{aligned} \tag{3}$$

For each $y_1 = \tau$, its occurrence probability is given by the joint pdf $P(\vec{x})$ of $\vec{x}$ to satisfy $y_1 = f(\vec{x}) = \tau$. To guarantee $y_1 = \tau$, we perform integration on $k-1$ dimensions, while the last variable $x_k$ is given by the inverse function $x_k = f^{-1}(y_1, x_1, x_2, \ldots, x_{k-1})$. Such an analytical inverse function $x_k$ is available for any order-$d$ polynomial approximation, where $d \leq 4$.

For example [8], [9], considering a piecewise quadratic approximation (2) of an output signal arrival time of two coupled interconnects, the pdf of the output signal arrival time is given by

$$\begin{aligned} P(y_1) &= \int_{-\infty}^{\infty} P(x_1 = y_1 - D_g) P(D_g) dD_g \\ &= \int_{t_0}^{t_1} P(x_1 = y_1 - a_0 - a_1 x') P(x' | x_1) dx' \\ &\quad + \int_{t_2}^{t_3} P(x_1 = y_1 - b_0 - b_1 x') P(x' | x_1) dx' \\ &\quad + P(x_1 = y_1 - d_0) \int_{t_1}^{t_2} P(x' | x_1 = y_1 - d_0) dx' \\ &\quad + P(x_1 = y_1 - d_1) \left(1 - \int_{0}^{t_3} P(x' | x_1 = y_1 - d_1) dx'\right) \\ &\quad + P(x_1 = y_1 - d_2) \int_{0}^{t_0} P(x' | x_1 = y_1 - d_2) dx'. \end{aligned} \tag{4}$$

For the input signal arrival times in the uncorrelated Gaussian distributions (i.e., in the linear representation of uncorrelated Gaussian random variables), the crosstalk aggressor signal alignment $x' = x_2 - x_1$ is also in a Gaussian distribution:

$$\begin{aligned} P(x_1) &= \frac{1}{\sqrt{2\pi}\sigma_1} e^{-\frac{(x_1 - \mu_1)^2}{2\sigma_1^2}} \\ P(x_2) &= \frac{1}{\sqrt{2\pi}\sigma_2} e^{-\frac{(x_2 - \mu_2)^2}{2\sigma_2^2}} \\ P(x') &= P(x_2 - x_1) \\ &= \frac{1}{\sqrt{2\pi}\sigma'} e^{-\frac{(x' - \mu')^2}{2\sigma'^2}} \end{aligned} \tag{5}$$

where

$$\begin{aligned} \mu' &= \mu_2 - \mu_1 \\ \sigma'^2 &= \sigma_1^2 + \sigma_2^2 + 2\mathrm{cov}(x_1, x_2). \end{aligned}$$

The conditional probability distributions of the input signal alignment $x'$ for each input signal arrival time $x_1$ have different means, but the same variance

$$\begin{aligned} \mu_{x'|x_1} &= \mu_{x_2} - x_1 \\ \sigma_{x'|x_1} &= \sigma_{x'}. \end{aligned}$$

Substituting the pdfs $P(x_1)$ and $P(x'|x_1)$ in (5) to (4) gives

$$\begin{aligned} P(y_1) &= \frac{1}{\sqrt{2\pi}\sigma_{ya}} e^{-\frac{(y_1 - \mu_{ya})^2}{2\sigma_{ya}^2}} \\ &\quad \times \frac{1}{2} \left(F(y_1, t_1, a_0, a_1, \sigma_{ya}) - F(y_1, t_0, a_0, a_1, \sigma_{ya})\right) \\ &\quad + \frac{1}{\sqrt{2\pi}\sigma_{yb}} e^{-\frac{(y_1 - \mu_{yb})^2}{2\sigma_{yb}^2}} \\ &\quad \times \frac{1}{2} \left(F(y_1, t_3, b_0, b_1, \sigma_{yb}) - F(y_1, t_2, b_0, b_1, \sigma_{yb})\right) \\ &\quad + \frac{1}{2} P(x_1 = y_1 - d_0) \left(\mathrm{erf}\left(\frac{t_2 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}\right) \right. \\ &\qquad \left. - \mathrm{erf}\left(\frac{t_1 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}\right)\right) \\ &\quad + \frac{1}{2} P(x_1 = y_1 - d_1) \left(2 - \mathrm{erf}\left(\frac{t_3 - \mu_2 + y_1 - d_1}{\sqrt{2}\sigma'}\right)\right) \\ &\quad + \frac{1}{2} P(x_1 = y_1 - d_2) \left(\mathrm{erf}\left(\frac{t_0 - \mu_2 + y_1 - d_2}{\sqrt{2}\sigma'}\right)\right. \end{aligned} \tag{6}$$

where

$$F(y,t,k_0,k_1,\sigma_{yk}) = \mathrm{erf}\Bigg(\frac{1}{\sqrt{2}\sigma'\sigma_1\sigma_{yk}} \times \left(t\sigma_{yk}^2 - (1-k_1)(k_0+\mu_2-y)\sigma_1^2 + k_1(k_0+\mu_1-y)\sigma'^2\right)\Bigg)$$

$$\mu_{ya} = \mu_1 + a_0 - a_1(\mu_1-\mu_2)$$
$$\sigma_{ya} = \sqrt{(1-a_1)^2\sigma_1^2 + a_1^2\sigma'^2}$$
$$\mu_{yb} = \mu_1 + b_0 - b_1(\mu_1-\mu_2)$$
$$\sigma_{yb} = \sqrt{(1-b_1)^2\sigma_1^2 + b_1^2\sigma'^2}.$$

From here, we can do the following: 1) compute the moments of the output signal arrival time and the correlations between the output signal arrival time and the other signal arrival times or 2) apply symbolic analysis and proceed to the next stage of the circuit.

## III. Implementation

Our proposed method takes $O(N)$ time for the performance characterization for the $N$ sampled crosstalk alignment configurations. For each crosstalk alignment sample, we compute the output signal arrival time by either SPICE simulation or gate modeling and the interconnect model order reduction-based delay-calculation techniques [13]. Regression takes $O(N)$ time. Statistical delay calculation for the coupled interconnect system takes constant time once the closed-form formulas are present.

Given the process variation extraction results, the overall runtime is dominated by the number of crosstalk alignment configurations in performance characterization, which is given by $N = O(\prod_{i=n} m_i)(N = O(\sum_{i=n} m_i))$ for $n$ crosstalk aggressors, each with $m_i$ sampling alignments, when additivity cannot (can) be applied. For each crosstalk aggressor, the number of sampling alignments $m_i = \mathrm{MIN}(t_3 - t_0, 6\sigma')/l$ is given by the smaller: 1) $t_3 - t_0$ the time frame within which an aggressor signal transition makes a difference on the victim-net driver gate delay and 2) the $6\sigma'$s of the crosstalk alignment (which can be based on the input signal "timing windows"), for a given time step $l$ between the sampling crosstalk alignments.

We achieve an improved efficiency by applying PCA to reduce the random variables to a minimum set of uncorrelated random variables. Having the uncorrelated random variables significantly simplifies statistical computation. Of the uncorrelated random variables $\vec{x}$, the joint pdf is given by the product of each individual random variable's pdf $P(\vec{x}) = \prod_i P(x_i)$, and the sum of uncorrelated random variables $\vec{x}$ has its mean and variance given by $\mu_{\sum_i x_i} = \sum_i \mu_i$ and $\sigma^2_{\sum_i x_i} = \sum_i \sigma_i^2$, respectively.

We also improve efficiency by applying superposition for the effects of different variation sources on the interconnect-delay variation, due to the linearity of an $R(L)C$ interconnect. For the gate-delay variations to which superposition finds limited application, we can leverage with the existing characterization and data-mining techniques, e.g., adaptive regression which prioritizes the sampling space [10].

Our proposed statistical delay calculation in the presence of signal-integrity effects can be implemented in a statistical timing analyzer, which goes through an iteration of pessimism reduction and estimation refinement, as is in the traditional deterministic STA in the presence of signal-integrity effects. A pessimistic distribution can be assumed initially and refined later during the iteration.

## IV. Experiments

We have applied our method in [8] and [9] to a variety of input signal transition times ranging from 10, 20, 50, to 100 ps and input signal alignment ranging from 50, 100, to 200 ps. To cover the different technology nodes, our test cases include 16× inverters which drive the following: 1) a pair of 1000-$\mu$m-coupled global interconnects in 70-nm technology given by BPTM [3] and 2) a pair of coupled interconnects which are extracted from a 130-nm industry design with 451 resistors and 1637 ground and coupling capacitors.

We sample the crosstalk aggressor signal alignment for every 2 ps and apply the SPICE simulation for the functional relationship between the interconnect (gate) delay and the crosstalk aggressor signal alignment. The SPICE outputs (Fig. 2 and similar figures for gate delay) verify the accuracy of our proposed piecewise-quadratic approximation.

In [8] and [9], we have compared the proposed statistical-timing-analysis technique in the presence of signal-integrity effects with 1000 SPICE Monte Carlo simulation runs for the interconnect (driver gate) delay and the output signal arrival time variations. We include the crosstalk aggressor signal alignment variation in a Gaussian distribution of 10-, 50-, 100-, or 200-ps standard deviation and −10-, 0-, or 10-ps mean. We bring into account the effects of manufacturing process variations on the interconnect and gate-delay variations, such effects differ with different crosstalk aggressor signal alignments. As an example, we assume a 100% width correlation among local wire segments [16] and compute the interconnect resistances and capacitances using the closed-form formulas [3] for normally distributed wire widths in the SPICE Monte Carlo simulation. We consider a gate-length variation in a normal distribution of which $3\sigma$ is 15% of the minimum gate length [2].

We compare with the statistical driver gate delay calculation without statistical crosstalk consideration, in which case, the best practice is to assume a unit Miller factor by grounding all coupling capacitors. We observe that, without statistical crosstalk consideration, assuming a unit Miller factor results in up to 159.4% (114.65%) mismatch in mean driver gate delay and up to 147.4% (71.26%) underestimate in the standard deviation of driver gate (interconnect) delay [8], [9].

We also observe that over a variety of technology nodes, input signal transition times and arrival time deviations, our method gives the means and the standard deviations of the gate (interconnect) output signal arrival times within 2.57% (2.09%) and 3.86% (3.38%) of SPICE Monte Carlo simulation results, respectively [8], [9].

## V. Conclusion

We propose a statistical timing analysis in the presence of signal-integrity effects. We study the interconnect and gate-delay variations that are induced by crosstalk aggressor signal alignment, i.e., signal arrival time difference at coupled interconnects. This is a significant source of variation, which must be taken into consideration in the statistical timing analysis. We present the closed-form formulas for the probabilistic gate delay calculation based on the deterministic delay calculation for sampling crosstalk alignment configurations. After sampling delay calculation, the probabilistic delay calculation and updating take constant time. Experimental results reported in [8] and [9] based on the 1000-$\mu$m global interconnect structures in BPTM 70-nm technology and industry designs in 130-nm technology verify

our method. These results show within 1.28% (3.38%) mismatch for the interconnect output signal arrival time means (standard variations) and within 2.57% (3.86%) mismatch for the gate output signal arrival time means (standard variations) compared with the SPICE Monte Carlo simulation results. On the other hand, lack of statistical crosstalk alignment consideration could lead up to 114.65% (71.26%) differences in interconnect-delay means (standard deviations) and up to 159.4% (147.4%) differences in gate-delay means (standard variations), respectively.

## REFERENCES


[1] A. Agarwal, D. Blaauw, V. Zolotov, and S. Vrudhula, "Statistical timing analysis using bounds," in *Proc. Des. Autom. Test Eur.*, 2003, pp. 62–68.

[2] A. Agarwal, F. Dartu, and D. Blaauw, "Statistical gate delay model considering multiple input switching," in *Proc. Des. Autom. Conf.*, 2004, pp. 658–663.

[3] *Berkeley Predictive Technology Model*. [Online]. Available: http://www-device.eecs.berkeley.edu/~ptm/

[4] H. Chang and S. S. Sapatnekar, "Statistical timing analysis considering spatial correlations using a single PERT-like traversal," in *Proc. Int. Conf. Comput.-Aided Des.*, 2003, pp. 621–625.

[5] J. F. Croix and D. F. Wang, "Blade and razor: Cell and interconnect delay analysis using current-based models," in *Proc. Des. Autom. Conf.*, 2004, pp. 386–389.

[6] P. D. Gross, R. Arunachalam, K. Rajagopal, and L. T. Pileggi, "Determination of worst-case aggressor alignment for delay calculation," in *Proc. Int. Conf. Comput.-Aided Des.*, 1998, pp. 212–219.

[7] V. Khandelwal and A. Srivastava, "A general framework for accurate statistical timing analysis considering correlations," in *Proc. Des. Autom. Conf.*, 2005, pp. 89–94.

[8] A. B. Kahng, B. Liu, and X. Xu, "Statistical gate delay calculation with crosstalk alignment consideration'," in *Proc. Great Lakes Symp. VLSI*, 2006, pp. 223–228.

[9] A. B. Kahng, B. Liu, and X. Xu, "Statistical crosstalk aggressor alignment aware interconnect delay calculation," in *Proc. Syst. Level Interconnect Prediction*, 2006, pp. 91–97.

[10] H. Liu, A. Singhee, R. A. Rutenbar, and L. R. Carkey, "Remembrance of circuits past: Macromodeling by data mining in large analog design spaces," in *Proc. Des. Autom. Conf.*, 2002, pp. 437–442.

[11] J. D. Ma and R. A. Rutenbar, "Interval-valued reduced order statistical interconnect modeling," in *Proc. Int. Conf. Comput.-Aided Des.*, 2004, pp. 460–467.

[12] F. N. Najm and N. Menezes, "Statistical timing analysis based on a timing yield model," in *Proc. Des. Autom. Conf.*, 2004, pp. 460–465.

[13] A. Odabasioglu, M. Celik, and L. T. Pileggi, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 17, no. 8, pp. 645–654, Aug. 1998.

[14] M. Orshansky and A. Bandyopadhyay, "Fast statistical timing analysis handling arbitrary delay correlations," in *Proc. Des. Autom. Conf.*, 2004, pp. 337–342.

[15] M. Orshansky and K. Keutzer, "A general probabilistic framework for worst case timing analysis," in *Proc. Des. Autom. Conf.*, 2002, pp. 556–561.

[16] M. Orshansky, L. Milor, P. Chen, K. Keutzer, and C. Hu, "Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 5, pp. 544–553, May 2002.

[17] M. Orshansky, W.-S. Wang, G. Xiang, and V. Kreinovich, "Interval-based robust statistical techniques for non-negative convex functions with applications to timing analysis of computer chips," in *Proc. Reliable Eng. Comput.*, 2006, pp. 1645–1649.

[18] D. Sinha and H. Zhou, "A unified framework for statistical timing analysis with coupling and multiple input switching," in *Proc. Int. Conf. Comput.-Aided Des.*, 2005, pp. 837–843.

[19] S. Sirichotiyakul, D. Blaauw, C. Oh, R. Levy, V. Zolotov, and J. Zuo, "Driver modeling and alignment for worst-case delay noise," in *Proc. Des. Autom. Conf.*, 2001, pp. 720–725.

[20] M. S. Srivastava, *Methods of Multivariate Statistics*. New York: Wiley-Interscience, 2002.

[21] S. K. Tiwary and R. A. Rutenbar, "Scalable trajectory methods for on-demand analog macromodel extraction," in *Proc. Des. Autom. Conf.*, 2005, pp. 403–408.

[22] C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, and S. Narayan, "First-order incremental block-based statistical timing analysis," in *Proc. Des. Autom. Conf.*, 2004, pp. 331–336.


# Minimization of Linear Dependencies Through the Use of Phase Shifters

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***Abstract*—Two-dimensional scan design with a linear test pattern generator is a practical built-in self-test technique, but it suffers from linear dependencies, which reduce the fault coverage. To alleviate this problem, networks of XOR gates known as phase shifters can be employed. Current techniques based on the empirical criterion of imposing large phase shift differences (channel separations) between successive scan chains cannot adequately remove the dependencies. In this paper, we present a method that addresses explicitly the minimization of linear dependencies through appropriate selection of phase shift values. The method is based on the criterion of minimizing the linear dependencies in each cone of the circuit under test, and is applicable to any type of linear test pattern generator, be it linear feedback shift register of the external-XOR or internal-XOR type, cellular automaton, etc. Experimental results demonstrate the effect of the approach in increasing fault coverage.**

***Index Terms*—Built-in self-test (BIST), cellular automata (CA), linear dependencies, linear feedback shift register (LFSR), linear finite state machine (LFSM), phase shifters, 2-D scan designs.**

## I. INTRODUCTION

Any built-in self-test (BIST) architecture (see, e.g., [1], [2], [5], [7], [13]) has to provide high fault coverage, high testability, and short testing times. Two-dimensional scan design can be used to achieve these objectives. In these designs (exemplified by the STUMPS architecture [2]), a linear finite state machine (LFSM), such as linear feedback shift registers (LFSRs) of the external-XOR or internal-XOR type and cellular automata (CA), is usually used as an on-chip test pattern generator, which drives chains of scanned flip-flops (scan chains or "channels") in parallel (2-D scan). The scanned flip-flops (scan cells) serve as test-phase inputs and apply the test bits received from the LFSM to the circuit under test (CUT). They also serve as test-phase outputs and receive the response of the CUT subcircuit that drives them. In this way, the CUT is, in effect, partitioned into overlapping single-output multiple-input subcircuits referred to as cones. The set of the cone inputs will be referred to as the cone-set.

Let $m$ be the maximum size of the cone-sets in the CUT. In general, a number of $2^\tau < 2^m$ of random patterns are applied, where the value of $\tau$ is chosen such that a desired level of fault coverage is obtained. [The case of using $2^\tau = 2^m$ patterns, known as pseudoexhaustive test, is only feasible when $m$ has been made sufficiently small by circuit modification (see, e.g., [1], [8]). In this paper, we do not assume any circuit modification and do not deal with this case.] However, regardless of the type of the LFSM used as test pattern generator, linear dependencies ([3], [6], [14], [15], [17], [18]) that are present among

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