Detailed Placement for Enhanced Control of Resist and Etch CDs

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***Abstract*—Subresolution assist feature (SRAF) and etch-dummy insertion techniques have been absolutely essential for process window enhancement and CD control in photo and etch processes. However, as focus levels change during lithography manufacturing, CDs at a given "legal" pitch can fail to achieve manufacturing tolerances. Placed standard-cell layouts may not have the ideal whitespace distribution to allow for an optimal assist-feature insertion. This paper first describes a novel dynamic programming-based technique for Assist-Feature Correctness (AFCorr) in detailed placement of standard-cell designs. At the same time, etch-dummy features are used in the mask data preparation flow to reduce CD skew between resist and etch processes and to improve the printability of layouts. However, etch-dummy rules conflict with the SRAF insertion because each of the two techniques requires specific design rules. We further present a novel SRAF-aware etch-dummy insertion method (SAEDM) which optimizes the etch-dummy insertion to make the layout more conducive to the assist-feature insertion after the etch-dummy features have been inserted. Since placement of cells can create forbidden-pitch violations of resist process and can increase etch skew, the placer must also generate etch-dummy-correct placement. This can be solved by Etch-dummy Correctness (EtchCorr), which is an intelligent whitespace management for etch-dummy-corrected placement, an extension of the AFCorr methodology. These methods for enhanced resist and etch CD control are validated on industrial test cases with respect to wafer printability, database complexity, and device performance. For benchmark designs, we validate the four methodologies: 1) AFCorr; 2) SAEDM; 3) AFCorr + SAEDM; and 4) AFCorr + EtchCorr + SAEDM. The AFCorr placement perturbation achieves a significant reduction in forbidden pitches between polysilicon shapes. Using 1) flow, forbidden-pitch count of photo process is reduced by 76%–100% for 130 nm and by 87%–100% for 90 nm. Our novel Corr design-perturbation technique, which combines the AFCorr and EtchCorr methods, facilitates additional SRAF and etch-dummy insertions and, thus, reduces the CD skew between the photo and etch processes. After Corr with SAEDM, edge placement error (EPE) count is also reduced by 91%–100% in the resist CD and by 72%–98% in the etch CD. Our methods provide a substantial improvement in CD control with negligible timing, area, and CPU overhead. The advantages of such correctness methods are expected to increase in future technology nodes.**

***Index Terms*—Defocus, etch, lithography, placement, subresolution assist feature (SRAF).**

I. Introduction

ACROSS-CHIP linewidth variation induced by photolithography and etch processes has been a major barrier in ultradeep submicrometer manufacturing. Photolithography has been a key enabler of the aggressive IC technology scaling implicit in Moore's Law. Minimum feature sizes have outpaced the introduction of advanced lithography hardware solutions so that gate length and CD tolerances prescribed in the 2005 International Technology Roadmap for Semiconductors [2] are extremely difficult to achieve. As a result, resolution-enhancement techniques (RETs), such as optical proximity correction (OPC) [19], phase-shift masks [13], and off-axis illumination (OAI), are being pushed ever closer to fundamental resolution limits [6]. Combinations of these techniques can provide advantages for lithography manufacturing, e.g., OAI and OPC, together with subresolution assist features (SRAFs), achieve enhanced CD control, and focus margin at minimum pitch.

However, when OAI is used, there will always be pitches for which the angle of illumination works with the angle of diffraction to produce a bad distribution of diffraction orders in the lens. These pitches are called the forbidden pitches because of their lower printability, and designers should avoid such pitches in the layout. Forbidden pitches consist of horizontal (H) and vertical (V) forbidden pitches, depending on whether they are caused by interactions of poly geometries in the same cell row or in different cell rows, respectively. The resulting forbidden-pitch problem for the manufacturing-critical poly layer must be solved before detailed routing. Since the detailed routing works on a fixed placement, except on some small placement ECOs as required, it "locks in" the poly-layer layout. At the same time, we wish to address the forbidden-pitch problem as late as possible to avoid extra rework upon modification of the manufacturing recipe. We first describe a novel dynamic-programming-based algorithm for Assist-Feature Correctness (AFCorr), which uses flexibility in detailed placement to avoid all possible H and V forbidden pitches and the manufacturing uncertainty that they cause.

Etch-dummy features are introduced into the layout to reduce the CD distortion induced by etch proximity. The etch dummies are placed outside of the active layers so that the leftmost

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and rightmost gates on active-layer regions are protected from ion scattering during the etch process. However, etch-dummy rules conflict with the SRAF insertion because each of the two techniques requires specific spacings from poly. In such a regime, the assist-feature-correct placement methodology must consider the assist-feature and etch-dummy corrections. In this paper, we also present a novel SRAF-aware etch-dummy insertion method (SAEDM) which applies flexible etch-dummy rules according to the distance from the active edge to the leftmost (or rightmost) poly. As a result, the layout will be more conducive to the assist-feature insertion after the etch-dummy features have been inserted. Finally, we introduce a dynamic programming-based technique for Etch-dummy Correctness (EtchCorr) which can be combined with the SAEDM in detailed placement of standard-cell designs.

A. Contributions of This Paper

In this paper, we present various analyses of lithographic printability within the context of the standard-cell-based design methodology. Our goal is to minimize CD variation and enhance feature printability and reliability. Our main contributions are as follows.

1) We propose a novel post-detailed placement perturbation algorithm for AFCorr. The dynamic programming-based algorithm of AFCorr reduces the incidence of the forbidden pitches by calculating H and V perturbation costs and by finding an optimal perturbation of cell placements in a given row, subject to upper bounds on cell displacement. In particular, in conjunction with the intelligent process-aware library layout, this technique can achieve substantial improvements in depth-of-focus (DOF) margin and CD control.
2) We present a SAEDM which optimizes etch-dummy insertion to make the layout more conducive to the assist-feature insertion after the etch-dummy features have been inserted.
3) We describe the Corr post-detailed placement perturbation algorithm that combines the EtchCorr and AFCorr techniques, removes the forbidden pitches of resist CD, and reduces the skew between resist and etch CDs, all of which being done simultaneously. We test this method within a complete industrial flow and achieve up to 100% reduction in the number of cell border-poly geometries having forbidden-pitch violations.
4) Various techniques that combine AFCorr, SAEDM, and EtchCorr are validated with respect to wafer printability, database complexity, and device performance. The penalties in data size, OPC running time, and delay are within 3%, 4%, and 6%, respectively, which are negligible compared to the large printability improvements and to the inherent "noise" in the relevant place-and-route tools.

B. Organization of This Paper

The remainder of this paper is organized as follows. In Section II, we review RET and its layout impact, focusing our discussion on strong OAI and OPC with SRAF. We then introduce a novel placement-perturbation technique for AFCorr. Evaluation flows to validate its impact on lithographic manufacturability and experimental results are described. In Section III, we describe the etch-dummy-insertion problems and the design-perturbation algorithms of SAEDM and EtchCorr for better etch-dummy insertion. Various techniques that combine AFCorr, SAEDM, and EtchCorr are evaluated with respect to printability and design metrics. We conclude in Section IV with directions for ongoing research.

II. Assist-Feature Correctness

A. RET and Layout Impact

The extension of optical lithography beyond the quarter-micrometer regime has been enabled by a number of RETs. These RETs address the available three degrees of freedom in lithography, namely, aperture, phase, and/or pattern uniformity [16]. However, the adoption of different RETs dictates certain tradeoffs with various aspects of process and performance [3].

The OAI brings light to the mask at an oblique angle. As the angle of diffraction through certain aperture shapes matches a given pitch, higher order pattern information can be projected on the pupil plane as determined by the numerical aperture (NA) of the illumination system. This technique enables certain pitches on the mask to obtain higher resolution and extended focus margin. However, other pitches beyond the optimum angle will have a lower process margin compared with the conventional illumination (i.e., with a circular aperture). Since strong OAI is an essential technique in current lithography, these other pitches should be forbidden, and their avoidance is a new challenge for physical design automation. OPC is the deliberate and proactive distortion of photomask shapes to compensate for systematic and stable patterning inaccuracies. Bias OPC, the most common and straightforward application of OPC, has been proven to be a useful technique for matching photoresist edges to layout edges with essentially a layout sizing technique. However, bias OPC has limitations in enhancing process margins with respect to DOF and exposure dose. The Bossung plot[1] in Fig. 1 shows that the bias OPC is not sufficient to reduce the CD difference between isolated and dense patterns with varying focus and exposure dose. The CD distortion in the isolated pattern is usually a problem since lithography and RET recipes are not tuned or optimized for isolated lines [14]. The SRAF OPC technique combines pattern biasing with assist-feature insertion to compensate for the deficiencies of bias OPC. SRAFs [or scattering bars (SBs)], which are extremely narrow lines that do not actually print on the wafer, modify the wavefront and allow the lens pupil to receive higher order pattern information. The SRAFs are placed adjacent to primary patterns such that a relatively isolated primary line behaves more like a dense line. This works well for bringing the lithographic performance of the isolated and dense

[1]The Bossung plot shows multiple CDs versus defocus curves at different exposure doses and has been a useful tool to evaluate lithographic manufacturability. The common process window between the dense and isolated patterns is an increasingly important requirement to maintain CD tolerances in the subwavelength lithography regime.

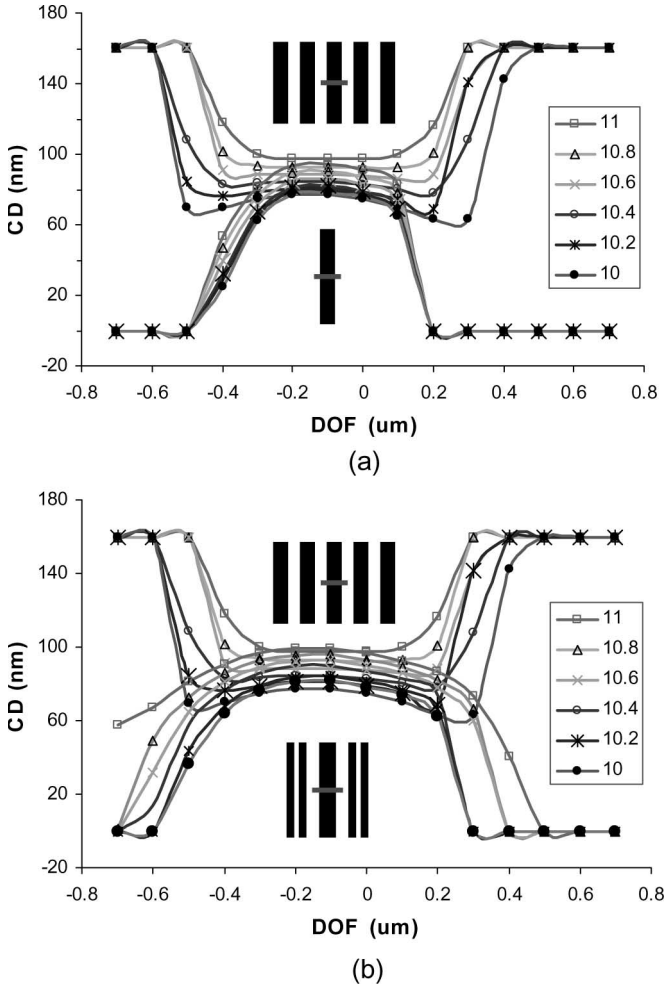

Fig. 1. Comparison of Bossung plots between the dense and isolated lines. (a) Results of bias OPC. (b) Results of SRAF OPC.

lines into agreement. The DOF margin of the isolated line, as shown in Fig. 1(b), is considerably improved from that shown in Fig. 1(a), and a larger overlap of process window[2] between the dense and isolated lines is achieved.

The key observation is that the SRAF technique places more constraints on the spacing between patterns. The SRAFs can be added whenever a poly line is sufficiently isolated, but certain minimum assist-to-poly and assist-to-assist spacings are required to prevent SRAFs from printing in the space [12]. We now briefly review previous works related to forbidden pitches and their design implications. Socha *et al.* [18] observe that under more aggressive illumination schemes such as annular and quasar illuminations, some optical phenomena become more prominent, most notably the forbidden-pitch phenomenon. Shi *et al.* [17] give a theoretical analysis of pattern distortion in forbidden pitches due to the destructive light-field interference. Although SRAFs are an effective method to collect high-order diffraction on the entrance pupil plane of a projection lens [15], Shi *et al.* report that incorrect SRAF placements around a given main feature can actually degrade the process latitude of that feature. A number of previous works have proposed techniques

[2]Process window is defined as the range of exposure dose and defocus within which acceptable CD tolerance is maintained.

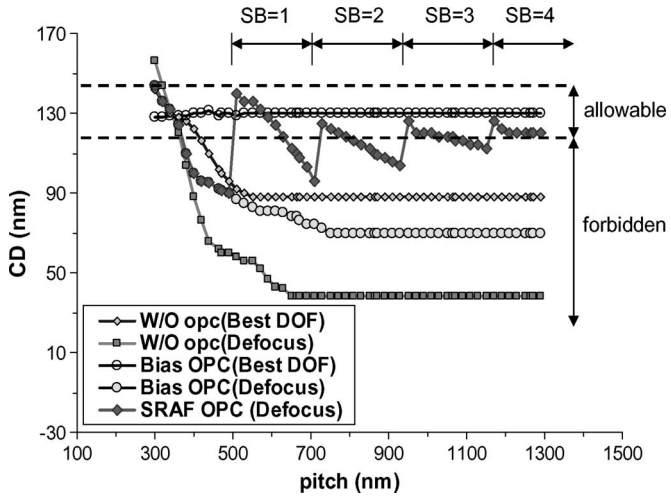

Fig. 2. Through pitch proximity plots for 130 nm technology: Best focus without OPC, worst defocus without OPC, worst defocus with BIAS OPC, and worst defocus with SRAF OPC are shown.

to control the forbidden pitches using optimization of optical conditions such as NA and illuminator aperture shape of OAI [11], [20], [21]. All of these works using optimizations of NA and OAI have sought to enlarge the ranges of allowable pitches, as shown in Fig. 2. However, approaches with process optimizations cannot completely remove the forbidden pitches, i.e., forbidden pitch always exists at any process conditions.

B. SRAF Rule and Forbidden-Pitch Extraction

Lack of space may prohibit insertion of a sufficient number of SRAFs, and as a result, patterns may violate CD tolerance through defocus. Forbidden pitches are pitch values for which the tolerance of a given target CD is violated. Allowable pitches are all pitches other than the forbidden pitches. In this section, we summarize the criteria for SRAF insertion and forbidden-pitch extraction considering a worst defocus model. Our SRAF insertion rule is initially generated based on the theoretical background given in [17]. Positioning of SRAFs is then adjusted based on OPC results. Large CD degradation through pitch increases pattern bias as model-based OPC is applied, and this requires trimming of the SRAF rule to guarantee a better process margin and prevent the SRAFs from printing.[3] After applying SRAF OPC to test patterns with the best focus model, OPCed pitch patterns are simulated with the worst defocus model which will be described in detail in Section II-D. This evaluation yields the forbidden pitches, considering a maximum printability and manufacturability. The forbidden pitch rule is determined based on CD tolerance and worst defocus level, which are, in turn, dependent on the requirements of device performance and yield. The SRAF OPC restores printing when there is enough room for one SB. However, larger pitches are forbidden until there is enough room for two SBs. We thus can extract a set of forbidden pitches which will be demonstrated

[3]More complicated approaches to SRAF rule generation may involve cooptimization of model-based OPC and SRAF insertion. We do not address such involved optimizations of OPC since the focus of this paper is OPC-aware design and not OPC itself.

TABLE I
SRAF RULE TABLE IN 130 nm AND 90 nm LITHOGRAPHY

	130 nm Lithography		90 nm Lithography	
	Pitch(X : μm)	Slope	Pitch(X : μm)	Slope
#SRAF = 0	$0 \le X <$ 0:51	0:28	$0 \le X <$ 0:41	0:162
#SRAF = 1	0:51 $\le X <$ 0:73	0:22	0:41 $\le X <$ 0:57	0:075
#SRAF = 2	0:73 $\le X <$ 0:95	0:105	0:57 $\le X <$ 0:73	0:062
#SRAF = 3	0:95 $\le X <$ 1:17	0:07	0:73 $\le X <$ 0:89	0:050
#SRAF = 4	1:17 $\le X$	0:02	0:89 $\le X$	0:012

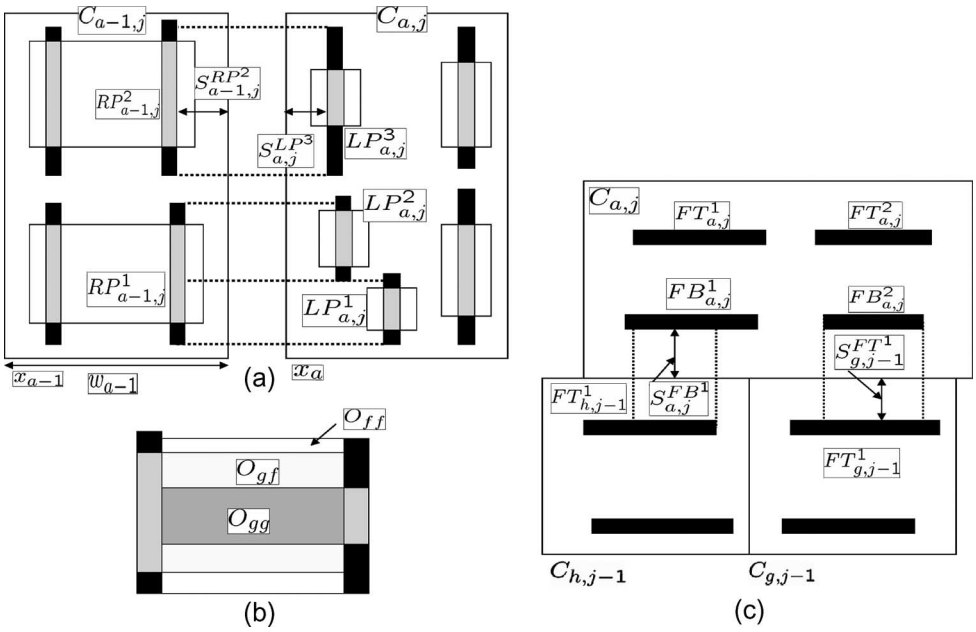

Fig. 3. (a) H interactions of gate-to-gate, gate-to-field, and field-to-gate polys. (b) Overlapped area in the region A of (a). (c) V interactions of field-to-field polys.

in Section II-D. In all of the works we report here, the CD tolerance is assumed to be $\pm 10\%$ of minimum linewidth, whereas the worst defocus levels are assumed to be 0.5 μm and 0.4 μm for the 130 nm and 90 nm technology nodes, respectively. All of these results are summarized in Table I.

C. AFCorr Placement Algorithm

In this section, we describe the proposed AFCorr placement-perturbation algorithm for assist-feature correction. Single orientation polysilicon geometries are becoming common for the current and future process generations. We consider the H forbidden pitches within a cell row and the V forbidden pitches between adjacent cell rows [7], [8]. In this paper, we treat the placement of a given cell row independently of all other rows, even though the cost function is calculated with respect to both the H and V perturbations, in order to avoid all forbidden pitches. Assuming that the spacings within the cell are assist-correct, then the only source of incorrect spacings between poly shapes for the assist-feature insertion is cell placement. Adjacent cells within the same standard cell row, as well as cells within the adjacent cell rows that have shapes overlapping, interact for this purpose. The vertical poly shapes (typically gates) at the left and right peripheries of a cell, which overlap with similar shapes in the neighboring cells in the row, constitute the horizontal interaction. Similarly, horizontal poly shapes (typically field) at the top and bottom peripheries of the cell that overlap with the similar shapes in vertically adjacent cells (in adjacent rows) constitute the vertical interaction. In the following, we describe the single-row AFCorr perturbation algorithm, using which the 2-D AFCorr problem is solved one cell row at a time.

Let $C_{a,j}$ be a cell at the a^{th} location in the j^{th} row. To explain the interactions of border-poly geometries, we adopt the following notations.

1) Horizontal polygon interaction: Given a cell $C_{a,j}$, let $\text{LP}_{a,j}$ and $\text{RP}_{a,j}$ be the sets of valid poly geometries in the cell, which are located closest to the left and right outlines of the cell, respectively. Only geometries with length that is larger than the minimum allowable length of SRAF features are considered. Define $s^{\text{LP}^i}_{a,j}$ to be the space between the left outline of the cell and the ith left border-poly geometry. O_{gg}, O_{ff}, and O_{gf} correspond to the length of overlapped area in the cases of gate-to-gate, field-to-field, and gate-to-field polys, as shown in Fig. 3. In addition, c_{gg}, c_{ff}, and c_{gf} are the proportionality factors which specify the relative importance of printability for gate and field polys.[4] Typically, gate poly geometries need to be better controlled through process as they have more direct impact on performance. Therefore, a typical order of importance is $c_{\text{gg}} \ge c_{\text{fg}} \ge c_{\text{ff}}$.

[4]Gate is the overlap region of polysilicon and diffusion. Field poly represents the rest area of polysilicon except for the gate.

2) Vertical polygon interaction: Given a cell $C_{a,j}$, let $\mathrm{FB}_{a,j}$ and $\mathrm{FT}_{a,j}$ be the sets of valid field poly geometries in the cell, which are located closest to the bottom and top outlines of the cell, respectively. Define $s_{a,j}^{\mathrm{FB}^i}(s_{a,j}^{\mathrm{FT}^i})$ to be the space between the bottom (and top) outline of the cell and the ith bottom (and top) border-poly geometry. O_{ff} corresponds to the length of field-to-field overlap between the horizontal geometries in adjacent cell rows.[5]

Assume an ordered set $\mathrm{AF} = \mathrm{AF}_1, \ldots, \mathrm{AF}_m$ of spacings which are "assist-correct," i.e., if the spacing between the two gate poly shapes belongs to the set AF, then the required number of assist features can be inserted between the two poly geometries. For example, in Fig. 2, the peaks of the CD correspond to AF_i. The acceptable CD tolerance range (e.g., 10%) results in a range of acceptable pitches starting at AF_i. AF is assumed to be sorted in increasing order. Note that the set AF may contain a number of spacings which correspond to varying SRAF widths. Let w_a denote the width of cell $C_{a,j}$, and let x_a denote its (leftmost) placement coordinate in the given standard cell row, where coordinates increase from left to right. In addition, let $\delta_{a,j}$ denote the placement perturbation of cell $C_{a,j}$ to adjust the spacing between cells. $\delta_{a,j}$ is positive if the cell is moved toward the right and negative otherwise. Then, the **assist-correct placement perturbation problem** is

$$\begin{aligned}
&\text{Minimize} \quad \sum |\delta_{a,j}| \\
&\delta_{a,j} + x_{a,j} - x_{a-1,j} - \delta_{a-1} - w_{a-1} + s_{a,j}^{\mathrm{LP}^f} + s_{a-1,j}^{\mathrm{RP}^g} \in \mathrm{AF} \\
&\text{s.t.} \quad \mathrm{LP}^f \text{ and } \mathrm{RP}^g \text{ overlap at the horizontal cell row} \\
&\qquad s_{a,j}^{\mathrm{FB}^m} + s_{h,j-1}^{\mathrm{FT}^n} \in \mathrm{AF} \\
&\text{s.t.} \quad \mathrm{FB}^m \text{ and } \mathrm{FT}^n \text{ overlap at the vertical cell row.} \qquad (1)
\end{aligned}$$

The objective can be made aware of cells in critical paths by a weighting function. Since the available number of allowable spacings is very small, obtaining a completely assist-correct solution is usually not possible in a fixed cell-row width context. Therefore, a more tractable objective is to minimize the expected CD error at a predetermined defocus level. This "continuous" version of the problem is similar in nature to placement legalization of row-based placements but with manufacturability-based cost metrics instead of traditional wirelength metrics. Placement legalization has been previously solved in the literature [22] using dynamic programming techniques. We solve this "continuous" version of the aforementioned problem with the following dynamic programming recurrence:

$$\begin{aligned}
&\mathrm{Cost}(1,b) = |x_1 - b| \\
&\mathrm{Cost}(a,b) = \lambda(a)\,|(x_a - b)| + \mathrm{Min}_{i=x_{a-1}-\mathrm{SRCH}}^{x_{a-1}+\mathrm{SRCH}} \\
&\qquad \times \{\mathrm{Cost}(a-1,i) + \alpha \mathrm{HCost}(a,b,a-1,i) \\
&\qquad\quad + \beta \mathrm{VCost}(a,b)\}. \qquad (2)
\end{aligned}$$

[5]Gates are typically laid out in a single orientation. We assume this orientation to be vertical in this paper.

HCost(a,b,a-1,i) of Cell $C_{a,j}$

Input:
User-defined weight for overlapping field polys : c_{ff}
User-defined weight for overlapping gate polys : c_{gg}
User-defined weight for overlapping gate and field polys : c_{gf}
Origin x (left) coordinate $C_{a,j}$ = b
Origin x (left) coordinate $C_{a-1,j}$ = i
Width of cell $C_{a,j}$ = w_a
Width of cell $C_{a-1,j}$ = w_{a-1}

Output:
Value of $HCost(a,b,a-1,i)$: horizontal cost of placing cell C_a at placement site b when C_{a-1} is placed at site i.

Algorithm:
01.**Case** $a = 1$: $HCost(1,b,0,i) = 0$
02.**Case** $a > 1$ **Do**
03. For every pair of left poly geometry in cell $C_{a,j}(LP)$ and right poly geometry in cell $C_{a-1,j}(RP)$ that overlap{
04. Call the geometries *LP*, *RP*
/* Let Hspace be the spacing between *LP* and *RP*. Let AF_l be the largest assist correct spacing smaller than Hspace. Let the CD degradation slope(delta CD/delta spacing) for AF_l be $slope(l)$. */
05. Split the vertical overlap between LP and RP into field-to-field O_{ff}, field-to-gate O_{fg} and gate-to-gate O_{gg} overlaps.
/* Calculate overlap weight between *RP* and *LP* */
06. $weight = slope(l) \times (Hspace - AF_l) \times (c_{ff}O_{ff} + c_{gf}O_{gf} + c_{gg}O_{gg})$ s.t. $AF_{l+1} > Hspace \geq AF_l$,
07. $HCost(a,b,a-1,i)$ += $weight$}

Fig. 4. Horizontal cost *(HCost)* calculation.

Cost (a,b) is the cost of placing cell a at placement site number b. The cells and the placement sites are indexed from left to right in the standard cell row. α and β give the relative importance between HCost and VCost. Typically, HCost has more weight because HCost is related to gate printability which determines device performance. HCost is the measure of total expected CD degradation of vertical poly geometries at the worst defocus for the cell. It can be thought of as the weighted change in the area of vertical poly geometries in the cell. Similarly, VCost is the measure of total expected CD degradation of horizontal poly geometries at the worst defocus.

Note the aforementioned memoryless cost structure which ensures that once the optimal solution up to cell i is obtained, it contains the optimal solution up to cell $i-1$. This optimal substructure is essential for dynamic programming. We restrict the perturbation of any cell to $\pm$SRCH placement sites from its initial location. This helps contain the delay and runtime overheads of AFCorr placement postprocessing. λ is a factor which decides the relative importance of preserving the initial placement and the final AFCorr benefit achieved for each given cell instance; in the current implementation, λ is directly proportional to the number of critical timing paths that pass through the given cell instance. HCost and VCost correspond to the printability deterioration under defocus conditions for the horizontal and vertical interactions, respectively. Cost (a,b) depends on the difference between the current nearest neighbor spacing of the polys and the closest assist-feature-correct spacing. The methods that we use to compute HCost and VCost are shown in Figs. 4 and 5. slope(l) is defined as the delta CD difference over delta pitch between AF_l and AF_{l+1}. Thus, perturbation cost is a function of slope, length, and weight of overlapped polys, and space for SRAF insertion. Our algorithm takes a legal placement as an input, and it outputs a legal placement with better DOF properties. In addition, VCost depends on the number of abutted cells L and R and the number of

VCost(a,b) of Cell $C_{a,j}$

Input:
$C_{a,j}$: a^{th} cell in j^{th} row
User-defined weight for overlapping field polys : c_{ff}
Origin x (left) coordinate $C_{a,j} = b$

Output:
$VCost(a,b)$: vertical cost of placing cell C_a at placement site b.

Algorithm:
01. **Case** $j = 1$: $VCost(a,b) = 0$
02. **Case** $j > 1$ **Do**
03. For every pair of bottom poly geometry in cell $C_{a,j}(FB)$ and top poly geometry in cell $C_{h,j-1}(FT)$ that overlap{
04. Call the geometries FB, FT
/* Let Vspace be the vertical spacing between FT and FB.
Let AF_l be the largest assist correct spacing smaller than Vspace.
Let O_{ff} denote the field-to-field overlap lengths. */
05. $weight = slope(l) \times c_{ff} O_{ff} \times (Vspace - AF_l)$
s.t. $AF_{l+1} > Vspace \geq AF_l$,
06. $VCost(a,b)$ += $weight$ }

Fig. 5. Vertical cost *(VCost)* calculation.

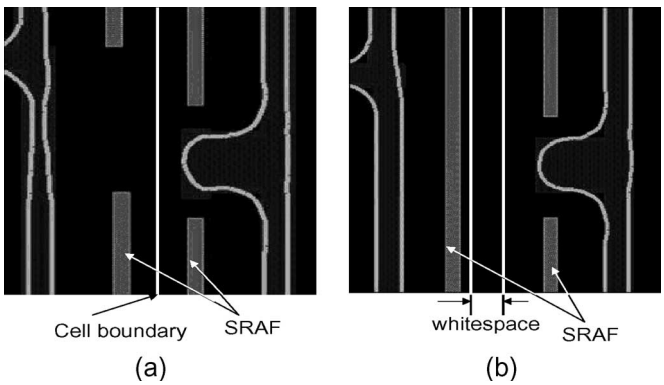

Fig. 6. (a) Cell placement before the horizontal AFCorr. (b) Cell placement after the horizontal AFCorr.

field-to-field poly interactions. The runtime of the AFCorr algorithm is $O(\text{ncell} \times \text{SRCH})$, where ncell is the total number of cells in the design.

Fig. 6 shows an example of a resist image profile with and without AFCorr technique. The H forbidden pitch is caused by interactions of poly geometries in the same row. After cell-placement perturbation in horizontal direction, additional SRAFs can be inserted at increased whitespace between cells, and thus, pattern printability is enhanced. In addition, the V forbidden-pitch violation is caused by inter-cell row interactions. As shown in Fig. 7(a), there is not enough space between the vertically adjacent poly geometries (coming from cells in adjacent cell rows), which results in less SRAFs than needed. By moving the cell in the upper row leftward, this violation can be removed and the printability can be enhanced.

D. Experimental Setup and Results

We synthesize the aes and alu128 benchmark designs from Opencores in Artisan TSMC 130 nm and 90 nm libraries using the Synopsys Design Compiler v2003.06-SP1. aes synthesizes to 12 993 and 10 286 cells in 130 nm and 90 nm technologies, respectively. alu128 synthesizes to 13 279 and 8722 cells in 130 nm and 90 nm technologies, respectively. The synthesized

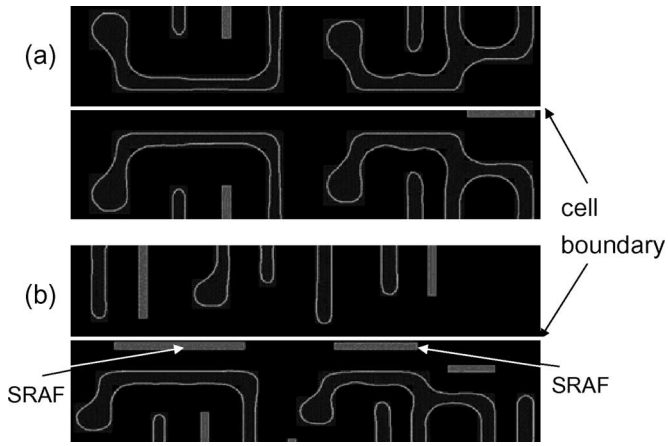

Fig. 7. (a) Cell placement before the vertical AFCorr. (b) Cell placement after the vertical AFCorr.

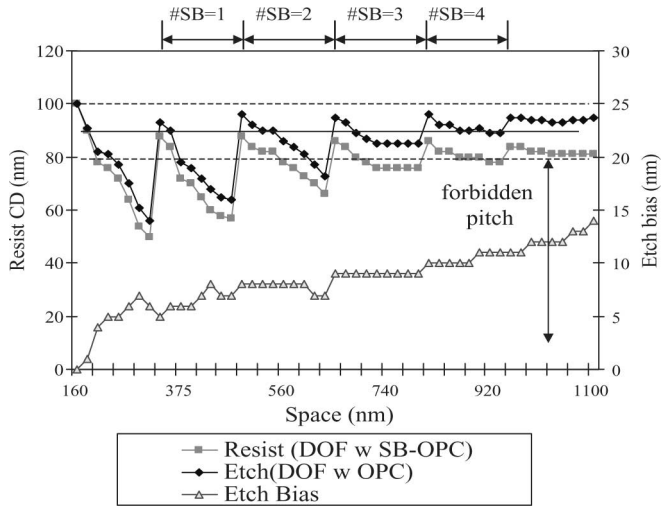

Fig. 8. Through pitch proximity plots and etch skew for 90 nm technology: Worst defocus with SRAF OPC and worst defocus with (left y-axis) etch OPC and (right y-axis) etch bias are shown.

netlists are placed with row utilization ranging from 50% to 90% using the Cadence First Encounter v3.3. All designs are trial-routed before running the timing analysis. On the lithography side, we use KLA-Tencor Prolith v9.1 to generate models for the OPC. Mentor Graphics Calibre v9.3_5.12 is used for the model-based OPC, SRAF OPC, and optical rule checking. Photo simulation is performed with wavelength $\lambda = 248$ nm and NA $= 0.6$ for 130 nm and $\lambda = 193$ nm and NA $= 0.75$ for 90 nm. An annular aperture with $\sigma = 0.85/0.65$ is used.

We use three printability quality metrics. Forbidden-pitch count is the number of border-poly geometries estimated as having greater than 10% CD error through-focus. Edge placement error (EPE) count is the number of edge fragments on border-poly geometries having greater than 10% EPE at the worst defocus level. SB count is the total number of SBs or SRAFs inserted in the design. A higher number of SRAFs indicates less through-focus variation and is hence desirable. We use $c_{\text{fg}} = c_{\text{gg}} = c_{\text{ff}} = 0.33$, $\lambda(a) = \text{sitewidth}/10 \times (\text{number of top 200 critical paths passing through cell } a)$ and SRCH $= 20$.

TABLE II
SUMMARY OF FORBIDDEN-PITCH RESULTS. FORBIDDEN-PITCH COUNTS SLIGHTLY CHANGE BASED ON DIFFERENT H VERSUS V WEIGHTS

	Utilization (%):	90		80		70		60		50	
	H:V weight	H F/P	V F/P	H F/P	V F/P	H F/P	V F/P	H F/P	V F/P	H F/P	V F/P
130 nm	0.9:0.1	4002	92	290	21	2	5	0	0	0	0
	0.7:0.3	5234	60	533	15	5	2	1	0	0	0
	0.5:0.5	5878	54	573	14	10	1	2	0	0	0
90 nm	0.9:0.1	4639	82	541	21	10	5	0	0	0	0
	0.7:0.3	5321	70	721	15	11	2	1	0	0	0
	0.5:0.5	6072	43	891	14	14	1	1	0	0	0

We first evaluate lithography printability of AFCorr with H and V assist corrections. Proximity plot with fixed linewidth for the 130 nm RET is shown in Fig. 2. CD degradation increases through pitch as the defocus level increases. Patterns in the pitches of over 0.4 μm before an OPC are outside the allowable tolerance range at the worst defocus of 0.5 μm. After the bias OPC, pitches up to 0.38 μm are allowable for CD tolerance, whereas all pitches larger than 0.38 μm should be forbidden. After evaluating the SRAF OPC patterns with the worst defocus model, a set of forbidden pitches of 0.13 μm technique is obtained: [0.37, 0.51), [0.635, 0.73), [0.82, 0.95), and [1.09, 1.17) (in micrometers). The forbidden pitches still remain after SRAF OPC even though the SRAF insertion considerably reduces the forbidden pitches compared with the bias OPC. Proximity plot with SRAF OPC for 90 nm technology is shown in Fig. 8. Resist CDs after SRAF OPC are evaluated with the worst defocus model of 0.4 μm. Resist CDs violate the allowable CD tolerance[6] as distance between the SRAF and the poly increases. A set of forbidden pitches of resist CD for 90 nm RET is calculated: [0.3, 0.41), [0.45, 0.57), [0.64, 0.73), and [0.78, 0.89) (in micrometers). We generated the SRAF rules which may be summarized, as shown in Table I. SRAF width and SRAF-to-pattern space are 40 nm and 120 nm, respectively, for 90 nm technology.

Table II shows the results of H and V forbidden pitches with various H versus V weights. Increasing weight of HCost reduces the number of H forbidden pitches while increasing the number of V forbidden pitches. H and V forbidden-pitch counts are reduced by 94%–100% and 76%–100% for 130 nm and by 96%–100% and 87%–100% for 90 nm, respectively. The design with 0.9 α for HCost and 0.1 β for VCost weights results in the highest reductions of total forbidden-pitch counts and is chosen to evaluate the SB count, the running time, etc. Fig. 9 shows that the total number of SRAFs increases as the utilization decreases due to an increased whitespace between cells. The benefit of AFCorr decreases with lower utilization because the design has already enough whitespace for the SRAF insertion. Due to the additional number of SRAFs inserted, there is a small increase in SRAF OPC runtime ($< 3.6\%$) and final data volume ($< 3\%$). Reductions of EPE and forbidden pitch are investigated for each utilization, as shown in Fig. 10. Total forbidden-pitch count is reduced by 89%–100% in 130 nm and 93%–100% in 90 nm. The EPE count is reduced by 80%–98% in 130 nm and 83%–100% in 90 nm. In addition, the SB count improves by 0.1%–7.4% for 130 nm and 0%–7.9% for 90 nm.

[6]Allowable CD tolerance is assumed to be 10% of minimum linewidth in the worst defocus level.

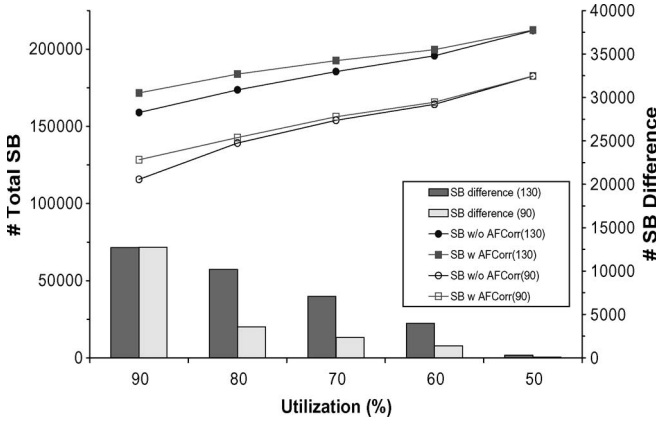

Fig. 9. Number of SRAFs with and without AFCorr for each of the five different utilizations.

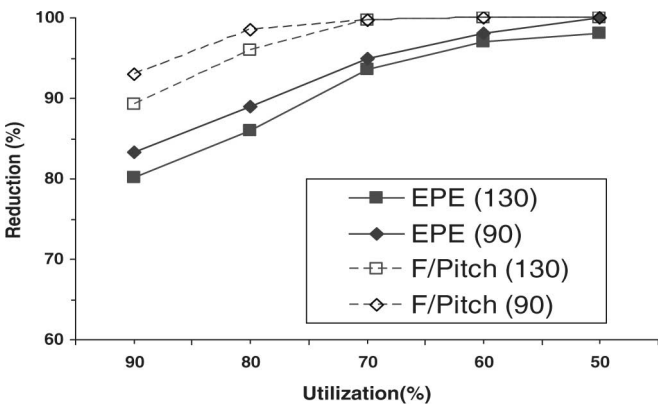

Fig. 10. Reductions of forbidden pitches with AFCorr methodology for each of the five different utilizations.

Note that these numbers are small as they correspond to the entire layout rather than just the border-poly geometries. The change in estimated post-trial route circuit delay ranges from -7% to $+11\%$. All of these results for AFCorr are summarized in Table III.

III. ETCH-DUMMY CORRECTNESS

A. Etch Dummy and Layout Impact

Insertion of etch-dummy features has been introduced to reduce the CD difference between the resist and etch processes for 90 nm and below technology nodes. In dry etch processes such as plasma, ion, and reactive-ion etch, different consumptions of etchants with different pattern densities lead to etch skew between the dense and isolated patterns. For example, all available etchants in areas with low density are consumed

TABLE III
SUMMARY OF AFCorr RESULTS. RUNTIME DENOTES THE RUNTIME OF SRAF AND ETCH-DUMMY INSERTION AND MODEL-BASED OPC. THE AFCorr PERTURBATION RUNTIME RANGES FROM 2 TO 3 min FOR ALL TEST CASES. GDS SIZE IS THE POST-SRAF OPC DATA VOLUME

	Utilization (%):	90		80		70		60		50	
	Flow:	Typical	AFCorr	Typical	AFCorr	Typical	AFCorr	Typical	AFCorr	Typical	AFCorr
130 nm	# Forbidden	20632	4094	3201	311	2011	7	1421	0	219	0
	# SB	158987	171691	173673	183860	185493	192578	195741	199704	212079	212412
	# EPE	4630	4721	5975	562	4276	15	1732	0	199	0
	Runtime (s)	7821	7902	7876	7934	7913	7973	7998	8013	8021	8121
	GDS (MB)	48.9	48.9	48.8	48.9	48.2	48.4	48.3	48.5	48.2	48.4
	Delay (ns)	4.2	4.6	4.5	4.7	4.5	4.6	4.6	4.9	5.2	5.4
90 nm	# Forbidden	22121	4721	4821	562	3812	15	2001	0	321	0
	# SB	115652	128387	139182	147520	153904	156244	164264	165649	182572	182666
	# EPE	7523	1262	4813	532	2131	107	1329	59	163	5
	Runtime (s)	6211	6327	6322	6431	6482	6499	6521	6571	6672	6692
	GDS (MB)	43.1	43.3	43.2	43.3	43.2	43.3	43.7	43.8	44.6	44.8
	Delay (ns)	2.7	2.7	2.6	2.6	2.4	2.47	2.8	2.9	3.1	3.2

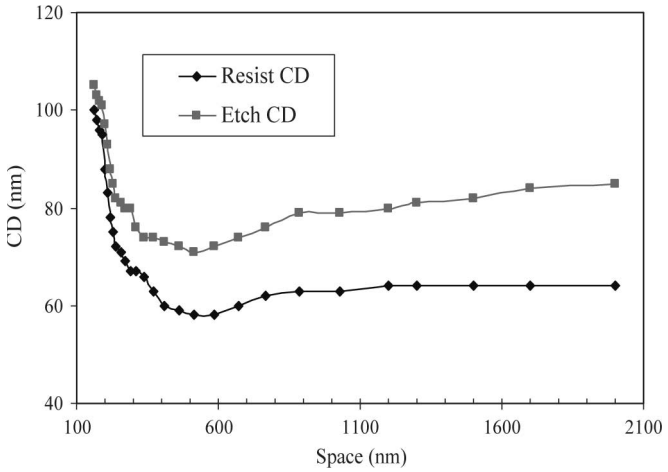

Fig. 11. Different proximity behaviors between photo and etching processes with pitch.

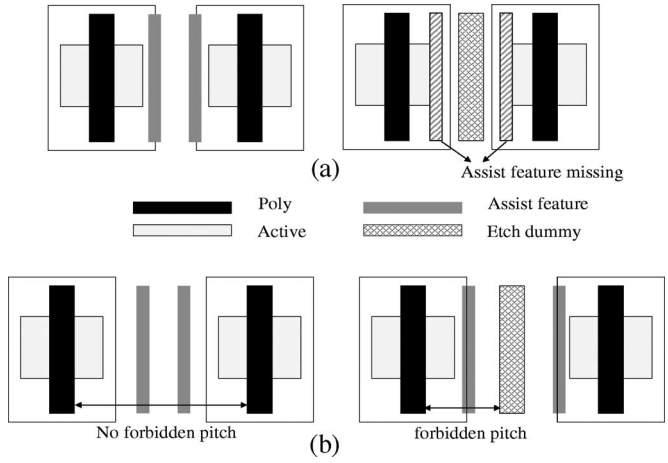

Fig. 12. Conflict between SRAF and etch-dummy rules. (a) Assist-feature missing. (b) Forbidden-pitch occurrence.

rapidly, and thus, the etch rate then drops off significantly. In areas with high density of patterns, the etchants are not consumed as quickly. As a result, the proximity behavior of the photo process differs from that of etch process, as shown in Fig. 11. Therefore, there is a CD skew between the resist and etch processes with varying pitch. In general, the etch skew of the two processes increases as the pitch increases. The OPC cannot determine the extent of layout distortion to match the layout pattern to the photoresist edges and the poly edge (after etch process) simultaneously. The OPC is typically used to compensate for the CD variation of the resist process, and then, the etch dummies are inserted to reduce the CD skew between the two processes.

When the etch dummies are placed adjacent to primary patterns, a relatively isolated primary line will behave more like a dense line, and thus, the etch dummies can reduce the etch skew. Moreover, the maximum relevant pitch is reduced through the etch-dummy insertion. This is an important consideration with respect to the model-based OPC, which calculates the proximity effect of all patterns within a given proximity range, such that a larger proximity range increases the OPC runtime. Granik [4] observes that the proximity range of the etch process is around 3 μm, which prevents the conventional model-based OPC from delivering a good OPC mask within a feasible turnaround time.

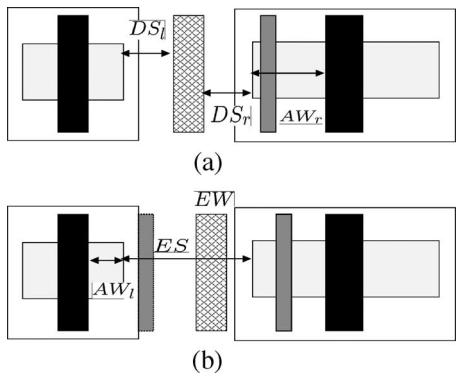

Fig. 13. (a) Typical etch-dummy generation. (b) SRAF-aware etch-dummy generation.

1) Etch-dummy-insertion problem: Given a layout, find an etch-dummy placement such that the following conditions are satisfied.

Condition 1) Etch dummies are inserted between the primary patterns with certain spacing to reduce the etch skew between the resist and etch processes.

Condition 2) Etch dummies are placed outside of the active-layer regions.

TABLE IV
COMPARISON OF ETCH-DUMMY RULES BETWEEN THE CONVENTIONAL ETCH-DUMMY METHOD AND THE SAEDM. NOTE THAT $AS_l + AS_r = ES - ED_l$

Etch dummy rules		Typical method		SAEDM	
	ES (X)	DS_l	DS_r	DS_l	DS_r
#ED = 0	$0 \le X < ED_1$				
#ED = 1	$ED_1 \le X < ED_2$	$(ES - EW)/2$	$(ES - EW)/2$	$AS_l + DAS$	$AS_r + DAS$
#ED = 2	$X \le ED_2$	DAS	DAS	$AS_l + DAS$	$AS_r + DAS$

Thus, the etch-dummy-correction problem is used to determine perturbations to intercell spacings to maximize insertion of etch dummy. Forbidden-pitch correction in the resist process is required after inserting the etch dummy because the etch dummy cannot be placed too close to the primary patterns due to Condition 2). The etch-dummy insertion can make the printability of the resist process worse in certain pattern configurations. Fig. 12 shows examples such as (a) missing assist feature and (b) forbidden-pitch occurrence. The assist features can be missed due to the lack of space between the primary pattern and the etch dummy even when there is enough space to insert multiple SRAFs before the etch-dummy insertion. New forbidden pitches for assist features can occur in the spacing between the poly and the etch dummy due to the mismatch between the rules for assist-feature and etch-dummy corrections. Therefore, we now propose a new Corr problem that combines the assist-feature and etch-dummy insertion methods as follows.

Assist-feature- and etch-dummy-correction problem: Given a standard-cell layout, determine the perturbations to intercell spacings to simultaneously insert the SRAFs in forbidden pitches and insert the etch dummies to reduce the etch skew.

B. SRAF-Aware Etch-Dummy Generation

To reduce the etch proximity, at most one etch dummy for each active (or diffusion) geometry is needed since the etch skew depends on pattern-to-pattern spacing regardless of local pattern density [10], i.e., the etch skew decreases as the spacing is reduced. SRAFs and etch dummies have been generated by rule-based methods with lookup tables since the simulation tools are much slower than the rule-based tools. Typically, etch-dummy rules consist of etch dummy-to-active space (DAS), etch-dummy width (EW), and etch dummy-to-dummy space (DDS) with respective values of 120, 100, and 200 nm being typical for 90 nm technology. Let ES denote the space between the active geometry in the left and right cells, as shown in Fig. 13. Let ED_1 and ED_2 denote the required spaces to insert one and two etch dummies in ES, respectively. For typical methods of etch-dummy insertion, the minimum space rules for one and two etch dummies are $ED_1 = 2 * DAS + EW$ and $ED_2 = 2 * DAS + 2 * EW + DDS$, respectively. The first etch dummy in the typical etch-dummy rule is always placed at the center of the space between the two active geometries, whereas the active-to-etch-dummy space for the second etch dummy is always according to the space rule (DAS).

Once the etch dummies have been inserted for only etch-proximity control, the spacing between the poly and the etch dummy may not be appropriate for the SRAF insertion. Fig. 13(a) shows an example where the left-hand-side SRAF cannot be inserted due to the lack of poly-to-etch-dummy spacing. Let AW_l and AW_r denote the distances between the border polys and the active geometries located at the left and right cells, respectively. Let $AF = AF_1, \ldots, AF_m$ denote a set of "assist-correct" spacings. AF_j is the j^{th} member of the set of assist-feature-correct spacings AF. Let AS_l and AS_r denote the additional spacings needed for assist-correctness in the left and right cells, respectively. To avoid missing SRAFs and occurrence of forbidden pitches, we propose a new SAEDM considering active width (AW) during the insertion of etch dummy, as follows:

$$\begin{aligned} \text{Minimize} \quad & \text{index values of } j \text{ and } k \text{ in a set AF} \\ \text{s.t.} \quad & AS_l = AF_j - (AW_l + DAS) \\ & AS_r = AF_k - (AW_r + DAS) \\ & (AS_l + AS_r) \le (ES - ED_1). \end{aligned} \tag{3}$$

The SAEDM searches assist-correct spacings with minimum index values in a set AF, so that the sum of the additional spacings AS_l and AS_r corresponding to the assist-correct spacings is less than $(ES - ED_1)$. Let DS_l and DS_r denote the left and right spaces from the etch dummy to the border active geometries in the left and right cells, respectively. Thus, new etch-dummy spaces of $DS_l = AS_l + DAS$ and $DS_r = AS_r + DAS$ are both assist-correct and etch-dummy correct. Note that the etch dummy after SAEDM is no longer located at the center of an active-to-active space since DS_l differs from DS_r, as shown in Fig. 13(b). Table IV compares the DS_l and DS_r values returned by the typical etch-dummy method and by the SAEDM.

C. Corr Placement Algorithm

Assist-correct pitch rules are violated if there is not enough space to insert AS_l and AS_r. We now describe an etch-dummy-correction placement-perturbation algorithm that uses intelligent whitespace management. EtchCorr differs from AFCorr as follows: 1) Corr is based on the active-to-cell outline spacing, whereas AFCorr is based on the poly-to-cell outline spacing; and 2) Corr calculates the virtual positions of etch dummy in order to both insert the SRAF in assist-correct spacing and the etch dummy in etch-dummy-correct spacing (EDS). Let EDS be the interdevice spacing with etch skew less than 10% of minimum linewidth. Thus, the etch-dummy-correct perturbation problem is used to minimize design perturbation to insert the etch dummies optimally and, thus, to reduce the etch skew between the resist and etch processes. However, as discussed above, a new design correction technique Corr which combines the assist-correct (AFCorr) and etch-correct (EtchCorr) placement methods is required to avoid conflict between the assist-feature and etch-dummy insertions.

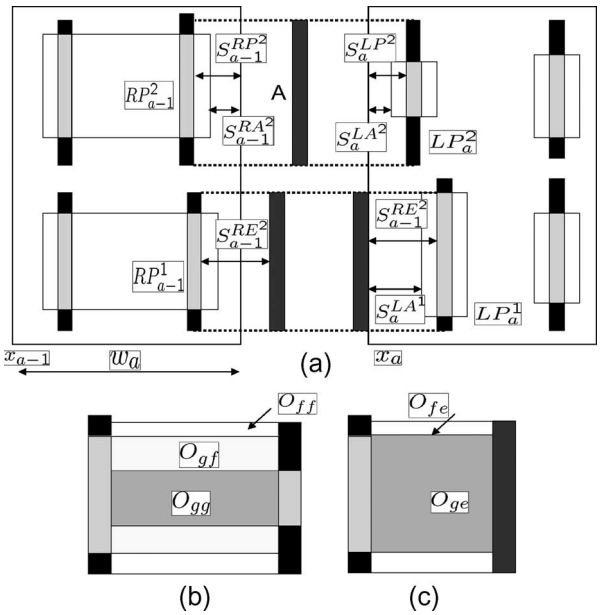

Fig. 14. Placement-perturbation problem for assist and etch-dummy insertion. (a) Multiple interactions of gate-to-dummy and field-to-dummy. (b) Overlap area when there is no etch dummy. (c) Overlap area in the presence of etch dummy.

In the following, we describe the single-row Corr perturbation algorithm. Let $s_a^{\mathrm{RP}_i}$ and $s_a^{\mathrm{RA}_j}$ denote the spacing between the right outline of the cell and the i^{th} right border-poly, and the spacing between the right outline of the cell and the j^{th} active geometry, respectively. $s_a^{\mathrm{RE}_i}$ is the spacing from the right border-poly to the etch dummy, as shown in Fig. 14. Let δ denote a cell-placement perturbation to adjust the spacing between cells. ES, the space between border actives, is $x_a - x_{a-1} - w_{a-1} + s_{a-1}^{\mathrm{RA}_i} + s_a^{\mathrm{LA}_i}$. Then, the **Corr placement-perturbation problem** is

$$\text{Minimize } \sum |\delta_i| \text{ such that}$$

$$\begin{cases} \text{If } (\mathrm{ES} < \mathrm{ED}_1) \\ \delta_a + x_a - x_{a-1} - \delta_{a-1} - w_{a-1} + s_{a-1}^{\mathrm{RP}^i} + s_a^{\mathrm{LP}^i} \in \mathrm{AF} \\ \delta_a + x_a - x_{a-1} - \delta_{a-1} - w_{a-1} + s_{a-1}^{\mathrm{RA}^i} + s_a^{\mathrm{LA}^i} \in \mathrm{EDS} \\ \text{s.t.} -\mathrm{SRCH} \le \delta_{a-1} \text{ and } \delta_a \le \mathrm{SRCH} \\ \text{otherwise} \\ S_{a-1}^{\mathrm{RP}^i} - S_{a-1}^{\mathrm{RA}^i} + S_{a-1}^{\mathrm{RE}^i} + \delta_{a-1}, S_a^{\mathrm{LP}^i} - S_a^{\mathrm{LA}^i} + S_a^{\mathrm{LE}^i} + \delta_a \in \mathrm{AF} \\ S_{a-1}^{\mathrm{RE}^i} + \delta_{a-1} \text{ and } S_a^{\mathrm{LE}^i} + \delta_a \in \mathrm{EDS} \\ \text{s.t.} -\mathrm{SRCH} \le \delta_{a-1} \text{ and } \delta_a \le \mathrm{SRCH} \end{cases} \tag{4}$$

$$\mathrm{Cost}(1,b) = |x_1 - b|$$

$$\begin{aligned} \mathrm{Cost}(a,b) = \lambda(a)|(x_a - b)| + \mathrm{Min}_{i=x_{a-1}-\mathrm{SRCH}}^{x_{a-1}+\mathrm{SRCH}} \\ \times \{\mathrm{Cost}(a-1,i) + W_1 \mathrm{AFCost}(a,b,a-1,i) \\ + W_2 \mathrm{EDCost}(a,b,a-1,i)\}. \end{aligned} \tag{5}$$

The terms AFCost and EDCost denote the assist-feature and etch-dummy costs, respectively. AFCost depends on the difference between the current nearest neighbor spacing of the polys and the closest assist-correct spacing. The methods of computing AFCost and EDCost are shown in Fig. 15.[7] The formulation is similar to the AFCorr when the space

Cost(a,b,a-1,i) of Cell C_a

Input:
User-defined weights for poly-to-poly overlap: c_{gg}, c_{ff}, c_{gf}
User-defined weights for poly-to-dummy overlap: c_{ge}, c_{fe}
Width of cell C_a = w_a

Output:
Value of *AFCost* and *EDCost*: costs for corrections of assist feature and etch dummy of placing cell C_a at placement site b, respectively.

Algorithm:
/* Cost of placing cell C_a at placement site 'b' when cell C_{a-1} is placed at site 'i'. */
Let *AFspace* denote the horizontal spacing between *RP* and *LP*.
Let *ES* denote the horizontal spacing between *RA* and *LA*.
Let $AFslope(j)$ be defined as ratio of resist CD degradation and change in pitch between AF_j and AF_{j+1}.
Let $EDslope(j)$ be defined as ratio of etch CD degradation and poly-to-dummy space.
Let ED_1 denote the required spaces to insert one etch dummy.
01. **Case** $a = 1$: $AFCost(1,b) = EDCost(1,b) = 0$
02. **Case** $a > 1$ **Do** {
03. **If** $(AFspace < ED_1)$ {
04. For every pair of left poly geometry in cell $C_a(LP)$ and right poly geometry in cell $C_{a-1}(RP)$ that overlap{
05. Call the geometries *LP*, *RP*
06. Split the vertical overlap between LP and RP into field-to-field O_{ff}, field-to-gate O_{fg} and gate-to-gate O_{gg} overlaps.
07. $AFweight = AFslope(j) \times (AFspace - AF_j) \times (c_{ff}O_{ff} + c_{gf}O_{gf} + c_{gg}O_{gg})$ s.t. $AF_{j+1} > AFspace \ge AF_j$
08. $EDweight = EDslope(AFspace) \times (c_{ge}O_{ge} + c_{fe}O_{fe})$ }}
09. **Else** {
10. For every pair of pattern geometries in $C_a(LP)$, $C_{a-1}(RP)$ and dummy that overlap{
11. Call the geometries *LP*, *RP*, and a dummy pattern
12. Split the vertical overlap between poly and dummy into gate-to-dummy c_{ge} and poly-to-dummy c_{fe} overlaps.
13. $AFweight = AFslope(j) \times (AW_l + DS_l - AF_j) \times (c_{ge}O_{ge} + c_{fe}O_{fe})$
14. $AFweight += AFslope(l) \times (AW_r + DS_r - AF_l) \times (c_{ge}O_{ge} + c_{fe}O_{fe})$
15. $EDweight = (EDslope(AW_l + DS_l) + EDslope(AW_r + DS_r)) \times (c_{ge}O_{ge} + c_{fe}O_{fe})$ }}
16. $AFCost(a,b,a-1,i)$ += $AFweight$
17. $EDCost(a,b,a-1,i)$ += $EDweight$ }

Fig. 15. Algorithm for AFCost and EDCost computations.

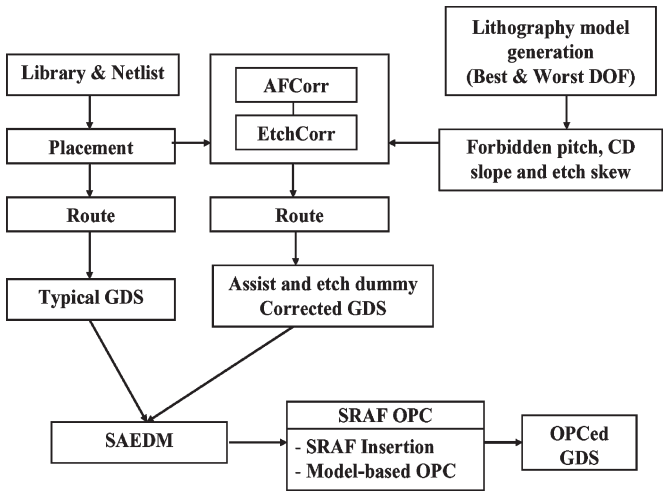

Fig. 16. Modified design and evaluation flows: Note the added steps of forbidden-pitch extraction, SAEDM, and post-placement optimization to the ASIC design flow.

[7]The figure shows only the horizontal AFCost computation for simplicity. We do not compute the vertical EDCost as the primary focus of the etch-dummy gate CD control.

TABLE V
ETCH-PROCESS CONDITIONS FOR THE SIMULATOR IN 90 nm TECHNIQUE

Stage	Etch time (sec)	Material	Vertical etch rate (sec)	Horizontal etch rate (sec)	Faceting Parameter Parameter
1	10	ArF Sumitomo	10.66	-0.6	0.5
		AZ BarLi-2	10.52	-0.7	0.0
		Si Nitride	10.28	-0.7	0.0
2	60	ArF Sumitomo	0.3	-0.12	0.5
		AZ BarLi-2	3.4	-0.2	0.0
		Si Nitride	30.4	-0.3	0.0
3	36	ArF Sumitomo	10.65	0.9	0.5
		AZ BarLi-2	0.25	1.0	0.0
		Si Nitride	0.0	1.5	0.0

between the border actives is not enough for a dummy insertion. However, the Corr perturbation problem calculates the poly-to-dummy spacings instead of the poly-to-poly spacings when there are etch dummies between cells. O_{gg}, O_{ff}, and O_{ff} correspond to the length of overlap areas of gate-to-gate, field-to-field, and gate-to-field polys, respectively, as shown in Fig. 14. O_{ge} and O_{fe} correspond to the overlapped length of gate-to-dummy and field-to-dummy, respectively. In addition, c_{gg}, c_{ff}, and c_{ff} are the proportionality factors which specify the relative importance of printability for gate and field polys. W_1 and W_2 are user-defined weights for AFCost and EDCost, respectively.

D. Modified Design and Evaluation Flow

To account for new geometric constraints that arise due to SRAF OPC in physical design, we add forbidden-pitch extraction and postplacement optimization into the current application-specific integrated-circuit (ASIC) design methodology. Fig. 16 shows the modified design and evaluation flows in the regime of forbidden-pitch restrictions. Of course, we must assume that the library cells themselves have been laid out with awareness of forbidden pitches, and indeed, our experiments with commercial libraries confirm that there are no forbidden-pitch violations in poly geometries within individual commercial standard cells. Our method solves the forbidden-pitch violations between the placed cells. The SRAF insertion rules of enhancing the DOF margin are determined based on the best and worst focus models.[8]

The post-placement optimization is performed based on the forbidden pitches and the slopes of CD error within them. After AFCorr (SAEDM and EtchCorr techniques will be described next in detail in this section), we obtain a new placement which is more conducive to the insertion of SRAFs, thus allowing a larger process window to be achieved. The two layouts generated by the conventional and assist-correct flows undergo a comprehensive SRAF OPC. The amount and impact of the applied RET are functions of the circuit layout. Thus, we can evaluate how the assist-correct placement impacts circuit performance and printability/manufacturability according to the metrics of SRAF insertions and EPE. The following sections give more details of forbidden-pitch extraction and design implementation.

[8]In general, the best focus is shifted from zero to about 0.1 μm due to the refraction in the resist. The worst defocus is the maximum allowable defocus corner for manufacturability in a lithography system. As the CD tolerance is $\pm 10\%$, the worst defocus model can be extracted by the Bossung plot in Fig. 1, i.e., worst defocus model is 0.5 μm for 130 nm technology.

E. Experimental Setup and Results

To account for new geometric constraints that arise due to SRAF and etch dummy in physical design, we extract the forbidden pitch, the CD slopes of the resist and etch processes with pitch, and the CD skew induced by the etch process. Post-placement optimization generates a new placement wherein the coordinates of cells have been adjusted to avoid the forbidden pitches and to reduce the etch skew. The target etch process consists of three etch steps: 10-s breakthrough etch step to get through the bottom anti-reflective coating, 60-s main etch step, and 36-s overetch step. The breakthrough and main etch steps in the model produce a fair amount of deposition, taking the resist profile to 100 nm. The overetch step trims this back to the 90 nm range. A set of etch parameters is shown in Table V. We only consider the first etch step to remove the Si nitride because the second etch step, a step to etch the gate poly, does not impact the CD variation with pitch [1].

We use the same benchmark designs as AFCorr and evaluate the pattern printability with combinations of the following: 1) SAEDM; 2) AFCORR+SAEDM; and 3) AFCorr+EtchCorr+SAEDM. We generated the SRAF rules with results in Table I. SRAF width and SRAF-to-pattern space are 40 and 120 nm, respectively. In addition, DAS, EW, and etch DDS correspond to 120, 100, and 200 nm, respectively. However, the spacing between active and etch dummy is varying because the SAEDM changes the space with the AW. The resist and etch CDs vary with location of the SRAF insertion, and the resist CDs violate the allowable CD tolerance as distance between the SRAF and the poly increases. The trend of etch CD follows the variation of resist CD. The skew of resist and etch CDs continuously increases with pitch and is not saturated by 1.1 μm, as shown in Fig. 8.

After the Corr placement perturbation, we obtain a new placement wherein the coordinates of cells minimize the occurrence of forbidden pitches of the resist and etch processes. The total cost of Corr is calculated using the specific weights of the resist and etch costs (in the results reported, we use the respective weights $W_1 = 0.9$ and $W_2 = 0.1$). Note that our post-placement perturbation problem reduces to the previously studied AFCorr problem if $W_2 = 0$.

TABLE VI
FORBIDDEN-PITCH RESULTS WITH VARIOUS ETCH-DUMMY INSERTION METHODOLOGIES IN THE RESIST AND ETCH PROCESSES

	Utilization (%):	90	80	70	60	50
Photo	W/O SAEDM, W/O AFCorr, W/O EtchCorr	37433	31314	29216	26765	21282
	W SAEDM, W/O AFCorr, and W/O EtchCorr	15743	8330	4423	2075	1198
	W SAEDM, W AFCorr, and W/O EtchCorr	2432	822	23	0	0
	W SAEDM, W AFCorr, and W EtchCorr	3566	1116	51	0	0
Etch	W/O SAEDM, W/O AFCorr, and W/O EtchCorr	15816	8812	4656	4345	3530
	W SAEDM, W/O AFCorr, and W/O EtchCorr	16418	9729	5282	5002	4209
	W SAEDM, W AFCorr, and W/O EtchCorr	5423	2221	172	109	92
	W SAEDM, W AFCorr, and W EtchCorr	4321	1032	143	92	92

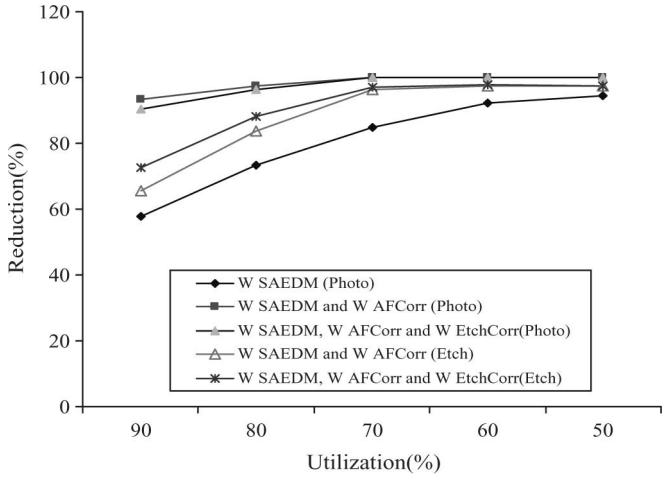

Fig. 17. Reductions of forbidden pitches with various etch-dummy insertion methodologies for each of the five different utilizations.

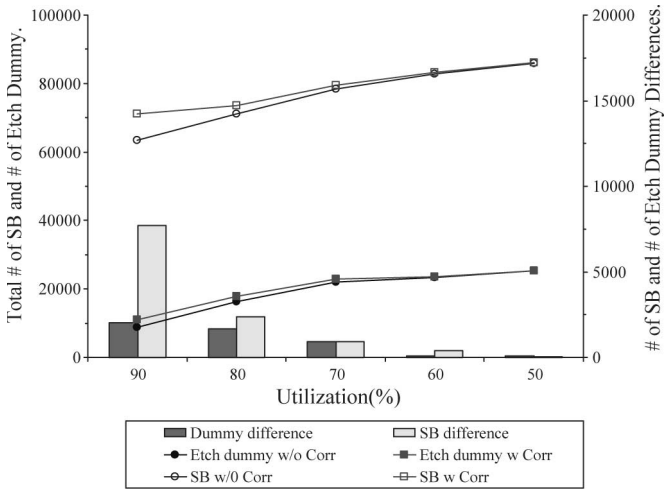

Fig. 18. Numbers of inserted SRAF and etch-dummy features with various etch-dummy insertion methodologies for each of the five different utilizations.

We evaluate the reduction of forbidden-pitch count with various etch-dummy insertion methodologies in the resist and etch processes shown in Table VI. After 1) SAEDM, the forbidden-pitch count of photo process can be reduced by 57%–94% with various utilizations because the etch-dummy-to-poly spacings become assist-correct. However, the forbidden-pitch count of the etch process may increase by up to 6% in certain layout configurations since the SAEDM increases the poly-to-etch-dummy spacing. The forbidden-pitch counts of etch process in 2) SEADM+AFCorr and 3) Corr+SAEDM are reduced by up to 64%–97% and 73%–98%, respectively, across a range of utilizations, as shown in Fig. 17. Corr+SAEDM facilitates additional SRAF and dummy insertions by up to 10.8% and 18.6%, respectively. Fig. 18 shows that the total numbers of SRAFs and etch dummies increase as the utilization decreases. Note that these numbers are small as they correspond to the entire layout rather than just the border-poly geometries. The EPE count is reduced by 91%–100% in the resist process and 72%–98% in the etch process. The change in the estimated post-trial route circuit delay ranges from 3% to 5.8%. The increases of data size and OPC running-time overheads of Corr are within 3% and 4%, respectively. The runtime of Corr placement perturbation is negligible (∼5 min) compared with the running time of OPC (∼2.5 h). All of these results for Corr are summarized in Table VII.

IV. CONCLUSION AND ONGOING WORK

In this paper, we have presented novel methods to optimize the etch-dummy insertion rules and the detailed standard-cell placements for improved etch-dummy and assist-feature insertions. We obtain a practical and effective approach to achieve assist-feature compatibility in physical layouts. AFCorr, as an approach to achieve the assist-feature compatibility, leads to reduced CD variation and enhanced DOF margin. We also introduce a dynamic programming-based technique (Corr) to achieve etch-dummy-insertion correctness in the detailed placement step of standard-cell-based chip implementation. Corr with SAEDM leads to reduced CD variation and increased insertion of assist features and etch dummies. For our test industrial cases, we have observed the following.

1) In lithographic-printability evaluation of AFCorr, the H and V forbidden-pitch counts for border-poly geometries are reduced by 94%–100% and 76%–100% for 130 nm and by 96%–100% and 87%–100% for 90 nm, respectively. For EPE count, reductions of 80%–98% in 130 nm and 83%–100% in 90 nm are obtained. We also achieve up to 7.6% increase in the number of inserted SBs.
2) In pattern-printability evaluation, the forbidden-pitch counts of photo process between the polysilicon shapes of neighboring cells are reduced by up to 54%–94%, 92%–100%, and 90%–100% for SAEDM, SAEDM+AFCorr, and SAEDM+Corr, respectively. The forbidden-pitch counts of etch process of SEADM+AFCorr and SAEDM+Corr are reduced by up

TABLE VII
SUMMARY OF SAEDM+Corr RESULTS. RUNTIME DENOTES THE RUNTIME OF SRAF AND ETCH-DUMMY INSERTIONS, AS WELL AS THE MODEL-BASED OPC. THE Corr PERTURBATION RUNTIME RANGES FROM 4 TO 5 min FOR ALL TEST CASES. GDS SIZE IS THE POST-OPC DATA VOLUME

	Utilization(%):	90		80		70		60		50	
	Flow:	Typical	SAEDM+Corr	Typical	SAEDM+Corr	Typical	SAEDM+Corr	Typical	SAEDM+Corr	Typical	SAEDM+Corr
Photo	# EPE	42102	3723	32434	1243	29349	98	28721	13	23134	2
	# Forbidden	37433	3566	31314	1116	29216	51	26765	0	21282	0
	# SB	63349	71051	71101	73501	78513	79432	82820	83230	85991	86026
Etch	# EPE	17209	4812	9213	1200	4820	182	4821	109	3890	109
	# Forbidden	15816	4321	8812	1032	4656	143	4345	92	3530	92
	# Dummy	8876	10911	16240	17920	22088	23001	23390	23499	25237	25309
Other	Runtime (s)	6835	7011	7451	7535	7529	7632	7685	7698	7943	7944
	GDS (MB)	41.1	42.3	41.2	43.2	42.2	42.3	42.9	42.8	43.6	43.6
	Delay (ns)	2.478	2.305	2.458	2.602	2.522	2.47	2.867	3.176	3.113	3.046

to 64%–97% and 73%–98%, respectively, across a range of utilizations. Corr with SAEDM facilitates additional SRAF and dummy insertions by up to 10.8% and 18.6%, respectively.

3) In impact on other design metrics, the increases of data size, OPC running time, and maximum delay overheads of Corr are within 3%, 4%, and 6%, respectively. In addition, the maximum delay overhead of 6% is within noise of the P&R tools [5]. The runtime of Corr placement perturbation is negligible (∼5 min) compared with the running time of OPC (∼2.5 h).

We are currently engaged in further experimental validation and research. Certain devices and cells may be able to tolerate more process variations than others in the design. We are investigating techniques to bias the AFCorr and EtchCorr solutions in favor of such devices to reduce timing and power impact and to increase overall parametric yield.

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