Toward Better Wireload Models in the Presence of Obstacles

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***Abstract*—Wirelength estimation techniques typically contain a site density function that enumerates all possible path sites for each wirelength in an architecture and an occupation probability function that assigns a probability to each of these paths to be occupied by a wire. In this paper, we apply a generating polynomial technique to derive complete expressions for site density functions which take effects of layout region aspect ratio and the presence of obstacles into account. The effect of an obstacle is separated into two parts: the *terminal redistribution* effect and the *blockage effect*. The layout region aspect ratio and the obstacle area are observed to have a much larger effect on the wirelength distribution than the obstacle's aspect ratio and location. Accordingly, we suggest that these two parameters be included as indices of lookup tables in wireload models. Our results apply to *a priori* wirelength estimation schemes in chip planning tools to improve parasitic estimation accuracy and timing closure; this is particularly relevant for system-on-chip designs where IP blocks are combined with row-based layout.**

***Index Terms*—Floorplanning, interconnect length estimation, obstacles, wireload models.**

I. Introduction

In DEEP submicron design, the importance of estimating interconnect parameters such as delay, power, wirelength, and routability increases; such estimates are part of the objectives of partitioning, placement and floorplanning tools. Also, the electronic design automation (EDA) flow is experiencing a trend of combining front end planning and physical implementation to help design convergence. In this process, an efficient yet accurate predictor of interconnect parameters (resource usage, performance, etc.) is crucial. The efficiency and accuracy of front end planning tools depend on the performance of floorplanning, placement, and partitioning tools, which in turn depend on that of the interconnect predictor.

Register transfer level (RTL) planning flows must constantly struggle with the chicken-egg impasse: 1) budgeting the path delays within blocks and between blocks and 2) finding a (good) placement of the blocks. Typically, this impasse is broken by using initial *wireload models*, i.e., statistically derived (or calibrated) estimates of routing lengths for given-sized nets placed in given-sized regions. These wireload models are certainly needed within blocks (since the blocks have not even been synthesized, let alone placed), and occasionally also between blocks (i.e., at the chip level); they are always needed at some point in the design flow. In this paper, we target *a priori* (preplacement) and online (during placement) wirelength estimations.

Wirelength estimation was initiated by Landman and Russo's paper [12] on Rent's rule, which was the basis for models of Donath [8], Davis *et al.* [7], and Stroobandt *et al.* [16]. A review of recent progress is given in [6]. Apart from techniques that estimate average wirelengths or wirelength distributions, individual net wirelength estimators have also been studied. These techniques exploit individual net information such as bounding-box dimensions or number of terminals to yield more accurate estimates. Current industry tools use lookup tables of wirelength as a function of number of terminals [3].[1] The aspect ratio of the region or net-bounding box is found to have a considerable effect on the expected wirelength for nets with few terminals [2].

All of these papers are based on regularly placed circuits such as gate array or standard-cell designs, with the exception of [3], which considers a building-block-design methodology. With the trend toward IP-block-based system-on-chip (SOC) design, it is more likely that the presence of macrocells as obstacles (e.g., memories or noise-sensitive memory blocks) may significantly lengthen wires and cause congestion. To the best of our knowledge, no work to date has provided interconnect wirelength site density functions in the presence of routing obstacles and the routing obstacle effect has been inadequately addressed for individual wirelength estimations. In [3], routing obstacles are handled by dividing the routing area into small bins, then applying global routing over the bins and using lookup tables for each bin. Recently, in [4], expected average wirelengths were predicted in the presence of obstacles.

Wirelength estimation techniques typically contain a *site-density function* that enumerates all possible path *sites* for each wirelength within a given routing resource architecture and an occupation probability function that assigns a probability to each of these paths to be occupied by a wire. In this paper, we combine the application of the generating polynomial technique [17] and the consideration of

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[1]Also, global routing may be used as a constructive estimator. Indeed, proponents of global routing—notably Scheffer and Nequist [13]—have argued that interconnect estimation can only be performed constructively. This is still an unresolved and somewhat controversial issue (e.g., contrast with the Monterey Design Systems emphasis on nonconstructive prediction and estimation). The analysis of [13] does acknowledge that different interconnect properties can be estimated with different levels of accuracy due to their inherent order statistics. Thus, we believe that the door is still open to development of strong *nonconstructive, a priori* interconnect estimation methods; this is the motivation for our present work.

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the presence of obstacles [4] to give a complete analysis of the wirelength distributions in the presence of obstacles. The generating polynomial technique leads to complete expressions for site density functions which take effects of layout region aspect ratio and the presence of obstacles into account. The effect of an obstacle is separated into two parts, the *terminal redistribution effect* and the *blockage effect*. The layout region aspect ratio and the obstacle area are observed to have a much larger effect on the wirelength distribution than the obstacle's aspect ratio and location. Accordingly, we suggest that the first two parameters be included as indices of lookup tables in wireload models. Our results provide a foundation for the prediction of various interconnect parameters, which apply to *a priori* wirelength estimation schemes in chip planning tools to improve parasitic estimation accuracy and timing closure; this is particularly relevant for system-on-chip designs where IP blocks are combined with row-based layout.

II. Background and Definitions

The well-known Rent's rule presents a simple empirical power law relationship between the number of terminals T and the number of gates N in a random-logic network [12], [7], [6], and [15]

$$T = kN^p \tag{1}$$

with k the average number of terminals per gate and p the Rent exponent. The Rent exponent is an empirical constant ranging from 0.2 to 1 across different architectures and different placement optimizations [14], [5], [9], and [10]. Microprocessors, gate array architectures, and high performance computers have been reported to have Rent exponent values of 0.45, 0.5, and 0.63, respectively [1]. Circuits under good placement tend to have smaller Rent exponent values, while randomly placed logic networks have Rent exponent $p = 1$ [6].

Rent's empirical relationship forms the foundation of most traditional wirelength estimators. The probability density function $n(\ell)$, defined as the fraction (percentage) of wires with length ℓ, is generally used to express the wirelength distribution [7], [6]. It contains two main parts, a *site function* $f(\ell)$ that enumerates all possible shortest paths of length ℓ between points in a grid and an *occupation probability function* $occ(\ell)$ that assigns to each path a probability to occur depending on its length. With proper normalization, we have [6], [7]

$$n(\ell) = \frac{N(\ell)}{N_{\text{total}}} = \frac{f(\ell)occ(\ell)}{\sum_{\ell=1}^{\ell_{\max}} f(\ell)occ(\ell)} \tag{2}$$

with

$$occ(\ell) \approx p(1-p)2^{p-1}\ell^{2p-4}. \tag{3}$$

The probability density function $n(\ell)$ can then be used to derive various kinds of interconnect parameter estimations. For example, the average wirelength can be obtained as

$$\bar{\ell} = \sum_{\ell} n(\ell)\ell \tag{4}$$

and the probability that all N wires are shorter than ℓ_0 is

$$\text{Prob}(\ell(p) < \ell_0 | \forall p \in P, |P| = N) = \left(\sum_{\ell<\ell_0} n(\ell)\right)^N. \tag{5}$$

Previous publications do not take obstacle effects into account when computing the site function $f(\ell)$. In this paper, we adopt an enumeration technique based on generating polynomials [17] which allows us to augment current wirelength estimation techniques with the analysis of obstacle effects. We also extend previous work [4] which gives only expected average wirelength in the presence of obstacles. In a row-based layout the site function is a discrete distribution and the generating polynomial technique is used to express the site function as a polynomial by using its Z-transform. This corresponds to a summation of $z^{\ell(p)}$ for each path p between two terminals with length $\ell(p)$ over the finite set P of shortest paths between all possible terminal-pairs in the layout. In other words, the site function $f(\ell)$ can be expressed by the generating polynomial

$$V(z) = \sum_{\ell} f(\ell)z^{\ell} = \sum_{p\in P} z^{\ell(p)}. \tag{6}$$

Our work pioneers the distinction between several effects of rectangular routing obstacles on wirelength distribution site functions. We observe that the introduction of an obstacle in a layout has the following effects: 1) an increase of the total layout area with the obstacle area; 2) a reduction of the number of possible terminal-pairs (within the resized layout) by restricting the set of all possible terminal locations to those outside of the obstacle; and 3) an increase in wirelengths because detours are needed around the obstacles. We combine the first two effects into the *terminal redistribution effect* and call the third one a *blockage effect*. We define the following scenarios to screen out each individual effect.

Definition 1—Intrinsic Wires: Intrinsic wires[2] are shortest paths between all possible terminal-pairs in a rectangular array of placement locations without any obstacle.

Definition 2—Point Redistribution Wires: Point redistribution wires are shortest paths between all possible terminal-pairs in a (resized) rectangular array of placement locations with "transparent" obstacles within which terminals cannot be located but through which wires can pass.

Definition 3—Resultant Wires: Resultant wires are shortest paths between all possible terminal-pairs in a (resized) rectangular array of placement locations with opaque obstacles within which terminals cannot be located and through which wires cannot pass.

The difference between redistribution wires and intrinsic wires is due to the *redistribution effect* of the obstacles, and the difference between resultant wires and redistribution wires is due to the *blockage effect*. In the rest of this paper, these

[2]Following virtually all previous literature, we study only two-terminal nets in this paper. Wirelengths of multiterminal nets could be defined as the length of the Steiner minimal tree, minimum spanning tree or another length, depending on the actual router. However, they may not have a closed-form formula. A lookup table of Steiner minimum tree intrinsic lengths is presented in [3] and extended in [2] for a rectangular layout region of arbitrary aspect ratio.

differences are respectively called *redistribution change* and *blockage change*.

Several parameters influence the redistribution and blockage effects in a SOC design: 1) the aspect ratio of the design itself; 2) the number of net terminals; 3) the number of obstacles; 4) the area of obstacles; 5) aspect ratio of obstacles; and 6) locations of obstacles in the design. In the remainder of this paper, we separate these effects and make observations on their impact and significance with respect to wirelength distributions. Section III investigates designs with a single obstacle and studies the influence of the dimension, aspect ratio and location of the obstacle, as well as the shape of the layout region. In Section IV, we extend our analysis to multiple obstacles. Section V presents our conclusions.

III. Single Obstacle

In this section, we analyze an array of $m \times n$ placement locations (with x indexes from 0 to $m-1$ and y indexes from 0 to $n-1$). The distance between two horizontally (vertically) adjacent placement locations is w (h) (see Fig. 2).[3] We evaluate the influence of including a rectangular obstacle spanning between (but not including) x indexes a and b and y indexes c and d ($0 \le a < b \le m-1$ and $0 \le c < d \le n-1$).[4] The inclusion of the obstacle area expands the layout region to an $m' \times n' = m \times n + w_o \times h_o$ region ($w_o = b-a-1$, $h_o = d-c-1$). We assume that the layout region aspect ratio is preserved ($m'/n' = A = m/n$) and that the layout region increases at each obstacle side proportional to the distance between the obstacle side and the layout region side such that the obstacle is relocated between x indexes a', b' and y indexes c', d' in the expanded layout region

$$\begin{aligned} n' &= \text{round}\left(\sqrt{n^2 + \frac{w_o h_o}{A}}\right) \\ m' &= \text{round}\left(\sqrt{m^2 + A w_o h_o}\right) \\ a' &= \text{round}\left(\frac{m' - w_o}{m - w_o} a\right) \\ b' &= a' + w_o \\ c' &= \text{round}\left(\frac{n' - h_o}{n - h_o} c\right) \\ d' &= c' + h_o \end{aligned} \tag{7}$$

where "round" is the rounding operator which preserves integral coordinates but may leave (negligible) rounding errors.

We respectively use polynomials $V_I(m, n, w, h)$, $V_P(m', n', a', b', c', d', w, h)$ and $V_R(m', n', a', b', c', d', w, h)$ to represent the site function of intrinsic, point redistribution and resultant wirelengths, and we calculate these distributions based on the generating polynomials technique [17].

[3]Thus, placement locations are located at absolute coordinates $0, w, 2w, \ldots, (m-1)w$ in the x direction and $0, h, 2h, \ldots, (n-1)h$ in the y direction.

[4]The obstacle spans from $aw+\epsilon$ to $bw-\epsilon$ in the x direction and from $ch+\epsilon$ to $dh-\epsilon$ in the y direction.

A. Theoretical Analysis for Site Functions

1) Intrinsic Wires: A simple example case helps to illustrate the principle of the generating polynomial technique and forms the basis for further analysis. We analyze a one-dimensional (1-D) array of m placement locations with distance w between two neighboring locations. The generating polynomial $V_1(m, w)$ of all site placement locations is found by summing up $z^{\ell(p)}$ for each path p between two terminals with length $\ell(p)$ over all possible terminal-pairs P. This results in[5]

$$\begin{aligned} V_1(m, w) &= \sum_{x_1=0}^{m-1} \sum_{x_2=0}^{m-1} z^{|x_1 - x_2| w} \\ &= \sum_{x_1=0}^{m-1} \left(\sum_{x_2=0}^{x_1} z^{(x_1 - x_2) w} + \sum_{x_2=x_1+1}^{m-1} z^{(x_2 - x_1) w} \right). \end{aligned} \tag{8}$$

Repeatedly using the expression of a geometric series

$$\sum_{i=0}^{n-1} z^i = \frac{z^n - 1}{z - 1} \tag{9}$$

equation (8) yields[6]

$$V_1(m, w) = \frac{2z^{(m+1)w} - m z^{2w} - 2z^w + m}{(z^w - 1)^2}. \tag{10}$$

We next apply the *convolution technique* to derive the site function of intrinsic wires $V_I(m, n, w, h)$ from the 1-D result. The convolution technique of generating polynomials composes paths from smaller paths, each from a "base set." A known property of generating polynomials (and more generally of Z-transforms) is that the polynomial of a convolution is the product of the polynomials of its base sets [17]. In a two-dimensional (2-D) array every shortest path between two terminals is composed of a horizontal segment and a vertical segment (with probable zero length if the two terminals share the same x or y coordinate). Intrinsic wires are, thus, the convolution of two base sets: one of horizontal segments and the other of vertical segments. Hence the polynomial $V_I(m, n, w, h)$ of intrinsic wires is the product of two 1-D site functions. Removing self-connections and double-counting of wires, we obtain

$$V_I(m, n, w, h) = \frac{V_1(m, w) V_1(n, h) - mn}{2}. \tag{11}$$

The distribution of intrinsic placement sites can be found by an inverse Z-transform or, alternatively, by applying the simple conversion formula from [17]

$$\frac{z^n}{(z-1)^i} = \sum_{\ell=0}^{n-i} \binom{n-\ell-1}{i-1} z^\ell + \frac{O(z^{i-1})}{(z-1)^i} \tag{12}$$

[5]There may be more than one way of derivation for any generating polynomial, e.g., by using a convolution of even more primitive base sets corresponding to the generating polynomials of individual cells. In this paper, we follow the derivation as found in [17].

[6]All the polynomial divisions in this paper yield a z expansion with integer coefficients for each term.

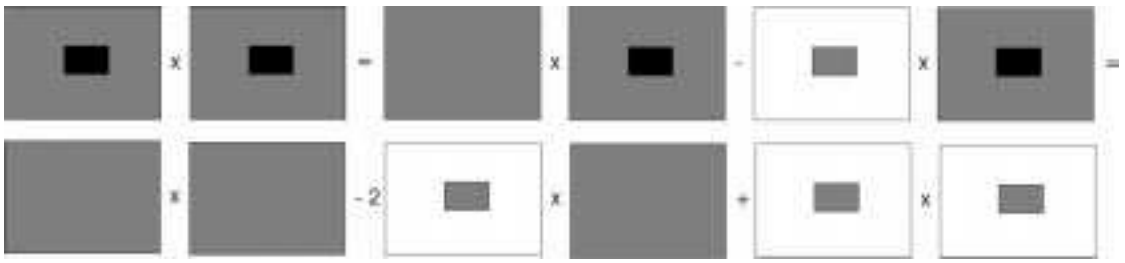


Fig. 1. Composition of the point redistribution polynomials from the intrinsic polynomials (black region denotes the obstacle, gray region contains the terminal sites for enumeration).

with

$$\binom{n-\ell-1}{i-1} = \frac{1}{(i-1)!}\prod_{j=1}^{i-1}(n-\ell-j).$$

Immediate application of (12) to all terms of (11), with the knowledge that all remainder terms $O(z^{i-1})$ vanish because the entire polynomial division does not have a remainder [17] and under the assumption that $w = h = 1$ and that $m \geq n$, results in

$$f_I(\ell) = \begin{cases} f_0(\ell), & (0 \leq \ell \leq n) \\ f_1(\ell), & (n \leq \ell \leq m) \\ f_2(\ell), & (m \leq \ell \leq n+m) \\ 0, & \text{otherwise} \end{cases} \tag{13}$$

with

$$\begin{aligned} f_0(\ell) &= \tfrac{1}{3}\ell(\ell^2-1) + \ell(n(m-\ell)+m(n-\ell)) \\ f_1(\ell) &= \tfrac{1}{3}n(n^2-1) + n^2(m-\ell) \\ f_2(\ell) &= \tfrac{1}{3}(n+m-\ell)^3 - \tfrac{1}{3}(n+m-\ell). \end{aligned}$$

The equations for $n > m$ are found by simply switching n and m in the above equations.

2) Point Redistribution Wires: The point redistribution site density function in the presence of a transparent (for wires) obstacle can be obtained by considering the intrinsic site density function in an $m' \times n'$ layout region and by observing that the enumeration of all paths between terminals located outside of the obstacle can be composed from 1) the enumeration of all paths in the entire region; 2) the enumeration of all paths from the inside of the obstacle to the entire region; and 3) the enumeration of all paths within the obstacle. See Fig. 1, which illustrates the polynomial expansion $(I-\alpha)^2 = I^2 - 2I\alpha + \alpha^2$ and represents the equation

$$\begin{aligned} &V_P(m', n', a', b', c', d', w, h) \\ &\quad = V_1(m', w)V_1(n', h) - 2V_2(a', b', m', w)V_2(c', d', n', h) \\ &\qquad + V_1(b'-a'-1, w)V_1(d'-c'-1, h). \end{aligned} \tag{14}$$

In this equation, $V_2(a, b, m, w)$ represents the polynomial for a distribution of paths between all points of a line segment (a, b) (end points not included) to an enclosing line segment $(0, m)$ with the distance between two points in the lines being w. This polynomial can be easily found to be

$$\begin{aligned} &V_2(a, b, m, w) \\ &\quad = \sum_{x_1=a+1}^{b-1}\sum_{x_2=0}^{m-1} z^{|x_1-x_2|w} \\ &\quad = \Big(z^{(b+1)w} + z^{(m-a)w} - z^{(a+2)w} - z^{(m-b+1)w} \\ &\qquad - (b-a-1)z^{2w} + (b-a-1)\Big)(z^w-1)^{-2}. \end{aligned} \tag{15}$$

Note that in (14), we have to remove self-connections $(-m'n' + (b'-a'-1)(d'-c'-1))$ and double-counting $(/2)$.

The same recipe as in the previous section can be applied by using (12) to convert the above generating polynomial into real space site density functions $f(\ell)$. Here, we present as an example the point redistribution site density function for a square obstacle $(a', m'-a'-1, a', m'-a'-1)$ located at the center of an $m' \times m'$ square layout region (with $w = h = 1$) when $m' \geq 4a' + 4$

$$f_P(\ell) = \begin{cases} f_0(\ell), & (0 \leq \ell \leq a'+1) \\ f_1(\ell), & (a'+1 \leq \ell \leq 2a'+2) \\ f_2(\ell), & (2a'+2 \leq \ell \leq m'-2a'-2) \\ f_3(\ell), & (m'-2a'-2 \leq \ell \leq m'-a'-1) \\ f_4(\ell), & (m'-a'-1 \leq \ell \leq m') \\ f_5(\ell), & (m' \leq \ell \leq 2m'-4a'-4) \\ f_6(\ell), & (2m'-4a'-4 \leq \ell \leq 2m'-2a'-2) \\ f_7(\ell), & (2m'-2a'-2 \leq \ell \leq 2m') \\ 0, & \text{otherwise} \end{cases} \tag{16}$$

with

$$\begin{aligned} f_7(\ell) &= \tfrac{1}{3}(2m'-\ell)^3 - \tfrac{1}{3}(2m'-\ell) \\ f_6(\ell) &= f_7(\ell) - \tfrac{2}{3}(2m'-2a'-2-\ell)^3 \\ &\quad + \tfrac{2}{3}(2m'-2a'-2-\ell) \\ f_5(\ell) &= f_6(\ell) + \tfrac{1}{3}(2m'-4a'-4-\ell)^3 \\ &\quad - \tfrac{1}{3}(2m'-4a'-4-\ell) \\ f_4(\ell) &= f_5(\ell) + \tfrac{2}{3}(m'-\ell)^3 - 2m'(m'-\ell)^2 - \tfrac{2}{3}(m'-\ell) \\ f_3(\ell) &= f_4(\ell) + 4(m'-2a'-2)(m'-a'-1-\ell)^2 \\ f_2(\ell) &= f_3(\ell) - \tfrac{2}{3}(m'-2a'-2-\ell)^3 \\ &\quad + \tfrac{2}{3}(m'-2a'-2-\ell) \\ &\quad - 2(m'-2a'-2)(m'-2a'-2-\ell)^2 \\ f_1(\ell) &= f_2(\ell) - \tfrac{2}{3}(2a'+2-\ell)^3 + \tfrac{2}{3}(2a'+2-\ell) \\ f_0(\ell) &= f_1(\ell) - 4(m'-2a'-2)(a'+1-\ell)^2. \end{aligned}$$

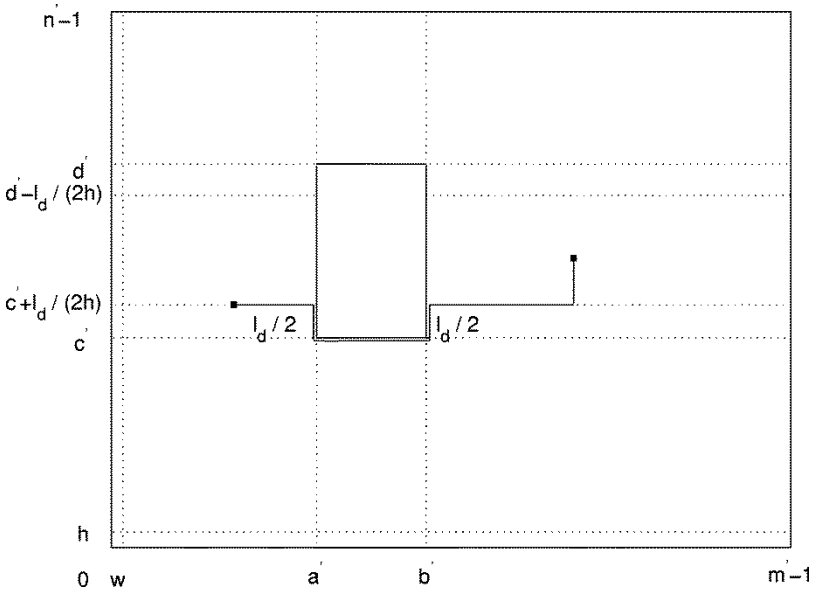


Fig. 2. An array of $m' \times n'$ placement locations with a rectangular obstacle between x indexes a' and b' and between y indexes c' and d'. The distance between horizontally or vertically adjacent cells is w or h, respectively. A horizontal detour of length ℓ_d occurs only with at least one terminal on either y index $c+(\ell_d/2h)$ or $d-(\ell_d/2h)$, and the other terminal between y indexes $c+(\ell_d/2h)$ and $d-(\ell_d/2h)$.

If $m' < 4a' + 4$ the equation changes to

$$f_P(\ell) = \begin{cases} f_0(\ell), & (0 \le \ell \le a'+1) \\ f_1(\ell), & (a'+1 \le \ell \le m'-2a'-2) \\ f_2(\ell), & (m'-2a'-2 \le \ell \le 2a'+2) \\ f_3(\ell), & (2a'+2 \le \ell \le m'-a'-1) \\ f_4(\ell), & (m'-a'-1 \le \ell \le 2m'-4a'-4) \\ f_5(\ell), & (2m'-4a'-4 \le \ell \le m') \\ f_6(\ell), & (m' \le \ell \le 2m'-2a'-2) \\ f_7(\ell), & (2m'-2a'-2 \le \ell \le 2m') \\ 0, & \text{otherwise} \end{cases} \tag{17}$$

with

$$\begin{aligned} f_7(\ell) &= \tfrac{1}{3}(2m'-\ell)^3 - \tfrac{1}{3}(2m'-\ell) \\ f_6(\ell) &= f_7(\ell) - \tfrac{2}{3}(2m'-2a'-2-\ell)^3 \\ &\quad + \tfrac{2}{3}(2m'-2a'-2-\ell) \\ f_5(\ell) &= f_6(\ell) + \tfrac{2}{3}(m'-\ell)^3 - 2m'(m'-\ell)^2 - \tfrac{2}{3}(m'-\ell) \\ f_4(\ell) &= f_5(\ell) + \tfrac{1}{3}(2m'-4a'-4-\ell)^3 \\ &\quad - \tfrac{1}{3}(2m'-4a'-4-\ell) \\ f_3(\ell) &= f_4(\ell) + 4(m'-2a'-2)(m'-a'-1-\ell)^2 \\ f_2(\ell) &= f_3(\ell) - \tfrac{2}{3}(2a'+2-\ell)^3 + \tfrac{2}{3}(2a'+2-\ell) \\ f_1(\ell) &= f_2(\ell) - \tfrac{2}{3}(m'-2a'-2-\ell)^3 \\ &\quad + \tfrac{2}{3}(m'-2a'-2-\ell) \\ &\quad - 2(m'-2a'-2)(m'-2a'-2-\ell)^2 \\ f_0(\ell) &= f_1(\ell) - 4(m'-2a'-2)(a'+1-\ell)^2. \end{aligned}$$

The distributions for rectangular obstacles and/or rectangular layout regions can also be obtained but contain many more regions. Looking at (16) and (17), one truly appreciates the compact generating polynomial representation.

3) Resultant Wires: Resultant wirelengths are obtained by counting the detour length for the corresponding point redistribution wires. We identify the point redistribution wires that need a detour of length ℓ_d and use $V_P^d(\ell_d)$ as the polynomial representation of the distribution of these wires.

Detours can only be needed if the two terminals are located at opposite sides of the obstacle, either one to the left and one to the right of the obstacle, or one below and one above the obstacle. Also, detours are only possible in one direction (x or y). Note that a horizontal detour[7] of length ℓ_d only occurs when at least one terminal of the wire is located at y index $c' + (\ell_d/2h)$ or $d' - (\ell_d/2h)$ (with $\ell_d/2h$ integer) and the other terminal of the wire is located between y indexes $c'+(\ell_d/2h)$ and $d'-(\ell_d/2h)$ (Fig. 2). The situation for a vertical detour is similar. Any horizontal path between terminals that requires a detour can be composed from a path between the left terminal and the obstacle (enumeration of a line of points to the point near the obstacle boundary), a constant length $w_o w$ to cross the obstacle, and a path between the obstacle side and the right terminal (enumeration of a rectangle of points to a corner point). Taking into account: 1) that there are two possible y-indexes for the left terminal and both cases are symmetrical (factor 2); 2) that we have a similar path decomposition if the right terminal is at one of the two y locations; and 3) that, in considering both 1) and 2) together, we double-counted situations with both the left and the right terminal at a fixed y location, we obtain the following polynomial equation for the point redistribution wirelength requiring a horizontal detour of length ℓ_d

$$\begin{aligned} &V_P^{d_h}(\ell_d) \\ &\quad = 2V_3(a', w) z^{w_o w} V_4(m'-b'-1, d'-c'-\ell_d/h, w, h) \\ &\qquad + 2V_3(m'-b'-1, w) z^{w_o w} V_4(a', d'-c'-\ell_d/h, w, h) \\ &\qquad - 2V_3(a', w) z^{w_o w} V_3(m'-b'-1, w) \\ &\qquad - 2V_3(a', w) z^{w_o w} z^{dh-ch-\ell_d} V_3(m'-b'-1, w) \end{aligned} \tag{18}$$

[7]Note that the adjective "horizontal" applies to the wire for which a detour is needed. The actual detour wire will then be vertical (see Fig. 2).

where $V_3(x, w)$ is the polynomial for a line of $x+1$ points (distance x between endpoints) to one of its end points and $V_4(x, y, w, h)$ is the polynomial for a rectangle of $(x+1) \times (y+1)$ points (distances x and y) to one of its corners. These polynomials are given by

$$V_3(x, w) = \sum_{x_1=0}^{x} z^{x_1 w} = \frac{z^{w(x+1)} - 1}{z^w - 1} \tag{19}$$

$$\begin{aligned} V_4(x, y, w, h) &= V_3(x, w) V_3(y, h) \\ &= \frac{z^{w(x+1)} - 1}{z^w - 1} \frac{z^{h(y+1)} - 1}{z^h - 1}. \end{aligned} \tag{20}$$

Equation (18) then results in

$$\begin{aligned} V_P^{d_h}(\ell_d) = 2 &\frac{\left(z^{w(a+1)} - 1\right) z^{w(b-a)} \left(z^{w(m-b)} - 1\right)}{(z^w - 1)^2} \\ &\cdot \frac{\left(z^{h(d-c)-\ell_d} - 1\right)(z^h + 1)}{z^h - 1}. \end{aligned} \tag{21}$$

A similar equation is found for the point redistribution polynomial $V_P^{d_v}$ for wires requiring a vertical detour.

The resultant polynomial for the wires contained in $V_P^d(\ell_d) = V_P^{d_h}(\ell_d) + V_P^{d_v}(\ell_d)$ is given by $z^{\ell_d} V_P^d(\ell_d)$ because all the wires get the additional detour, so that the overall resultant wirelength distribution is represented by the polynomial

$$\begin{aligned} &V_R(m', n', a', b', c', d', w, h) \\ &\quad = V_P(m', n', a', b', c', d', w, h) + \sum_{\ell_d} V_P^d(\ell_d)(z^{\ell_d} - 1) \\ &\quad = V_P(m', n', a', b', c', d', w, h) + V_d(a', b', c', d', w, h) \\ &\qquad + V_d(c', d', a', b', h, w) \end{aligned} \tag{22}$$

with

$$\begin{aligned} &V_d(a, b, c, d, w, h) \\ &\quad = 2 \frac{\left(z^{w(a+1)} - 1\right) z^{w(b-a)} \left(z^{w(m-b)} - 1\right)}{(z^w - 1)^2} \frac{z^h + 1}{z^h - 1} \\ &\qquad \cdot \left(\left(z^{h(d-c)} + 1\right)(d - c) - \frac{z^h + 1}{z^h - 1} \left(z^{h(d-c)} - 1\right) \right). \end{aligned}$$

The site density function can then be obtained using the same recipe as in the previous sections, but it will have many more regions and dependencies on the values of m', n', a', b', c', and d'. The resulting expression is omitted for brevity and because all information is already present in the polynomial form. In Section III-C, we present some numerical examples and make observations regarding the effects of obstacle and layout region aspect ratio on the site functions of intrinsic, point redistribution, and resultant wires.

B. Occupation Probability

The probability density function $n(\ell)$ is obtained by combining the site functions in the previous section with a suitable occupation probability function (2). This could be a uniform occupation probability function $occ(\ell) = 1$ as in some customized circuits where the terminals are equally distributed within the net bounding box [3] or as in Donath's wirelength distribution model [8], or it could be the occupation probability function of (3) if the layout is assumed "Rentian" under placement optimization [6],[8] or it could be an occupation probability function in any other form depending on the actual case.

We note that there is an inconsistency between the "obstacle conscious" site functions and the occupation probability function of (3), which neglects layout region boundary and obstacles. However, several papers have indicated that the effects of the finite size of the floorplan do not seem to have a large effect on the occupation probability as evidenced by the close fit of experimental results to the theoretical predictions. We are confident that the same applies to the effect of the obstacles. Indeed, the occupation probability function (approximation) ℓ^{2p-4} represents the placement optimization assuming that it is only dependent on wirelengths, not on the position of wires in the grid, nor on the fact whether or not the wires are affected by the blockage. If we thus assume a placement that is aware of the obstacle–in the sense that placement is optimized taking into account the increased distances due to detours around the obstacle–we can still apply the conventional occupation probability model. However, our model presents a unique opportunity to compare such an obstacle-aware placement to a placement that is obstacle-blind.[9] Applying the occupation probability to the redistribution wirelength after or before the detour lengths are added (i.e., to the resultant wirelength or to the point redistribution wirelength) makes a lot of difference in the interpretation. In the first case (occupation probability applied to the resultant wirelength distribution) the placement is supposed to be obstacle-aware, in the second case (occupation probability applied to the point redistribution wirelength distribution, then adding the detours) the placement is obstacle-blind.

In Section III-C, we present experimental results combined with two kinds of occupation probability functions: with equally distributed terminals (just the site functions) and with an occupation probability function in the form of ℓ^{2p-4}. [These are just two out of many ways of modeling the behavior of a placement tool. Certainly, some placement applications (e.g., mixed-signal or analog) may be more constrained so that the solutions are less predictable. Also, different tools may have different behaviors, e.g., we may retain the form of ℓ^{2p-4} but with different p values.] Our observations based on numerical analyzes not only verify our theoretical results from the previous section but also provide an alternate and more complete view of the wirelength distributions—this is especially useful since in most cases a theoretical analysis cannot come up with a closed-form expression for the entire analyzed distribution.

C. Numerical Examples and Experimental Observations

1) Experimental Setup: To experimentally verify our theoretical analysis and extend our study to multiple obstacles, we have developed a program to observe wirelength distributions for intrinsic, point redistribution and resultant wires. The program takes as inputs a set of obstacles with their dimensions and

[8]Equation (3) is calculated by applying the *conservation of terminals* technique [7], [6]: applying Rent's rule to an infinite plane of gates and analyzing the connections between a central gate and the boundary gates of a Manhattan disk.

[9]With this, we do not suggest that placement tools would not "see" the obstacle, only that they may not adequately foresee the detours in wirelengths that the obstacle will induce for the routing.

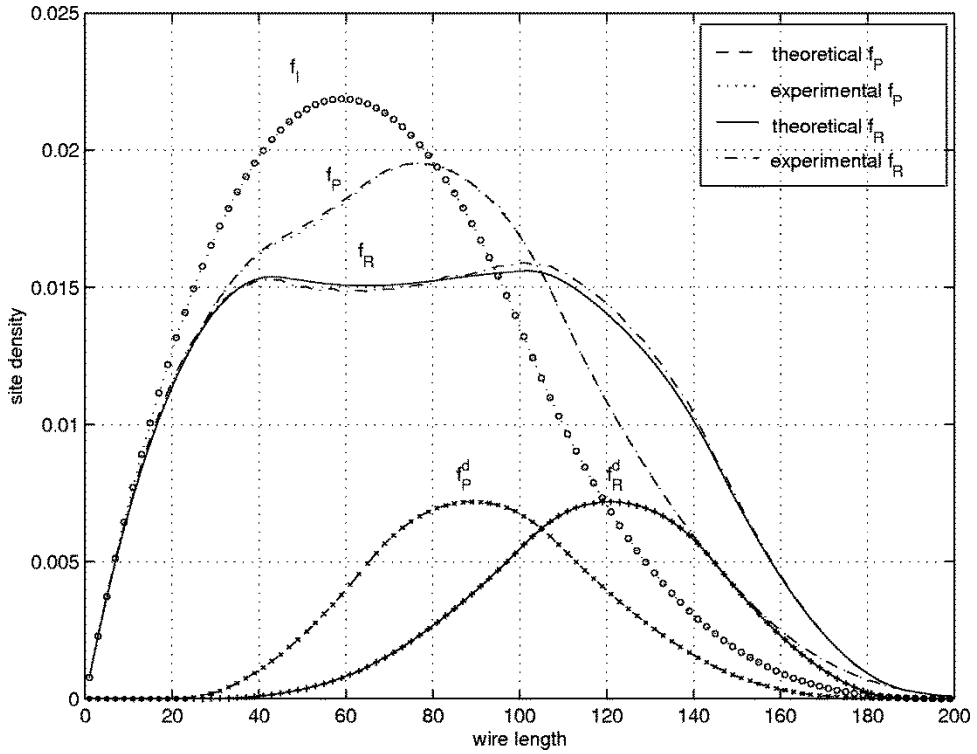


Fig. 3. Site functions with a 20 × 80 obstacle located at the center of the layout region. (a) f_I for intrinsic wires. (b) f_P for point redistribution wires. (c) f_R for resultant wires. (d) $f_P^d = \sum_{\ell_d} f_P^d(\ell_d)$ for the subset of point redistribution wires that need a detour. (e) $f_R^d = \sum_{\ell_d} f_P^d(\ell_d)$ with all wirelengths augmented with ℓ_d for the subset of resultant wires with a detour.

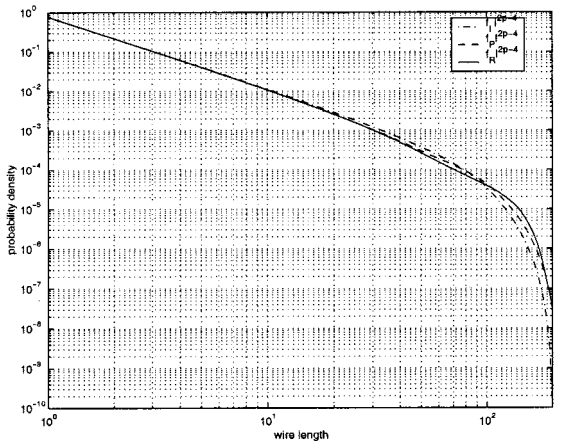
locations as well as the number of net terminals. For calculation of the point redistribution wirelength, obstacles are treated as areas where net terminals are not allowed but wires can pass through. For the calculation of the resultant wirelength, routing is prohibited inside the obstacle areas. The site functions are averaged out over 10000 or more uniformly random terminal sets; the probability density functions are obtained with a ℓ^{2p-4} occupation probability function with Rent exponent $p = 0.6$, unless otherwise indicated.

2) Redistribution and Blockage Effects: As a numerical example we take a 100 × 100 array of placement locations with a 20 × 80 obstacle located at the center of the layout region (i.e., $m = n = 100$, $a = 39$, $b = 60$, $c = 9$, $d = 90$, $w = h = 1$). The site functions of intrinsic, point redistribution and resultant wires obtained from both a theoretical analysis and experimental observations are plotted in Fig. 3. The set of intrinsic wires consists of all the terminal pairs in an $m \times n$ layout region. With a transparent obstacle, some of the intrinsic wires disappear because one of their endpoints was located in the obstacle and others are added because of the increasing layout region. Because the new wires are generally longer than the removed wires, Fig. 3 shows that the f_P curve is completely below and to the right of the f_I curve. When the transparent obstacle becomes opaque, a subset $f_P^d(\ell_d, \ell)$ of the point redistribution wires f_P require a detour of length ℓ_d and become a set of resultant wires $f_R^d(\ell_d, \ell)$ with their length increased by ℓ_d. The resultant wires are obtained by replacing all subsets $f_P^d(\ell_d, \ell)$ of the point redistribution wires by their equivalent subset $f_R^d(\ell_d, \ell)$ of the resultant wires. The area under the curves f_I, f_P and f_R (or the total number of wires) is the same for all cases since the total number of terminal pairs is not changed. The difference of total wirelength (defined as the sum of wirelengths weighted by the number of wires with that wirelength) between the $f_P^d(\ell)$ point redistribution wires and the $f_R^d(\ell)$ resultant wires is the total detour length experienced by point redistribution wires because of the obstacle. In this case, the detour length is 10.2% of the total wirelength for point redistribution wires.

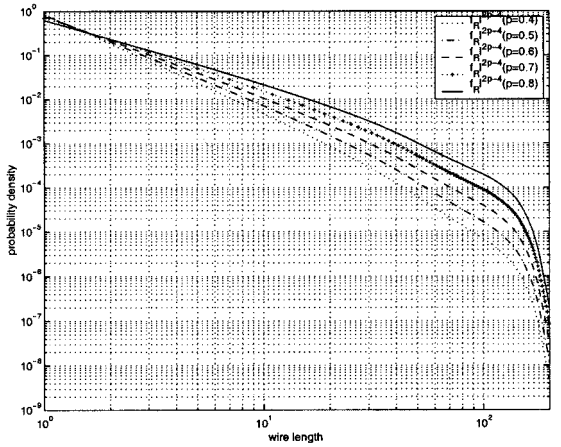
The plots in Fig. 3 also show good agreement between theoretical results and experiments, confirming the analysis in the previous section.

Fig. 4 shows the probability density functions obtained by combination of the above site functions with an occupation probability function ℓ^{2p-4} and appropriate normalization. We plot the site functions for typical Rent exponent values from 0.4 to 0.8. For intrinsic wires with length less than 100, each straight line segment in Fig. 4 represents a power law relationship between probability densities and wirelengths, with its slope rate corresponding to a Rent exponent value. In the presence of a transparent obstacle, it is less probable for the wires with length between 10 and 100 to occur; in the presence of an opaque obstacle, it is even less probable for the wires with length between 40 and 100 to occur, but more probable for longer wires to occur. For a larger Rent exponent value, it is more probable for longer wires to occur, so there is a larger blockage effect and a larger redistribution effect.

In the following sections, we study the effects of obstacle dimension, obstacle location, and layout region aspect ratio on wirelength distributions.

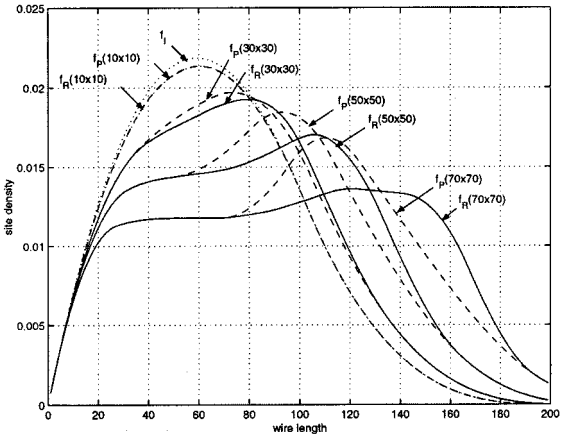


(a)

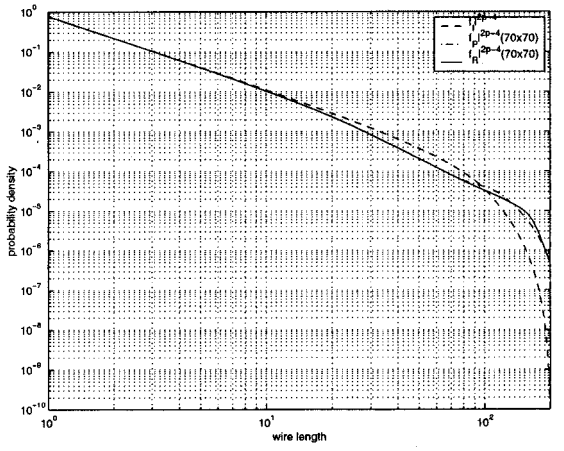


(b)

Fig. 4. Probability density functions of intrinsic, point redistribution and resultant wires with Rent exponent $p = 0.6$ (a) and probability density functions of resultant wires with Rent exponent $p = 0.4$ to 0.8 (b) in the presence of a 20×80 obstacle located at the center of the layout region.



(a)



(b)

Fig. 5. Site functions (a) and probability density functions (b) with different obstacle dimensions, where $f_P(w_o \times h_o)$ and $f_R(w_o \times h_o)$ respectively denote the probability density functions of the point redistribution and the resultant wires in the presence of a $w_o \times h_o$ obstacle located at the center of the layout region.

3) Effect of Obstacle Area: We assume a square obstacle in the center of a 100×100 region and change the obstacle area while observing the wirelength distribution. The resultant wirelength site functions are plotted in Fig. 5(a) . A larger obstacle brings a larger redistribution effect; of the point redistribution wires more are blocked by the obstacle and longer detours are taken, resulting in a larger blockage effect. The blockage effect of a large obstacle flattens the wirelength distribution, resulting in a relatively constant number of wires within a wide range of lengths. For example, we see that in the presence of a 70×70 obstacle, the number of resultant wires remains at about 1.2% with resultant wirelength between 15–145, while the number of point redistribution wires varies from about 1.3% with length 65 to about 1.7% with length 110.

Observation 1: A larger obstacle area not only yields a larger redistribution effect, but also a larger blockage effect, with more wires taking a longer detour.

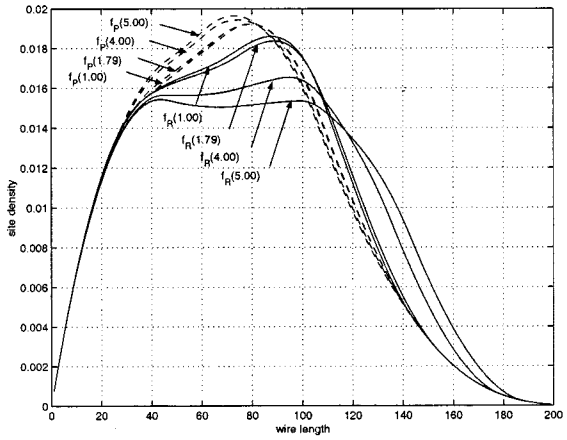
Fig. 5(b) shows the wirelength probability density functions. There is a considerable redistribution effect, effectively resulting in a smaller Rent exponent for wires with length between 10–100. The blockage effect is significant for very large obstacles, and extends the power law relationship between probability density and wirelength to longer wires.

4) Effect of Obstacle Aspect Ratio: In our next experiment we study obstacles with different aspect ratios but identical area, centered at $(50, 50)$ of a 100×100 region. The site functions are plotted in Fig. 6 with four obstacles of dimensions 36×36, 48×27, 72×18 and 81×16. With a high obstacle aspect ratio, there are more short and less long point redistribution wires; and more long and less short resultant wires. This is not surprising because an obstacle with a higher aspect ratio will cover more long intrinsic wires (thus reducing the point redistribution effect), and there will be more point redistribution wires taking longer detours resulting in a larger blockage effect.

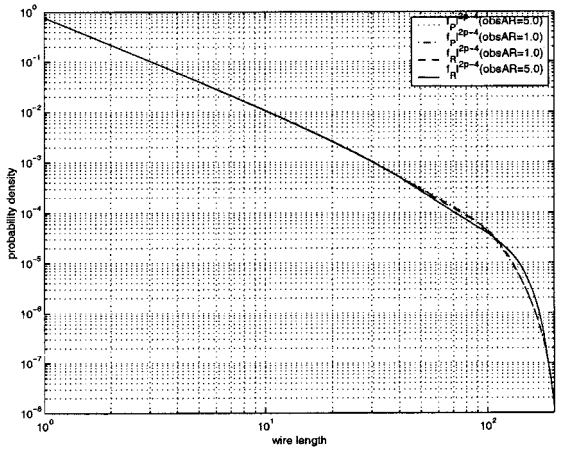
Fig. 6(b) shows that the probability density function for point redistribution wires does not change with obstacle aspect ratio and there is only a slight change for resultant wires.

Observation 2: High obstacle aspect ratios shorten point redistribution wires slightly and lengthen resultant wires.

5) Effect of Obstacle Location: We study the effect of obstacle displacement on the wirelength distribution by moving a 50×50 obstacle from the center of the layout region toward the boundary of the layout region. As the obstacle approaches the boundary of the layout region, more point redistribution wires are of smaller length, but the blockage effect does not change

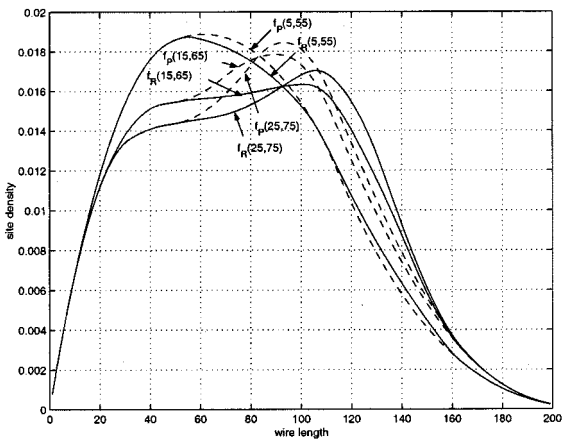


(a)

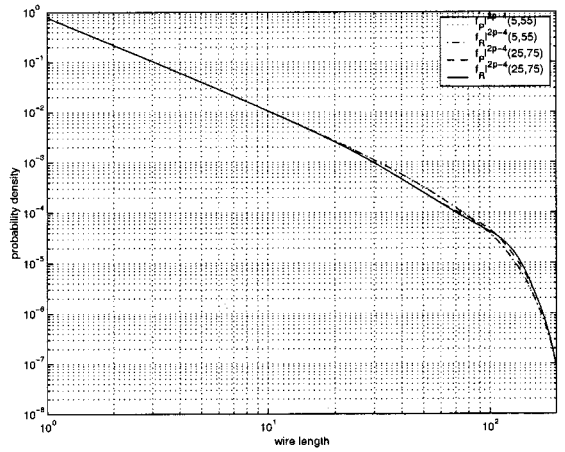


(b)

Fig. 6. Site functions (a) and probability density functions (b) with different obstacle aspect ratio. $f_P(a)$ and $f_R(a)$, respectively, denote the site functions for point redistribution and resultant wires in the presence of an obstacle located at the center of the layout region with area 1296 and aspect ratio a. The f_P and f_R curves at (a) are keyed in pairs; the f_P curve is always "above and to the left of" its f_R counterpart.



(a)



(b)

Fig. 7. Site functions (a) and probability density functions (b) with obstacle displacement. $f_P(a\times b)$ and $f_R(a\times b)$, respectively, denote the site functions of point redistribution and resultant wires in the presence of an obstacle spanning between x indexes a and b

much [Fig. 7 (a)]. The probability density function curves of all obstacle locations superpose with each other, implying that obstacle displacement has a negligible effect on probability density functions.

Observation 3: Obstacle displacement from the center of the layout region shortens point redistribution wires, but makes no considerable change on blockage effect. The overall effect of obstacle displacement is negligible for probability density functions.

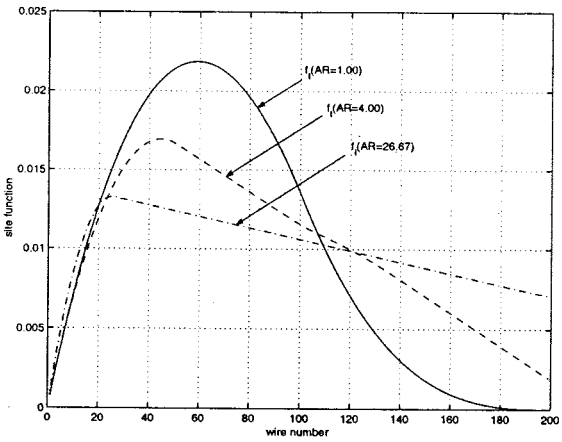
6) Effect of Layout Region Aspect Ratio: The aspect ratio of the layout region has significant impact on the site functions. We keep a 20×10 obstacle at the center of the layout region and compare three layout regions with identical area but different aspect ratios.[10] The resultant site functions in Fig. 8 show that a higher layout region aspect ratio increases the maximum wirelength and lengthens the wires significantly. However, the areas under the curves in Fig. 8 are the same, since they are the number of the intrinsic wires in several layout regions with identical area. It is less probable for the wires with length between 10–100 to occur, but more probable for the longer wires to occur [Fig. 8 (b)].

Observation 4: A high layout region aspect ratio increases the maximum wirelength and lengthens the wires; middle-length wires are less probable, while long wires are more probable.

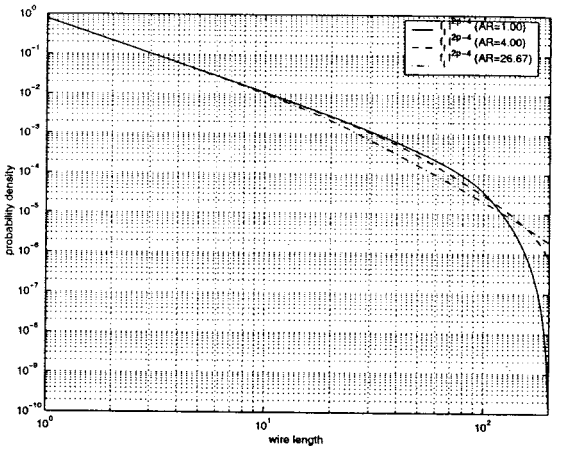
7) Analysis of Wirelength Distribution in L- and C-Shaped Regions: L-shaped and C-shaped layout regions are quite common in system-on-chip designs in the presence of large IP blocks. Wirelength distributions in these layout region shapes can be studied by viewing the shapes as rectangles with rectangular obstacles on their boundary. Their point redistribution wires can still be expressed using the same polynomial given in (14). However, we must derive new expressions for resultant wires of the C-shaped layout region,[11] since the boundary of the layout region blocks one side of the obstacle and all the detours go around the obstacle on the other side, resulting in a much larger blockage effect. Consider an obstacle spanning between x indexes a', b' and y indexes c', $m'-1$. It touches

[10]A 20×10 obstacle is chosen to minimize the effect of obstacle. In Fig. 8, the probability density function curves of intrinsic, point redistribution and blockage wires superpose with each other, showing little redistribution and blockage effect.

[11]No detour occurs in an L-shaped layout region.



(a)



(b)

Fig. 8. Site functions. (a) Probability density functions. (b) With different layout region aspect ratios.

the top boundary of the $m' \times n'$ layout region so no wire can go above the obstacle. A pair of points on either side of the obstacle will take a horizontal detour of length ℓ_d only when at least one terminal of the wire is located at y index $c' + (\ell_d/2h)$. The site function for point redistribution wires with horizontal detour of length ℓ_d, which we denote by $V_P^{cd_h}(\ell_d)$, is given by

$$V_P^{cd_h}(\ell_d) = \left(2\frac{z^{(n'-c')h-\ell_d}-1}{z^h-1} - 1\right) \cdot \frac{(z^{(a'+1)w}-1)(z^{(m'-b')w}-1)z^{(b'-a')w}}{(z^w-1)^2}. \quad (23)$$

There is no vertical detour in this C-shaped region.

The overall resultant wirelength distribution is presented by the polynomial

$$\begin{aligned} V_R^c(m', n', a', b', c', w, h) &= V_P(m', n', a', b', c', w, h) + \sum_{\ell_d} V_P^{cd_h}(\ell_d)(z^{\ell_d}-1) \\ &= V_P(m', n', a', b', c', w, h) + V_d^c(a', b', c', w, h) \end{aligned} \quad (24)$$

with

$$\begin{aligned} V_d^c(a, b, c, w, h) &= \left(1+\frac{2}{z^h-1}\right)\left(2(n'-c'-1) - z^h\frac{z^{2h(n'-c'-1)}-1}{z^h-1}\right) \\ &\quad + \frac{2z^{h(n'-c')}}{z^h-1}\left(2(n'-c'-1) + \frac{z^{-2h(n'-c'-1)}-1}{z^h-1}\right). \end{aligned}$$

There is a similar equation for C-shaped region with only vertical detour, where the obstacle is on the left or right boundary of the layout region.

Fig. 9 gives a simple verification of the above expressions for an obstacle spanning between x indexes (24, 75) and y indexes (49, 100) on the top boundary of the 100×100 layout region (i.e., $m = n = 100$, $a = 24$, $b = 75$, $c = 49$). The good agreement between experimental and theoretical site functions for the point redistribution and resultant wires shows the correctness of the above theoretical analysis.

IV. Multiple Obstacles

Consider an $m \times n$ array of placement locations in the presence of a set of k obstacles, each of area s_i and between x indexes a_i, b_i, and y indexes c_i, d_i, where the distance between horizontally (vertically) adjacent placement locations is w (h). In this section, we extend our theoretical analysis in the previous section to this multiple obstacle case.

A. Point Redistribution Wires

The theoretical analysis for point redistribution wires in Section III-A2 can be applied to multiple obstacle cases in much the same way. By distinguishing the intrinsic wires either starting from or ending inside an obstacle and following the polynomial expansion $(I - s_1 - s_2 \cdots - s_k)^2 = I^2 - 2\sum_i Is_i + \sum_i \sum_j s_i s_j$, point redistribution wires are presented by

$$\begin{aligned} V_P(m', n', a'_1, b'_1, c'_1, d'_1, \ldots, a'_k, b'_k, c'_k, d'_k, w, h) &= V_1(m', w)V_1(n', h) \\ &\quad - 2\sum_{i=1}^{k} V_2(a'_i, b'_i, m', w)V_2(c'_i, d'_i, n', h) \\ &\quad + \sum_{i=1}^{k}\sum_{j=1}^{k} V_5(a'_i, b'_i, a'_j, b'_j, w)V_5(c'_i, d'_i, c'_j, d'_j, h) \end{aligned} \quad (25)$$

with

$$V_5(a'_i, b'_i, a'_j, b'_j, w) = \sum_{x_1=a'_i+1}^{b'_i-1} \sum_{x_2=a'_j+1}^{b'_j-1} z^{|x_1-x_2|w}.$$

Removing self-connections and double-counting completes the derivation.

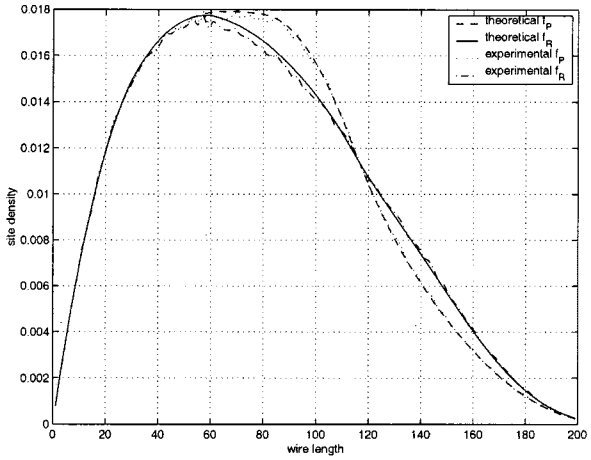


Fig. 9. Experimental verification of the site functions for point redistribution and resultant wires in a C-shaped layout region.

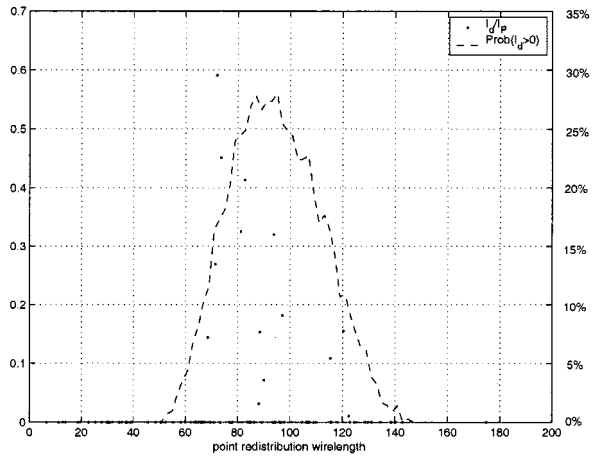


Fig. 10. Detour for different point redistribution wirelengths: each dot is the ratio of detour length ℓ_d over point redistribution wirelength l_P of an individual wire, which values are shown on the left side; the dashed line is percentages of wires that take detour for each point redistribution wirelength, which values are shown on the right side.

B. Resultant Wires

The resultant wires are more complicated to calculate. If we assume that neither the x- nor the y-spans of the obstacles overlap, then wires can only be blocked by a single obstacle at a time and the resultant wires are presented by

$$\begin{aligned} V_R(m', n', a'_1, b'_1, c'_1, d'_1, \ldots, a'_k, b'_k, c'_k, d'_k, w, h) \\ = V_P(m', n', a'_1, b'_1, c'_1, d'_1, \ldots, a'_k, b'_k, c'_k, d'_k, w, h) \\ + \sum_{i=1}^{k} V_d(m', n', a'_i, b'_i, c'_i, d'_i, w, h) \end{aligned} \tag{26}$$

with V_d the same expression as in Section III-A3.

We say that the blockage effect is *additive* and we can treat this special case as a combination of single obstacle problems. However, in the general case, the nonoverlapping assumption does not hold and the blockage effect will be smaller if there is any overlap between obstacles. The exact blockage effect requires a more complicated calculation but the expression above can serve as an upper bound of estimation. In [4], we studied the error made by using the equation under the assumption of additive blockage effects for general cases.

V. Conclusion

The inclusion of IP blocks in SOC design potentially has large effects on the wirelengths in the rest of the design. For example, in Fig. 10, a 50×50 obstacle centered in a 100×100 square routing region accounts for up to 30% wires that take a detour.[12] The detour wirelength can go up to 60% of the original length, showing a significant blockage effect for these wirelengths. In this paper, we have studied both the effect of redistributing net terminals outside of obstacle regions and the detours that wires have to make due to the obstacles. Several parameters influence the effects: the aspect ratio of the design, the dimensions and location of the obstacle(s), the number of obstacles, and the number of net terminals.

[12]This is for site density functions only. The occupation probability effect is not included.

We have derived theoretical expressions for wirelength distributions by applying the generating polynomials technique. The results provide us with a good framework for studying the effect of layout region aspect ratio, obstacle area, obstacle aspect ratio, and obstacle displacement on wirelength distributions. We observe that only layout region aspect ratio and obstacle area have a considerable effect on wirelength distributions. We also separate the effect of obstacles into two parts: a terminal redistribution effect and a blockage effect. The blockage effect only occurs for wires with length comparable to the obstacle dimension and is negligible for most cases. Our theoretical analysis and experiments lead to four observations presented in the paper which can be used to guide physical design. Smaller wirelengths are expected when the routing obstacles are smaller, do not have high aspect ratios, and are located away from the center of the layout region. Wirelengths are also smaller when the layout region does not have a high aspect ratio. A large IP block in a SOC design would lengthen interconnects and affect design performance. The IP blocks are suggested to have comparable size and aspect ratio with that of the layout region; they should be away from the center of the layout region and avoid touching the boundary of the layout region. We believe that these observations provide a clear understanding of the effects of obstacle and layout region aspect ratio, help us in finding equivalent obstacle models for a group of small obstacles or an obstacle with irregular shape, and can form the foundation of efficient and accurate wirelength estimation schemes.

Wireload models have been widely adopted to provide *a priori* interconnect parameter estimates, but their poor accuracy has been detrimental to convergence of modern design methodologies. Of course, a basic reason for inaccuracy is that there are too many unknown factors affecting the outcome of a wireload model, which need to be taken into account by the model. Our study in this paper suggests that two more parameters be included as indexes of lookup tables in wireload models: the layout regions aspect ratio, and the obstacle area

(obstacle aspect ratio and obstacle location are negligible). Our results suggest that this will lead to more accurate and effective wireload models.

Our ongoing research on this topic concentrates on such issues as the following.

1) For large obstacles, a lot of detours follow the obstacle boundary but these wires are not infinitely thin (as we implicitly assumed). The real detour will hence be longer than the one we consider in this paper.
2) The capacity of a small region in between two obstacles or an obstacle and the design boundary is limited and prohibits some detours from being routed through this region. These wires have to be routed at the other side of the obstacle, again increasing the actual detour needed.

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