Submitted to IEEE Trans. on CAD

An Analytical Delay Model for RLC Interconnects *

Andrew B. Kahng and Sudhakar Muddu
UCLA Computer Science Department, Los Angeles, CA 90095-1596 USA
abk@cs.ucla.edu, sudhakar@cs.ucla.edu

Abstract

Elmore delay has been widely used to estimate the interconnect delays in the performance-driven synthesis and layout of VLSI routing topologies. For typical *RLC* interconnections, Elmore delay can deviate significantly (by up to 33% or more) from SPICE-computed delay, since it is independent of inductance. Here, we develop an analytical delay model based on first and second moments to incorporate inductance effects into the delay estimate for interconnection lines. Delay estimates using our analytical model are within 10% of SPICE-computed delay across a wide range of interconnect parameter values. We also extend our delay model for estimation of source-sink delays in arbitrary interconnect trees. Even for the small tree topology considered, we observe significant improvement of at least 20% in the accuracy of delay estimates when compared to the Elmore model, even though our estimates are as easy to compute as Elmore delay. The speedup of delay estimation via our analytical model is several orders of magnitude compared to simulation methodology such as SPICE.

1 Introduction

Accurate calculation of propagation delay in VLSI interconnects is critical to the design of high speed systems. With the evolution of VLSI technology, transmission line effects now play an important role in determining interconnect delays and system performance. Various techniques have been proposed for the delay analysis of interconnects. These techniques are based on either *simulation techniques* or (closed-form) *analytical formulas*. Simulation tools such as SPICE give the most accurate insight into arbitrary interconnect structures, but are computationally expensive. Transient simulation of lossy interconnects based on convolution techniques is presented in [8, 13]. Faster techniques based on moment computations are proposed in [11, 12, 17, 19]. Since these methods are too expensive to be used during iterative layout optimization, the Elmore delay [2] approximation (which represents the first moment of the transfer function) is the most widely

*This work was supported by NSF grant MIP-9257982.

used delay model in the performance-driven design of clock distribution and Steiner global routing topologies. However, Elmore delay cannot accurately estimate the delay for RLC interconnect lines, i.e., the representation for interconnects whose inductive impedance[1] cannot be neglected [4]. To see the effect of inductance impedance on the response, consider a 2-port model for an interconnect driven by a step input with finite source impedance. Figure 1 compares the RC and RLC line responses computed by SPICE3e: 90% threshold delay is 288 ps for the RLC model, but is 358 ps for the RC model. Elmore delay, which does not depend on line inductance, will yield the same delay estimate of 386 ps for both the RC and the RLC cases. More generally, the Elmore delay formula gives good estimates if the interconnect lines are RC or overdamped, but gives overestimates for RLC or underdamped interconnects. This inaccuracy can be harmful for current performance-driven routing methods which try to optimize interconnect segment lengths and widths (as well as drivers and buffers).

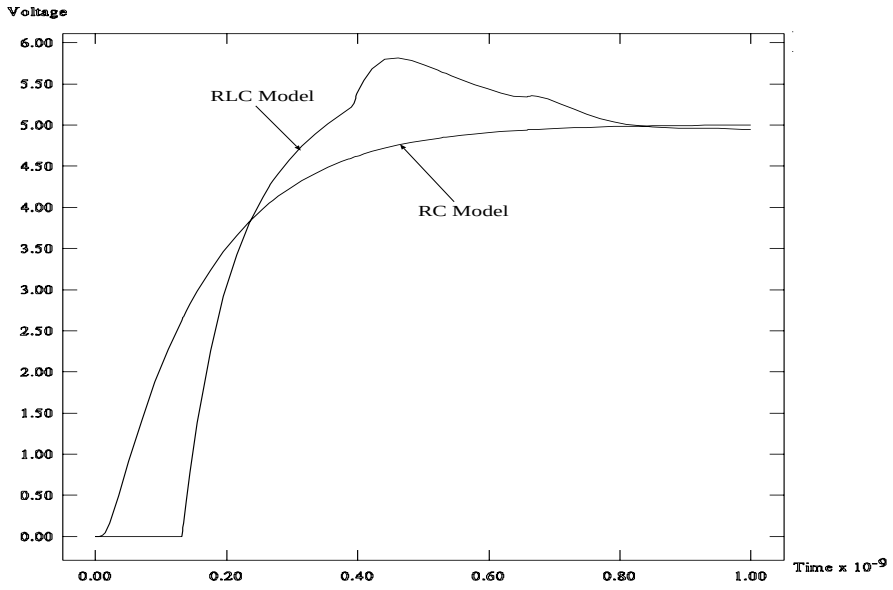

Figure 1: Comparison of SPICE3e responses at the end of an interconnect line driven by a step input and terminated with a capacitive load using both RC and RLC 2-port models. The 90% threshold delay for the RLC model is 288 ps, and for the RC model the delay is 358 ps. The driver resistance is 10.0 Ω and the load capacitance at the end of the line is 2.0 pF. The interconnect line parameters are $R = 0.075\ \Omega/\mu m$, $L = 0.123\ pH/\mu m$, $C = 8.8\ fF/\mu m$; the length of the line is 400 μm.

This paper gives a new and accurate *analytical* delay estimate for distributed RLC interconnects which considers the effect of inductance. Previous moment-based approaches (e.g.,

[1] Inductive impedance is $2\pi fL$, where f is the frequency of operation.

[9, 11, 8]) can compute a delay estimate only from a simulated response but not from an analytical formula. To experimentally validate our analysis and delay formula, we model VLSI interconnect lines having various combinations of source and load parameters, and obtain delay estimates from SPICE, Elmore delay and the proposed analytical delay model. The delay estimate using SPICE is extracted from a computed response at the desired node, whereas the other two models are analytical (closed-form) expressions. Over our range of test cases, Elmore delay estimates can be as much as 50% from the SPICE-computed delays, while our analytical delay model estimates are within 15% of SPICE delays. We also extend our delay model to estimate source-sink delays in arbitrary interconnect trees. For the small tree topology considered, delay estimates using our analytical model are within 15% of SPICE-computed delays. While Elmore delay estimates vary by as much as 35% from the SPICE-computed delays. Since our analytical model has the same time complexity as the Elmore model, we believe that it can be useful in present-day performance-driven routing methodologies.

The organization of our paper is as follows. In Section 2 we discuss previous analytical delay models for distributed interconnect lines. Section 3 presents a new analytical delay model model for a distributed RLC line, and finally Section 4 extends our delay model for interconnection trees.

2 Previous Analytic Delay Models

The transfer function of an RLC interconnect line with source and load impedance (Figure 2) can be obtained using the ABCD parameters [1] as

$$H(s) = \frac{V_2(s)}{V_0(s)} = \frac{1}{\left[\cosh(\theta h) + \frac{Z_S}{Z_0}\sinh(\theta h)\right] + \frac{1}{Z_T}\left[Z_0 \sinh(\theta h) + Z_S \cosh(\theta h)\right]} \tag{1}$$

where $\theta = \sqrt{(r + sl)sc}$ is the propagation constant and $Z_0 = \sqrt{\frac{R+sL}{sC}}$ is the characteristic impedance; $r = \frac{R}{h}, l = \frac{L}{h}, c = \frac{C}{h}$ are resistance, inductance, and capacitance per unit length and h is the length of the line. To compute the RLC line response from the transfer function, the method of Padé approximation has been used by, e.g., [9, 10]. The output transfer function is expanded into a Maclaurin series of s around $s = 0$, and the series is truncated to desired order.[2]

[2] The work of [8] used a recursive convolution based approach and expanded the admittance and the propagation coefficient term around $s = \infty$.

In general, analytical computation of the exact voltage response is very tedious and is usually in the form of an infinite series.

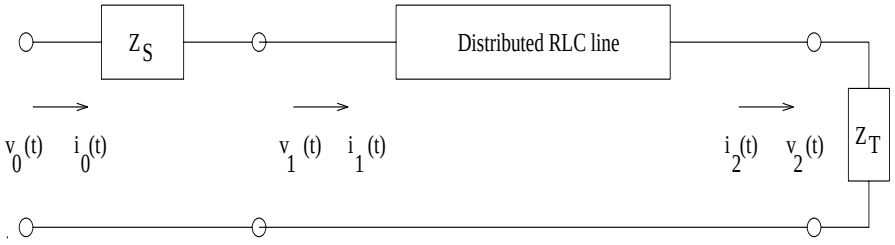

Figure 2: 2-port model of a distributed RLC line with source impedance Z_S and load impedance Z_T.

Efficient delay estimates for RC lines are typically derived by considering a single interconnect line with resistive source and capacitive load impedances; delay formulas for an interconnect tree entail recursive application of the formula for a single line. The analytical Elmore delay [2] estimate, Sakurai's heuristical delay formula [15, 16] and single pole delay estimates of [3] have been widely used.

- Elmore delay is defined to be the first moment of the system impulse response, i.e., the coefficient of s or the first moment in the system transfer function $H(s)$. Applying this definition to $H(s)$ in Equation (1) and considering a source resistance R_S and a capacitive load C_T, the Elmore delay for a distributed RC or RLC line model is

$$T_{ED} = R_S(C + C_T) + R(\frac{C}{2} + C_T) \quad (2)$$

  By considering only one pole in the transfer function, i.e, approximating the denominator polynomial to only first moment, the single pole response can be obtained as in [3]. The single pole of the transfer function is equal to the inverse of the Elmore delay T_{ED}. Hence, the delay at arbitrary thresholds of the single pole response can be directly related to Elmore delay (Elmore delay actually corresponds to the 63.2% threshold voltage of the single pole response). For example, delay at 90% threshold voltage is

$$T_{0.9} = 2.3 * T_{ED} = 1.15RC + 2.3\,(R_S(C + C_T) + RC_T) \quad (3)$$

- Sakurai [15] also gave response and delay calculations for the distributed RC line. He calculates the time-domain response from the transfer function using the Heaviside expansion

over poles of the transfer function. Then, he approximates the response using a single pole and observes the variation of delay with respect to source and load parameters; a 90% threshold delay estimate is *heuristically* obtained as

$$T_{0.9}(h) = 1.02RC + 2.3\,(R_S(C + C_T) + RC_T)$$

Note that Sakurai's heuristic delay formula is almost identical to the Elmore delay equation (3). In this paper, to compute the 90% threshold delay according to the Elmore model we apply Equation (3). Since these single pole delay estimates cannot accurately estimate delay for RLC interconnects, Zhou et al. [19] proposed a two-pole approximation for the transfer function to compute the *response* at the load for RLC interconnection trees. However, this technique is based on response computation and does not provide any analytical expression for delay; it is too time-consuming to be used in iterative optimization of layout. Recently, [7] proposed to improve the Elmore delay model by using higher-order moments; this work gave a heuristic net delay model equal to the sum of the first moment (M_1) and its standard deviation.[3]

3 A New Analytical Delay Model

We now develop a simple closed-form delay estimate, based on first and second moments, which considers the effect of inductance. To our knowledge, this is the first analytical delay model which handles arbitrary threshold voltages and inductance effects for a distributed line. We give experimental confirmation via 90% threshold delay estimates[4] which we compare against SPICE output.[5]

We model an arbitrary interconnect line as follows: (i) the source is modeled as a resistive and inductive impedance ($Z_S = R_S + sL_s$), and (ii) the load at the end of the interconnect line is modeled using capacitive impedance. Thus, the transfer function for the interconnect line of

[3]Standard deviation is equal to $\sigma = \sqrt{|M_1^2 - M_2|}$. In the early drafts of our paper [6] we also considered exactly the same model; however, it turns out that this model is not accurate for various source and load parameters, as discussed in detail by [6]. The full version of our paper [6] studies various combinations of first and second moments, of which the analytical model described here performs best.

[4]Our analytical model extends to any threshold delays; we simply give the derivation for 90% delay threshold.

[5]SPICE simulation results are obtained using SPICE3 and the built-in LTRA (lossy transmission line) model, which is based on convolution techniques [13].

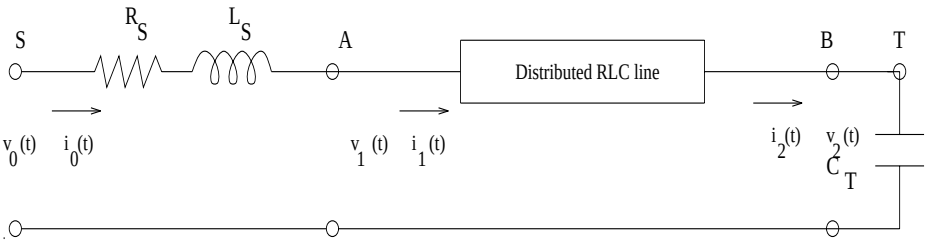

Figure 3: 2-port model of a distributed RLC line with resistive and inductive source impedance, and capacitive load impedance.

Figure 3 is

$$H(s) = \frac{1}{\cosh(\theta h)\left(1 + \frac{Z_S}{Z_T}\right) + \sinh(\theta h)\left(\frac{Z_S}{Z_0} + \frac{Z_0}{Z_T}\right)}$$

where $Z_T = \frac{1}{sC_T}$, $Z_S = R_S + sL_S$, $Z_0 = \sqrt{\frac{R+sL}{sC}}$ and $\theta h = \sqrt{(R+sL)sC}$. We truncate this transfer function by expanding the hyperbolic functions around $s = 0$; expansion around $s = \infty$ is not necessary since we consider only the first few coefficients of the transfer function. I.e., expanding *cosh* and *sinh* as infinite series and collecting terms up to the coefficient of s^2 in the denominator, we obtain the truncated transfer function

$$H(s) \approx \frac{1}{1 + sb_1 + s^2 b_2}$$

with coefficients

$$\begin{aligned} b_1 &= R_S C + R_I C_T + \frac{RC}{2} + RC_T \\ b_2 &= \frac{R_S RC^2}{6} + \frac{R_S RCC_T}{2} + \frac{(RC)^2}{24} + \frac{R^2 CC_T}{6} + L_S C + L_S C_T + \frac{LC}{2} + LC_T \end{aligned} \tag{4}$$

Note that the first and second moments of the transfer function can be obtained from the coefficients b_1 and b_2, i.e., $M_1 = b_1$ and $M_2 = b_1^2 - b_2$. We use the coefficient notation b_1, b_2 and the moment notation M_1, M_2 interchangeably according to the simplicity of the expression. Depending on the sign of $b_1^2 - 4b_2$, the poles of the transfer function can be either real or complex. We separately derive our delay model from the two-pole response for each of these cases.

Real Poles:

The two-pole methodology [6, 19] yields the following response for the case of real poles:

$$v(t) = V_0(1 - \frac{s_2}{s_2 - s_1}e^{s_1 t} + \frac{s_1}{s_2 - s_1}e^{s_2 t})$$

Source		**Load**	**Delay from Response**	**Analytical Delay Models**	
R_S	L_S	C_T	**SPICE**	**Elmore**	**New Model**
Ω	pH	pF	ps	ps	ps
50	2.46	0.176	22.33	22.93	22.21
100	2.46	0.176	45.30	45.20	45.70
500	2.46	0.176	224.50	223.50	228.95
1000	2.46	0.176	446.20	446.4	457.46
25	2.46	1.76	107.10	108.40	108.65
50	2.46	1.76	210.10	210.80	214.74
100	2.46	1.76	415.20	415.40	425.10
500	2.46	1.76	2052.60	2053.0	2103.68
1000	2.46	1.76	4099.50	4100.0	4101.30

Table 1: 90% threshold voltage delay estimates for combinations of source and load parameters for which the poles of the response are real (i.e., overdamped response). The interconnect line parameters are $R = 0.015\ \Omega/\mu m$, $L = 0.246\ pH/\mu m$ and $C = 0.176\ fF/\mu m$ and the length of the interconnect is 100 μm.

where

$$s_{1,2} = \frac{2}{-M_1 \pm \sqrt{4M_2 - 3M_1^2}} = \frac{-b_1 \pm \sqrt{b_1^2 - 4b_2}}{2b_2}$$

The condition for the poles to be real is $(4M_2 - 3M_1^2) = (b_1^2 - 4b_2) \geq 0$. Since $s_2 - s_1 = -\frac{\sqrt{b_1^2-4b_2}}{b_2}$ is negative, the coefficients $\frac{s_2}{s_2-s_1}$ and $\frac{s_1}{s_2-s_1}$ are positive. Also, since the magnitude $|s_2|$ is greater than $|s_1|$, the second term in the time-domain response decreases rapidly compared to the first term. Hence, the two-pole response can be approximated (lower-bounded) as

$$v(t) \approx V_0(1 - \frac{s_2}{s_2 - s_1} e^{s_1 t})$$

Since the voltage is lower-bounded, the delay obtained is an upper bound on the actual delay. The delay τ_r (the subscript indicates the case of real poles) at threshold voltage v_{th} can be obtained via

$$s_1 \tau_r = \ln\left(\frac{(s_2 - s_1)(1 - v_{th})}{s_2}\right) = -\ln\left(\frac{1}{2(1 - v_{th})}[1 + \frac{b_1}{\sqrt{b_1^2 - 4b_2}}]\right)$$

Letting $K_r = \ln\left(\frac{1}{2(1-v_{th})}[1 + \frac{b_1}{\sqrt{b_1^2-4b_2}}]\right)$, we have

$$\tau_r \quad = \quad \frac{K_r}{|s_1|} = K_r \frac{M_1 + \sqrt{4M_2 - 3M_1^2}}{2} = K_r \frac{2b_2}{b_1 - \sqrt{b_1^2 - 4b_2}}$$

i.e., K_r is a function of the coefficients b_1 and b_2. For the wide range of source, load and interconnect parameter values considered in our simulations (see Table 1), we find that K_r is actually almost a constant: the plot on the left side of Figure 4 shows the linear regression used to find the value $K_r = 2.36$ which gives a very strong fit between SPICE delay values and $\frac{1}{|s_1|}$. The variation of K_r with the quantity $X = \frac{b_2}{b_1^2}$ is further discussed in [6]. Thus, we use

$$\tau_r = 2.36 * \frac{2b_2}{b_1 - \sqrt{b_1^2 - 4b_2}} = 2.36 * \frac{(M_1 + \sqrt{4M_2 - 3M_1^2})}{2}; \tag{5}$$

the resulting delay estimates are compared against those of various other methods in Table 1. We see that our analytical delay model gives estimates close to those obtained from SPICE, but as expected Elmore delay also gives good estimates for this case where the interconnect response is overdamped.

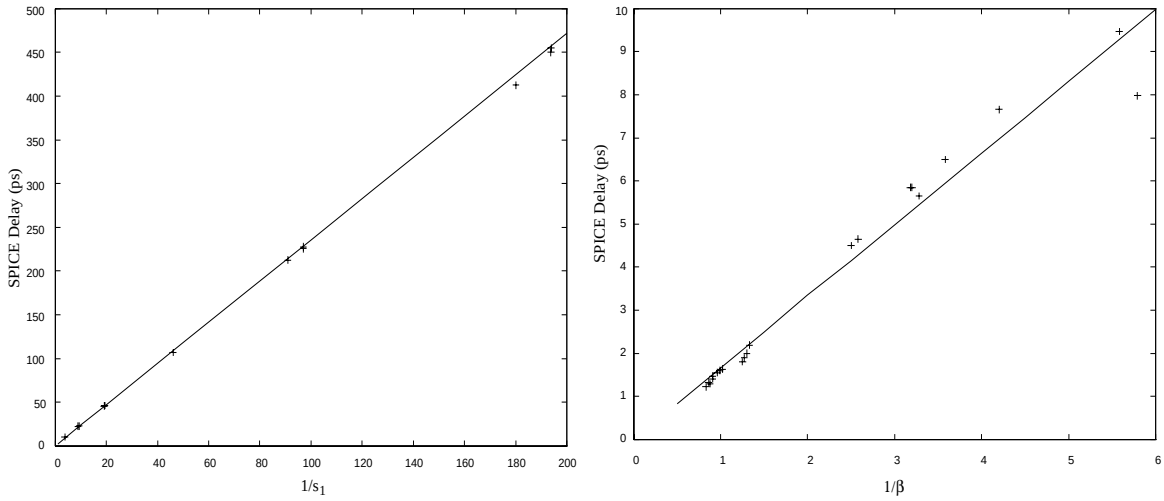

Figure 4: The plot on the left shows the strong linear fit between SPICE delay and $\frac{1}{|s_1|}$ for real poles with $K_r = 2.36$. The plot on the right shows the strong linear fit between SPICE delay and $\frac{1}{\beta}$ for complex poles with $K_c = 1.66$.

Complex Poles

The condition for complex poles is $(4M_2 - 3M_1^2) = (b_1^2 - 4b_2) \leq 0$. The time-domain response for complex poles is given by

$$v(t) = V_0 \left(1 - \frac{\sqrt{\alpha^2 + \beta^2}}{\beta} e^{-\alpha t} * \sin(\beta t + \rho)\right)$$

where $\alpha = \frac{M_1}{2(M_1^2 - M_2)}$ $\beta = \frac{\sqrt{3M_1^2 - 4M_2}}{2(M_1^2 - M_2)}$ and $\rho = \tan^{-1}(\frac{\beta}{\alpha})$. Using the above equation and threshold

voltage v_{th}, we get

$$e^{-\alpha t} * \sin(\beta * t + \rho) = \frac{1 - v_{th}}{\sqrt{1 + (\frac{\alpha}{\beta})^2}} \tag{6}$$

The delay at a given threshold voltage can be computed by solving for time in Equation (6) recursively. One way to solve the recursive Equation (6) is to approximate the time variable in the exponential term by Elmore delay, i.e., substitute T_{ED} for time t. Expanding *sine* as a Taylor series and considering only the first term yields

$$e^{-\alpha * T_{ED}} * \sin(\beta * \tau_c + \rho) \approx e^{-\alpha * T_{ED}} * (\beta * \tau_c + \rho) = \frac{1 - v_{th}}{\sqrt{1 + (\frac{\alpha}{\beta})^2}}$$

Therefore,

$$\tau_c = \frac{K_c}{\beta}$$

where $K_c = \left(\frac{(1-v_{th})e^{\alpha * T_{ED}}}{\sqrt{1+(\frac{\alpha}{\beta})^2}} - \rho \right)$. Substituting for β and using $M_1 = b_1$ and $M_2 = b_1^2 - b_2$, our delay estimate is given by

$$\tau_c = \frac{K_c}{\beta} = K_c * \frac{2b_2}{\sqrt{4b_2 - b_1^2}}$$

Even though K_c is function of b_1 and b_2, for a wide range of interconnect, source, and load parameters it too is almost a constant. We determined the constant value $K_c = 1.66$ again by finding a good fit between SPICE delay values and $\frac{1}{\beta}$, as shown on the right side of Figure 4. Therefore, the 90% threshold delay estimate for complex poles is

$$\tau_c = 1.66 \cdot \frac{2b_2}{\sqrt{4b_2 - b_1^2}} = 1.66 \cdot \frac{2(M_1^2 - M_2)}{\sqrt{3M_1^2 - 4M_2}} \ . \tag{7}$$

Table 2 shows delay values for various combinations of source, load and interconnect parameters assuming the value of K_c obtained by this regression analysis. The delay estimates using our analytical model are within 10% of SPICE-computed delay estimates, while Elmore delay estimates vary by as much as 33% from SPICE-computed delays. Hence, for the case of complex poles (i.e., underdamped response), the Elmore model is no longer acceptably accurate. Last, we consider the special case in which poles are equal, i.e., a double pole configuration.

Double Poles

The condition for a double pole is $(b_1^2 - 4b_2) = 0$. The double-pole response is

$$V(s) \ = \ \frac{V_0}{s} \frac{1}{1 + b_1 s + b_2 s^2} = \frac{V_0}{s} \frac{1}{b_2 (s - s_1)^2} = V_0 \left(\frac{1}{s} - \frac{1}{s - s_1} - \frac{2}{b_1} \frac{1}{(s - s_1)^2} \right)$$

Source		**Load**	**Delay from Response**	**Analytical Delay Models (% error)**	
R_S	L_S	C_T	**SPICE**	**Elmore**	**New Model**
Ω	pH	pF	ps	ps	ps
10	0.0246	0.0176	1.22	0.90 (26%)	1.30 (6%)
15	0.0246	0.0176	1.33	1.31 (2%)	1.38 (4%)
20	0.0246	0.0176	1.47	1.71 (16%)	1.51 (3%)
25	0.0246	0.0176	1.60	2.12 (33%)	1.64 (3%)
10	0.0246	0.176	4.50	5.12 (14%)	4.25 (6%)
15	0.0246	0.176	5.85	7.32 (25%)	5.31 (9%)
20*	0.0246	0.176	7.90	9.55 (21 %)	8.60 (7%)
10	2.46	0.0176	1.31	0.90 (31%)	1.40 (%)
15	2.46	0.0176	1.40	1.31 (7%)	1.49 (7%)
20	2.46	0.0176	1.55	1.71 (10%)	1.59 (2%)
25	2.46	0.0176	1.63	2.12 (30%)	1.69 (4%)
10	2.46	0.176	4.65	5.10 (10%)	4.30 (8%)
15	2.46	0.176	5.85	7.33 (25%)	5.30 (9%)
20	2.46	0.176	7.98	9.55 (19%)	8.70 (9%)
10	24.6	0.0176	1.80	0.90 (50%)	1.96 (9%)
15	24.6	0.0176	1.89	1.31 (31%)	2.06 (9%)
20	24.6	0.0176	2.00	1.71 (15%)	2.15 (7%)
25	24.6	0.0176	2.19	2.11 (4%)	2.21 (1%)
10	24.6	0.176	5.65	5.10 (10%)	5.44 (4%)
15	24.6	0.176	6.50	7.33 (13%)	5.95 (8%)
20	24.6	0.176	7.66	9.55 (25%)	6.97 (9%)
25	24.6	0.176	9.47	11.78 (24%)	9.26 (2%)

Table 2: 90% threshold voltage delay estimates for the combinations of source and load parameters for which the poles of the response are complex (i.e., underdamped configurations). The interconnect line parameters are $R = 0.015\ \Omega/\mu m$, $L = 0.246\ pH/\mu m$ and $C = 0.176\ fF/\mu m$ and the length of the interconnect is 100 μm. The percentage error of each delay model with respect to SPICE is also given.

where $s_1 = -\frac{b_1}{2b_2}$, and the time-domain response is given by $v(t) = V_0\left(1 - e^{ts_1} - \frac{2t}{b_1}e^{ts_1}\right)$. The delay at 90% threshold is

$$\tau_{0.9} = \frac{2b_2}{b_1}\ln\left(10(1 + \frac{2T_{0.9}}{b_1})\right) = K_d\frac{2b_2}{b_1} = K_d\frac{b_1}{2}$$

which gives a recursive equation for K_d, i.e.,

$$K_d = \ln\left(10(1 + \frac{2T_{0.9}}{b_1}\right) = \ln\left(10(1 + K_d)\right)$$

from which $K_d \approx 3.9$. Thus, in the case of a double pole the 90% threshold delay is estimated as

$$\tau_{0.9} = K_d \cdot \frac{b_1}{2} = 1.95 b_1 \tag{8}$$

which is independent of the inductance value and different from the Elmore delay expression.

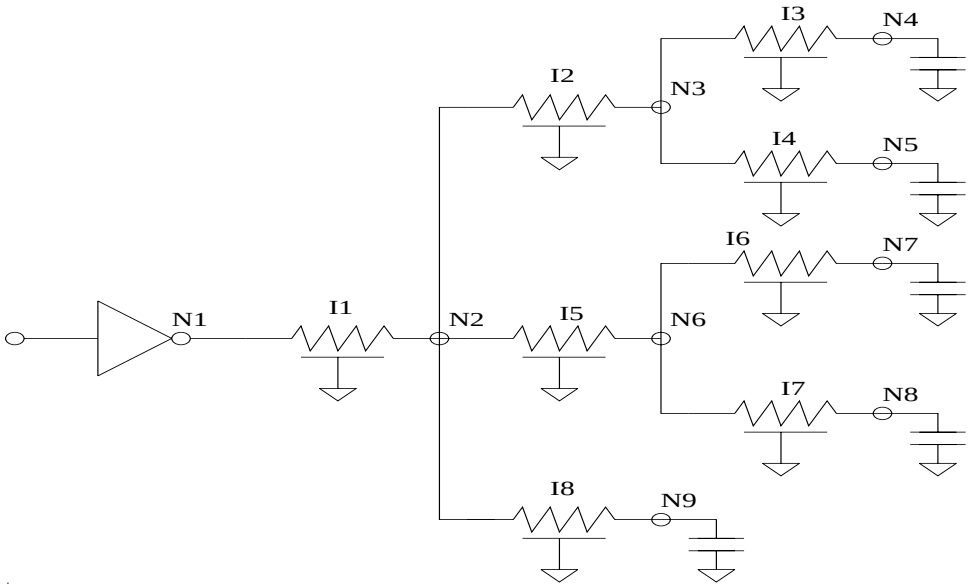

Figure 5: A simple interconnection tree consisting of distributed RLC lines. The lengths of the various interconnects are given in Table 3.

4 Interconnection Trees

Finally, we now describe the extension of our analytical model to estimate delays in arbitrary interconnect trees. An RLC network is called an RLC tree if it does not contain a closed path of resistors and inductors, i.e., all resistors and inductors are floating with respect to ground and all capacitors are connected to ground. Consider an RLC interconnect tree with root (or source) S and set of sinks (or leafs) $L = \{L_1, L_2, \ldots, L_n\}$. The unique path from root S to the sink node i is denoted by $p(i)$ and is referred as the *main path*. The edges/nodes not on the main path are referred as the *off-path* edges/nodes. We model each edge on the main path of the tree using a lumped RLC segment, e.g., an **L**, **T**, or **Π** model. We replace the off-path subtree rooted at node k with the total subtree capacitance at node k. (Figure 6 shows an example of a main path where each branch in the tree is replaced by RLC segments, and the off-path subtrees are replaced by their respective subtree capacitances.) Hence, at any node k the total capacitance is given by

Interconnect	**Length** μm
I1	50
I2	100
I3	50
I4	200
I5	100
I6	50
I7	100
I8	200

Table 3: The length of various interconnects in the tree of Figure 5.

$$\begin{aligned} C'_k &= C_k && \text{if no off-path subtree at node } k \\ C'_k &= C_k + C_{T(k)} && \text{if node } K \text{ has off-path subtree } T(k) \end{aligned}$$

where C_k is the capacitance at the node and $C_{T(k)}$ is the off-path subtree capacitance at node k. The k^{th} coefficient b_k of the transfer function for the general RLC circuit of Figure 6 can be expressed using the following recursive equation [5]:

$$b_k^{N+1} = R_N \sum_{j=1}^{N} C'_j \cdot b_{k-1}^j + L_N \sum_{j=1}^{N} C'_j \cdot b_{k-2}^j + b_k^N \tag{9}$$

where b_K^N refers to the coefficient of s^k in the transfer function between node k and node 1. Note that $b_0^j = 1$, $b_{-1}^j = 0$ for all j and $b_k^1 = 0$ for all k. Using the above recursive equation the expressions for the first and second coefficients of the transfer function can be derived as

$$\begin{aligned} b_1^{N+1} &= R_N \sum_{j=1}^{N} C'_j + b_1^N = \sum_{i=1}^{N} R_i \sum_{j=1}^{i} C'_j \\ b_2^{N+1} &= R_N \sum_{j=1}^{N} C'_j b_1^j + L_N \sum_{j=1}^{N} C'_j + b_2^N \\ &= \sum_{j=2}^{N} C'_j \sum_{l=j}^{N} R_l \sum_{i=1}^{j-1} C'_j \sum_{d=i}^{j-1} R_d + \sum_{j=1}^{N} C'_j \sum_{l=j}^{N} L_l \end{aligned} \tag{10}$$

For any given source and sink pair the coefficients b_1 and b_2 can be computed in linear time by traversing the main path and using the above recursive equation. Using the analytical delay model developed in the previous section, we can obtain a analytical delay estimate for RLC

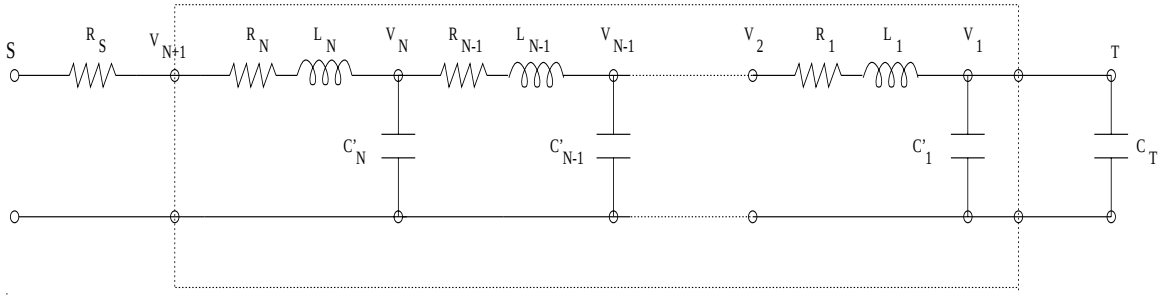

Figure 6: Representation of the main path in the tree, where each distributed line is modeled using RLC segments.

interconnect trees using the first and second coefficients. Thus, the 90% threshold delay at a given sink i, depending on the value of $(4M_2 - 3M_1^2)$, is

$$T_{ND}(i) = \begin{cases} K_r \cdot \frac{(M_1 + \sqrt{4M_2 - 3M_1^2})}{2} & \text{for Real poles} \\ K_c \cdot \frac{2(M_1^2 - M_2)}{\sqrt{3M_1^2 - 4M_2}} & \text{for Complex poles} \\ K_d \cdot \frac{M_1}{2} & \text{for Double poles} \end{cases} \tag{11}$$

where the first and second moments are expressed as $M_1 = b_1$ and $M_2 = b_1^2 - b_2$. The coefficients of the transfer function are obtained from Equation (10). By contrast, the Elmore delay at the sink is equal to the first moment, or the first coefficient b_1 of the transfer function of the source-sink main path [14]. The 90% threshold delay using the first moment is simply

$$T_{ED}(i) = 2.3 * M_1 \tag{12}$$

which we emphasize can be inaccurate despite its wide use, since it ignores inductance of the interconnect line.

We evaluate the effect of our analytical model by considering a simple interconnection tree shown in Figure 5. We consider the sink node $N4$ for delay estimation. Each edge on the main path between the root and node $N4$ is replaced by a two **L** segment model.[6] We then apply the above described recursive coefficient (or moment) computation for the resultant RLC circuit of the main path. The 90% threshold delays according to both the Elmore model and our new analytical model are computed using Equations (11) and (12). We also compute the delay at the given sink node using SPICE3e, where each edge of the tree is modeled using the LTRA

[6]Our model is not limited to traditional segment models, and indeed we believe the accuracy of our results would improve if we use non-uniform segment models [5, 18] designed to perfectly match the low-order moments of the distributed RLC line.

Interconnect parameters /μm	**Driver res.** Ω	**Load cap.** pF	**SPICE Delay** ps	**Elmore Delay** ps	**New Model Delay** ps
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 0.246\ pH$	10	0.02	5.7	6.6	5.0
$R = 0.0015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	10	0.2	37	26	31
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	10	0.2	39	29	32
$R = 0.0015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	10	2.0	179	238	205
$R = 0.0015\ \Omega$ $C = 0.176\ fF$ $L = 0.246\ pH$	10	2.0	231	238	232
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	10	2.0	199	270	230
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	100	2.0	2419	2361	2367

Table 4: 90% threshold delay values for a wide range of interconnect parameters at Node 4 of the tree in Figure 5. We compare SPICE LTRA, and the Elmore model, against our analytical delay model.

(Lossy Transmission Line) model (with SPICE, we first compute the response at the sink node and then obtain the delay for 90% threshold voltage). Table 4 presents delay estimates for a range of interconnect parameters, driver resistance values, and sink load capacitance values. The Elmore delay varies by as much as 35% from the SPICE-computed delay. However, our new model is within 15% of the SPICE delay for all examples. Another advantages of our model is due to simulation complexity. Our delay estimates also require three orders of magnitude less computation than SPICE, since they have the same time complexity as the Elmore delay estimate.

5 Conclusions

Fast delay estimation methods, as opposed to simulation techniques, are needed for incremental performance-driven layout synthesis. Elmore delay based estimation methods, although efficient, cannot accurately estimate the delay for RLC interconnect lines. We have obtained an analytical delay model, based on first and second moments of RLC interconnection lines, which considers the effect of inductance. Resulting delay estimates are significantly more accurate than Elmore delay. We also extend our delay model to estimate source-sink delays in arbitrary interconnect trees. Even for the small tree topology considered, we observe significant improvement of at least 20% in the accuracy of our delay estimates, compared to the Elmore model. Since our model has the same time complexity as the Elmore model, we believe it can be valuable in modern iterative layout synthesis methodologies. Our ongoing work applies our analytical model to delay-driven routing tree construction, zero-skew routing, and delay estimation in nets spanning multiple routing layers (i.e., with modeling of vias).

References

[1] L. N. Dworsky, *Modern Transmission Line Theory and Applications*, Wiley, 1979.

[2] W. C. Elmore, "The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers", *Journal of Applied Physics* 19, Jan. 1948, pp. 55-63.

[3] M. A. Horowitz, "Timing Models for MOS Circuits", *PhD Thesis*, Stanford University, Jan. 1984.

[4] C. C. Huang and L. L. Wu, "Signal Degradation Through Module Pins in VLSI Packaging", *IBM J. Res. and Dev.* 31(4), July 1987, pp. 489-498.

[5] A. B. Kahng and S. Muddu, "Two-pole Analysis of Interconnection Trees", *Proc. IEEE MCMC Conf.*, January 1995, pp. 105-110.

[6] A. B. Kahng and S. Muddu, "Accurate Analytical Delay Models for VLSI Interconnections", *UCLA CS Dept. TR-950034*, Sep. 1995.

[7] B. Krauter, R. Gupta, J. Willis, and L. T. Pileggi, "Transmission Line Synthesis", *Proc. 32th ACM/IEEE Design Automation Conf.*, June 1995, pp. 358-363.

[8] S. Lin and E. S. Kuh, "Transient Simulation of Lossy Interconnect", *Proc. 29th ACM/IEEE Design Automation Conf.*, June 1992, pp. 81-86.

[9] S. P. McCormick and J. Allen, " Waveform Moment Methods for Improved Interconnection Analysis", *Proc. 27th ACM/IEEE Design Automation Conf.*, June 1990, pp. 406-412.

[10] L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis", *IEEE Trans. on CAD* 9, Apr. 1990, pp.352-366.

[11] V. Raghavan, J. E. Bracken and R. A. Rohrer, "AWESpice: A General Tool for the Accurate and Efficient Simulation of Interconnect Problems", *Proc. 29th ACM/IEEE Design Automation Conf.*, June 1992, pp. 87-92.

[12] C. L. Ratzlaff, N. Gopal, and L. T. Pillage, "RICE: Rapid Interconnect Circuit Evaluator", *Proc. 28th ACM/IEEE Design Automation Conf.*, June 1991, pp. 555-560.

[13] J. S. Roychowdhury and D. O. Pederson, "Efficient Transient Simulation of Lossy Interconnect", *Proc. 28th ACM/IEEE Design Automation Conf.*, June 1991, pp. 740-745.

[14] J. Rubinstein, P. Penfield and M. A. Horowitz, "Signal Delay in RC Tree Networks", *IEEE Trans. on CAD* 2(3), July 1983, pp. 202-211.

[15] T. Sakurai, "Approximation of Wiring Delay in MOSFET LSI", *IEEE Journal of Solid-State Circuits*, Aug. 1983, Vol.18, No.4, pp. 418-426.

[16] T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's", *IEEE Trans. on Electron Devices* 40, Jan. 1993, pp. 118-124.

[17] M. Sriram and S. M. Kang, "Fast Approximation of The Transient Response of Lossy Transmission Line Trees", *Proc. ACM/IEEE Design Automation Conf.*, June 1993, pp. 691-696.

[18] Q. Yu and E. S. Kuh, "Exact Moment Matching Model of Transmission Lines and Application to Interconnect Delay Estimation", *IEEE Trans. VLSI Systems* 3, June 1995, pp. 311-322.

[19] D. Zhou, S. Su, F. Tsui, D. S. Gao and J. S. Cong, "A Simplified Synthesis of Transmission Lines with A Tree Structure", *Intl. Journal of Analog Integrated Circuits and Signal Processing* 5, Jan. 1994, pp. 19-30.