Electrical assessment of lithographic gate line-end patterning

Puneet Gupta
University of California, Los Angeles
Electrical Engineering Department
Los Angeles, California 90095

Kwangok Jeong
University of California, San Diego
Electrical and Computer Engineering Department
La Jolla, California 92093
E-mail: kjeong@vlsicad.ucsd.edu

Andrew B. Kahng
University of California, San Diego
Electrical and Computer Engineering Department
and
Computer Science and Engineering Department
La Jolla, California 92093

Chul-Hong Park
Samsung Electronics Co., Ltd.
Semiconductor R&D Center, CAE Team
NRD Building, Hwasung-City
Gyeonggi-Do, Korea

Abstract. Line-end pullback is a major source of patterning problems in low-k_1 lithography. Lithographers have been well-served by geometric metrics such as critical dimension (CD) at a gate edge; however, the ever-rising contribution of line-end extension to layout area necessitates reduced pessimism in qualification of line-end patterning. Electrically aware metrics for line-end extension can be helpful in this regard. The device threshold voltage is, with nominal patterning, a weak function of line-end shapes. However, the electrical impact of line-end shapes can increase with overlay errors, since displaced line-end extensions can be enclosed in the transistor channel, and nonideal line-end shape will manifest as an additional gate CD variation. We propose a *super-ellipse* parameterization that enables exploration of a large variety of line-end shapes. Based on a gate capacitance model that includes the fringe capacitance due to the line-end extension, we model line-end-dependent incremental current ΔI_{on} and ΔI_{off} to reflect inverse narrow width effect. Last, we calculate the I_{on} and I_{off} considering line-end shapes as well as line-end extension length, and we define a new electrical metric for line-end extension—namely, the *expected* change in I_{on} or I_{off} under a given overlay error distribution. Our model accuracy is within 0.47% and 1.28% for I_{on} and I_{off}, respectively, compared to 3-D TCAD simulation in a typical 45-nm process. Using our proposed electrical metric, we are able to quantify the electrical impact of optical proximity correction, lithography, and design rule parameters, and we can quantify trade-offs between cost and electrical characteristics. © *2010 Society of Photo-Optical Instrumentation Engineers.* [DOI: 10.1117/1.3452319]

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1 Introduction

In the low-k_1 patterning regime ($k_1 < 0.3$), gate shape is no longer a perfect rectangle. Current circuit analysis tools assume that transistor gate and diffusion shapes are perfect rectangles, and they are unable to handle complicated geometries. Large discrepancies can be observed between the simulated and measured values of such transistor parameters as current and threshold voltage. Moreover, such discrepancies are likely to become more significant as overlay becomes a more critical issue in future technologies.

Several previous works electrically model nonrectilinear geometries.[1–7] All of these works consider the threshold voltage and hence the current density to be uniform along the device width. As a result, variations including that of gate length are treated the same, irrespective of the location of the variation. It is known that the fringing capacitance[8] due to line-end extension and dopant scattering significantly affects the device threshold voltage. These effects are more pronounced near the device edges and roll off sharply toward the center of the device. Several previous works have accounted for this effect via nonrectangular gate models.[9–11] Most of these works slice nonrectangular gates along the device width at a certain level of granularity and then sum I_{on} (or I_{off}) of all slices to model I_{on} (or I_{off}) of the nonrectangular device. For each slice, the current density model corresponding to its length is used. The total current of the device is the integral of the current density over its width. The total current can be used to provide an equivalent length for the rectangular device, so that it can be modeled using SPICE-like tools. Gupta et al.[12] have also used TCAD simulation to investigate the impact of the nonrectangular shape of diffusion on circuit performance.

The primary concerns of lithographic patterning are *line-end pullback* and *linewidth*. Traditionally, lithographers have measured line-end printing quality by (1) line-end gap (space between two facing line-ends); (2) critical dimension (CD) at the gate edge (*LW*0); and (3) nonexistence of line-end shortening (i.e., the condition where poly fails to cover active completely). Although these geometric metrics have served as good indicators, the ever-rising contribution to layout area of line-end extension—defined as the extension of polysilicon shape beyond the active edge—strongly motivates reduction of pessimism in qualifying line-end patterning. The quality of line-end patterning depends on the rounded shape of the line-end extension as well as on linewidth at the device edge (and, to a negligible extent, on line-end gap).

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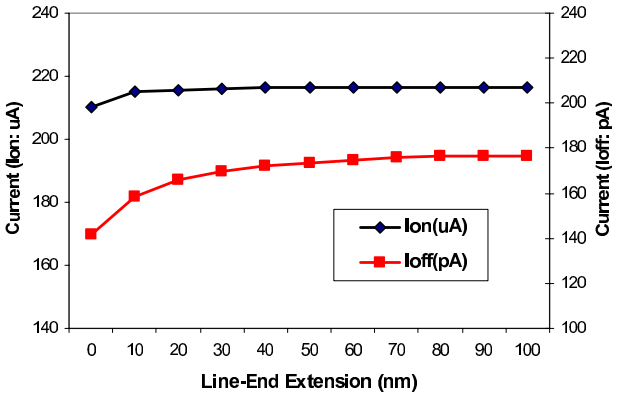

Fig. 1 I_{on} and I_{off} change due to line-end extension length.

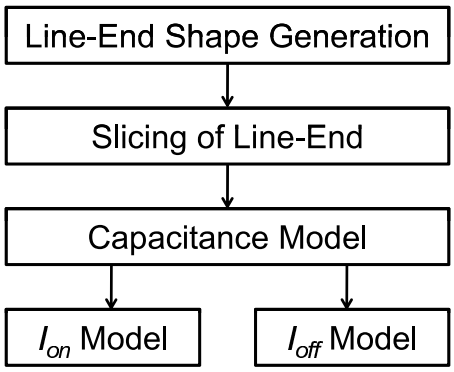

Fig. 2 Line-end extension modeling flow. I_{on} and I_{off} can be modeled as functions of line-end extension capacitance.

We employ 3-D TCAD simulators[13,14] to investigate the changes of gate capacitance, I_{on} and I_{off}, according to various line-end shapes and line-end extension lengths. We observe that I_{on} and I_{off} have strong relationships with line-end shapes. For example, our preliminary experiments using the 3-D TCAD tool, Synopsys DaVinci,[15] indicate that line-end extension length can affect I_{on} and I_{off} by as much as 4.5% and 30%, respectively, as shown in Fig. 1. Moreover, the electrical impact of the line-end extension can vary significantly with overlay.

In this paper, we propose a novel modeling framework that includes (1) capacitance modeling of a line-end extension and consequent current density changes in channel, and (2) I_{on} and I_{off} modeling from the new capacitance model. We define a new electrical metric for a line-end shape as the *expected* change in I_{on} or I_{off} under a given overlay error distribution. We further apply *a super-ellipse* form to parameterize line-end shapes, and we then generate a large variety of line-end shapes. We evaluate the electrical metric on these line-end shapes to come up with simple rules of thumb that the lithographer can use to quickly evaluate the quality of a lithography+optical proximity correction (OPC) solution with respect to line-end shaping. We also evaluate post-litho line-end shapes while varying OPC, lithography, and design rule parameters, and find a trade-off between cost and electrical characteristics.

2 Line-End Modeling

Line-end extension affects the fringe capacitance to the channel of a MOS gate, which in turn affects the threshold voltage of the gate. Hence, I_{on} and I_{off} models accounting for line-end impact can be developed in terms of line-end capacitance. Figure 2 shows the overall flow of the line-end modeling.

2.1 *Line-End Shape Generation with Super-Ellipse*

We propose a line-end shape generation method using the super-ellipse equation. A super-ellipse is defined as the set of all points (x,y) that satisfy

$$\left|\frac{x}{a}\right|^n + \left|\frac{y-k}{b}\right|^n = 1,$$

where $n>0$, a and b are the semiminor and semimajor axes of the super-ellipse, and k represents the line-end shift in the y axis, as shown in Fig. 3. For a given line-end shape, a and b represent the gate length and the length of the line-end extension, respectively. The exponent n determines the curvature, or corner rounding, of the line-end extension. For example, $n=2$ yields an ordinary ellipse, and increasing n beyond 2 yields shapes with sharper corners, increasingly resembling a rectangle. The center o of a super-ellipse represents a overlay error value, where 3σ is considered to be the worst-case overlay error.

To capture asymmetric line-end shapes, the super-ellipse can be rotated about its center using the transform $x=x'\cos\theta-y'\sin\theta$ and $y=x'\sin\theta+y'\cos\theta$ (or $x=x'\cos\theta+y'\sin\theta$ and $y=-x'\sin\theta+y'\cos\theta$), where x' and y' are the coordinates of the original super-ellipse shape. The quantity $b+k$ represents the new line-end extension (LEE) length after the line-end shift. In this paper, we focus on symmetric line-end shapes only.

3 Nonuniform Channel Modeling Including Line-End

An electrical model for the line-end extension must capture change in power and performance characteristics of a given device. For line-end modeling, we convert a lithography contour to several sliced rectangles, as shown in Fig. 4. For each slice, we use a current density model corresponding to its length l_i. The sum of the currents of all slices is the total current of the device. The total current can be used to calculate the gate length of an equivalent rectangular device, so that the current can be evaluated by SPICE-like tools. This line-end model, along with a nonuniform channel

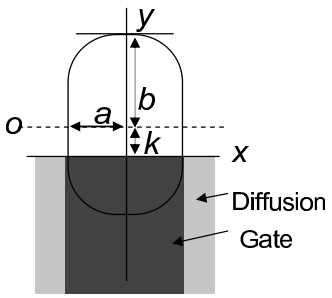

Fig. 3 An example of line-end shape represented by the super-ellipse equation.

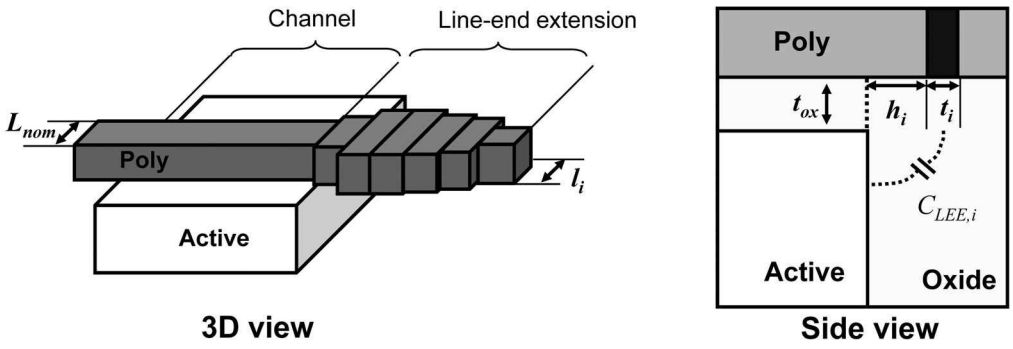

Fig. 4 Modeling line-end capacitance.

model similar to Gupta et al.'s work,[10] is used to model the device under overlay error. We calculate the probability of each slice being placed at a given location from the overlay error distribution. Using location-dependent fringe capacitance and current models for the line-end extension and channel, as discussed in Secs. 3.1–3.3, as well as the overlay error probability model in Sec. 3.4, we predict I_{on} or I_{off} considering a given overlay error.

3.1 *Capacitance Model*

Gate capacitance is the sum of capacitance of the gate channel ($C_{channel}$) and capacitance of the line-end extension (C_{lee}). C_{lee} is the fringe capacitance between the line-end extension and gate channel. We can simply model the capacitance of the line-end extension as the sum of the fringe capacitance of each slice of the line-end extension, as illustrated in Fig. 4:

$$C_{lee} = \sum_{i=1}^{N} C_{lee,i},$$

$$\text{where } C_{lee,i} = l_i^{\alpha}\left(\frac{t_i}{h_i + t_i/2 + t_{ox}}\right)^{\beta}. \quad (1)$$

Capacitance of each line-end slice or segment can be modeled as a function of its length (l_i), thickness (t_i), distance from the gate edge (h_i) and gate oxide thickness (t_{ox}). Intuitively, the fringe-capacitance effect increases with larger length, larger thickness, and smaller distance from the gate edge.

We simulate capacitance changes using a 3-D RC extraction tool, Synopsys Raphael, while varying line-end extension length. In this simulation, we assume STI oxide depth of 100 nm, t_{ox} of 1.5 nm, gate thickness of 100 nm, and gate length of 45 nm, consistent with the 3-D device simulation setup used to characterize I_{on} and I_{off}. We find model coefficients α and β using the MATLAB nonlinear regression function (*nlinfit*).[16] Our model shows 1.19% of average magnitude error on 150 different line-end shapes, with α=0.1389 and β=0.4253. All dimensional parameters of our model are in units of nm, and the calculated capacitance is in units of aF.

Figures 5(a)–5(c) show three representative shapes of line-end extension, for which l_i can be calculated directly from the super-ellipse parameters a, b, k, and n, as follows:

Tapering: Fig. 5(a) shows the case of *tapering*, in which the center of the super-ellipse is on the gate edge, and l_i can be calculated as

$$l_i = 2a\left(1 - \left|\frac{h_i - k}{b}\right|^n\right)^{1/n}.$$

Bulge: Fig. 5(b) represents a *bulge* line-end shape, in which the minor axis is greater than L_{nom} and the minimum linewidth between the center of the super-ellipse and the gate edge is greater than or equal to the nominal linewidth

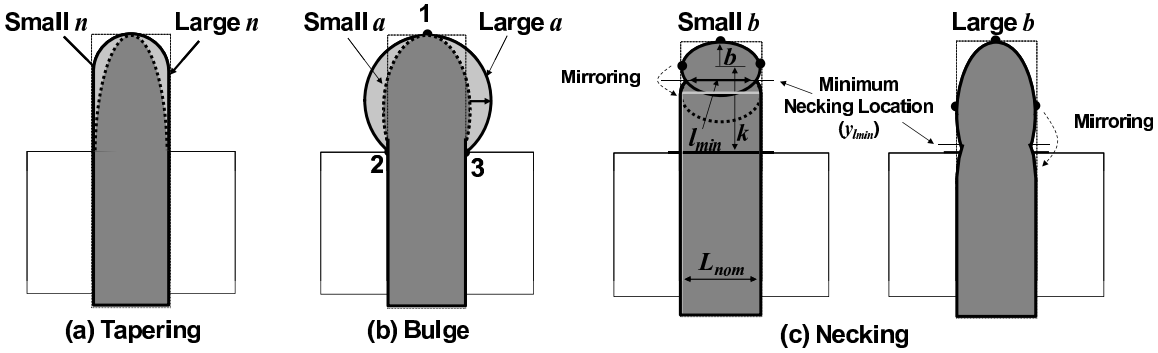

Fig. 5 Line-end shapes represented by the super-ellipse equation.

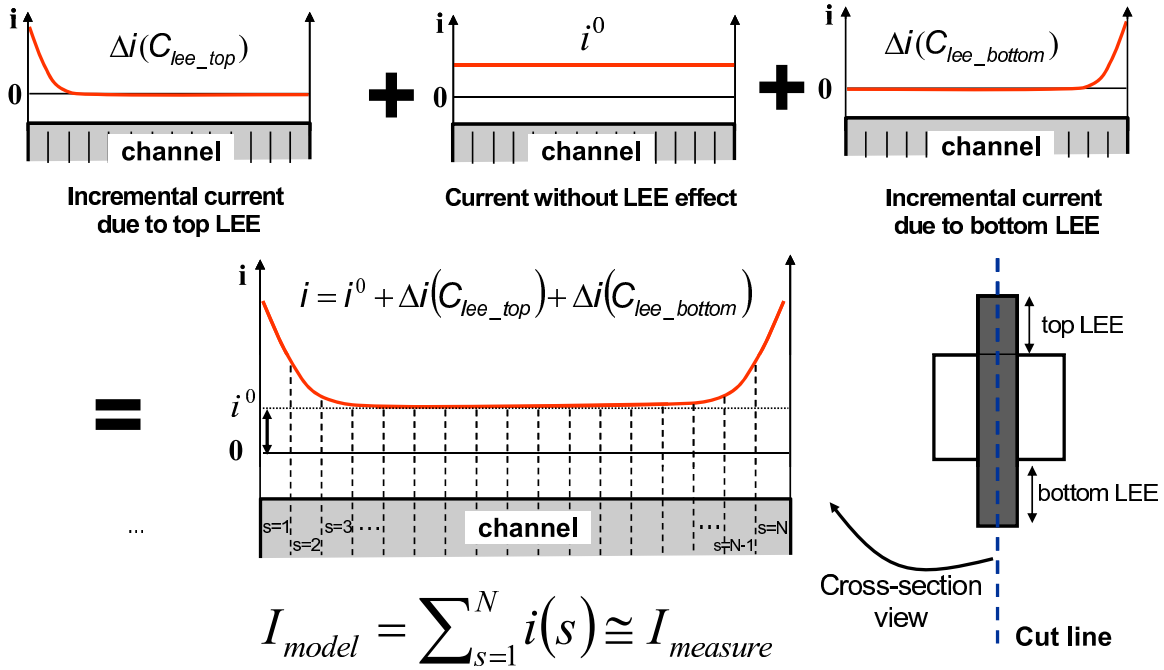

Fig. 6 Nonuniform channel modeling procedure.

(L_{nom}). The corresponding y coordinate, when the linewidth is L_{nom}, is calculated by

$$y_{L_{nom}} = k - b\left(1 - \left|\frac{L_{nom}/2}{a}\right|^n\right)^{1/n}.$$

The value of l_i for the bulge shape is then computed as

$$l_i = 2a\left(1 - \left|\frac{h_i - k}{b}\right|^n\right)^{1/n}, \quad h_i \geq y_{L_{nom}},$$

$$l_i = L_{nom}, \quad 0 \leq h_i \leq y_{L_{nom}}.$$

Necking: Fig. 5(c) gives two examples of *necking* shapes. It is difficult to ensure smooth changes in linewidth for necking cases by using one super-ellipse. Therefore, we apply a mirroring transform where the mirroring axis has the minimum linewidth (l_{min}). The corresponding y coordinate of the mirroring axis $y_{l_{min}}$ is calculated by

$$y_{l_{min}} = k - b\left(1 - \left|\frac{l_{min}/2}{a}\right|^n\right)^{1/n}. \tag{2}$$

The value of l_i for the necking shape is then

$$l_i = 2a\left(1 - \left|\frac{h_i - k}{b}\right|^n\right)^{1/n}, \quad h_i \geq y_{l_{min}},$$

$$l_i = 2a\left(1 - \left|\frac{h_i - 2y_{l_{min}} + k}{b}\right|^n\right)^{1/n}, \quad 2y_{l_{min}} - k \leq h_i \leq y_{l_{min}},$$

$$l_i = L_{nom}, \quad h_i \leq 2y_{l_{min}} - k.$$

3.2 I_{on} Model

Using the capacitance model for line-end extension, we propose a new model for I_{on}. Inverse narrow width effect (iNWE) due to the line-end fringe capacitance is modeled in the BSIM4 SPICE model[17] as an exponentially decaying function of gate width. We assume that the impact of line-end capacitance decreases exponentially from the gate edge to the channel, to account for the iNWE model in BSIM4. Figure 6 illustrates our modeling approach, where i_{on} is the on-current of an individual gate segment s, and the segment index s represents the distance from the gate edge. C_{lee_top} and C_{lee_bottom} represent the line-end capacitances at the top and bottom sides of a gate, respectively. Thus, total current I_{on} is expressed as a sum of segment currents i_{on} over all segments:

$$I_{on} = \sum_{s=1}^{N} i_{on}(C_{lee_top}, C_{lee_bottom}, s, L)$$

$$i_{on}(C_{lee_top}, C_{lee_bottom}, s, L) = i_{on}^0(L_s) + \Delta i_{on}(C_{lee_top}, s, L_s) + \Delta i_{on}(C_{lee_bottom}, N - s + 1, L_s).$$

Here, $i_{on}^0(L_s)$ is the on-state current of a gate segment that is not affected by line-end extension. The additive on-state current (Δi_{on}) for each segment of a gate is modeled as a function of the line-end capacitance (C_{lee}), segment index (s), and length (in gate length direction) of the segment (L_s). More precisely, $i_{on}^0(L_s)$ and Δi_{on} are defined as

$$i_{on}^0(L_s) = h(L_s) \cdot i_{on_nom}^0,$$

$$\Delta i_{on}(C_{lee}, s, L_s) = f(C_{lee}) \cdot g(s) \cdot h(L_s),$$

$$f(C_{lee}) = (C_{lee})^{\alpha},$$

$$g(s) = \gamma \exp[-\beta(s-1)],$$

$$h(L_s) = \left(\frac{L_{nom}}{L_s}\right)^{k},$$

where $i^0_{on_nom}$ is the baseline current of a segment with a nominal gate length L_{nom}, as measured from the current value difference between two large-width devices that have the same line-end shape. Functions f and g account for the size and the exponential decay rate of the impact of line-end capacitance. Function h linearly scales the calculated current based on the gate length of a gate segment, since on-state current is an inverse-linear function of gate length.

Our fitting accuracy using the MATLAB nonlinear regression function (*nlinfit*)[16] is 0.24% average magnitude of error for 38 nm$\leq L_s \leq$52 nm. Here, α, β, and γ are 0.1616, 0.030, and 0.1349, respectively, and k is 1.035. I_{on} is given in units of μA.

3.3 I_{off} Model

I_{off} is similarly modeled as a sum of segment currents i_{off}. Again, C_{lee_top} and C_{lee_bottom} represent line-end capacitances at the top and bottom sides of a gate. Last, total off-state current I_{off} is expressed as

$$I_{off} = \sum_{s=1}^{N} i_{off}(C_{lee_top}, C_{lee_bottom}, s, L_s)$$

$$i_{off}(C_{lee_top}, C_{lee_bottom}, s, L_s) = i^0_{off}(L_s) + i_{off}(C_{lee_top}, s, L_s) + \Delta i_{off}(C_{lee_bottom}, N-s+1, L_s),$$

where $i^0_{off}(L_s)$ is the off-state current of a gate segment that is not affected by line-end extension. The additive off-state current (Δi_{off}) for each segment of a gate is modeled as a function of the line-end capacitance (C_{lee}), segment index (s), and length of the segment (L_s). More precisely,

$$i^0_{off}(L_s) = h_1(L_s) \cdot i^0_{off_nom},$$

$$\Delta i_{off}(C_{lee}, s, L_s) = f(C_{lee}) \cdot g(s) \cdot h_2(L_s),$$

$$f(C_{lee}) = (C_{lee})^{\alpha},$$

$$g(s) = \gamma \exp[-\beta(s-1)],$$

$$h_1(L_s) = k_1 \exp[k_2(L_s - L_{nom})],$$

$$h_2(L_s) = k_3 \exp[k_4(L_s - L_{nom})],$$

where $i^0_{off_nom}$ is the baseline current of a segment with nominal gate length L_{nom}, as measured from the current value difference between two large-width devices that have the same line-end shape. Functions f and g again account for the size and the exponential decay rate of the impact of line-end capacitance. Functions h_1 and h_2 exponentially scale the calculated current based on the gate length of a gate segment, since off-state current is an exponential function of gate length.

We find the coefficients using the MATLAB nonlinear regression function (*nlinfit*).[16] Here, α, β, and γ are 0.045, 0.012, and 667.2, respectively, and k_1, k_2, k_3, and k_4 are −0.5129, 0.6118, −0.2739, and 1.971, respectively. The model shows 1.02% average magnitude error compared to TCAD simulation for 38 nm$\leq L_s \leq$52 nm. I_{off} is given in units of nA.

3.4 Overlay Error Model

With overlay error, the segments near the channel edge change. Since segments in the channel affect I_{on} and I_{off} differently compared to the segments in the line-end extension, we first determine whether the segment belongs to the channel or the line-end extension. Overlay error is a vector component quantity in the x and y directions. We assume that the minimum poly-to-diffusion spacing is larger than the overlay error so that the overlay error does not cause any spurious transistor channels. Therefore, x direction (i.e., perpendicular to the poly direction) overlay error is neglected. Given an overlay error, we can calculate the I_{on} and I_{off} of the entire gate by summing up the current values (i_{on} and i_{off}) of segments that are in the channel.

Overlay error is assumed to have a normal distribution. To account for the different probabilities for different magnitudes of overlay error and corresponding current changes, we calculate expected current I_{exp} based on the normal distribution assumption of overlay error, with mean and 3σ assumed to be zero and 10 nm, respectively. (The ITRS sets 3σ overlay error for the MPU 45-nm half-pitch node as 11 nm (Ref. 18). We use 10 nm for simplicity in calculations. All results in the rest of this paper assume 10-nm 3σ overlay error.) Due to our segmentation-based current calculation, we discretize the range of magnitudes of overlay error. N_{sites} denotes the number of possible sites of poly placement due to overlay error. $P(m)$ is the probability of poly being placed at the m'th site, where $1 \leq m \leq N_{sites}$. In our modeling, we use 5 nm for segmentation size and five different sites (i.e., N_{sites}=5) for overlay error. The third site represents no (i.e., 0 nm) overlay error, and the others represent movement of poly segments by $\pm$5 nm$\sim\pm$10 nm. Each site m has probability $P(m)$ calculated by integrating the normal distribution between the limits of the site m, as shown in Fig. 7(b). The current $I(m)$ of a gate poly placed at site m is calculated according to where each segment of poly belongs. Last, we can calculate the expected current I_{exp} by integrating the product of $P(m)$ and $I(m)$ over the range of possible overlay error values:

$$I_{exp} = \sum_{m=1}^{N_{sites}} P(m) I(m).$$

4 Electrical Assessment of Line-End Shapes

In this section, we evaluate the accuracy of our models and assess the electrical characteristics of the various line-end shapes generated from the super-ellipse equation.

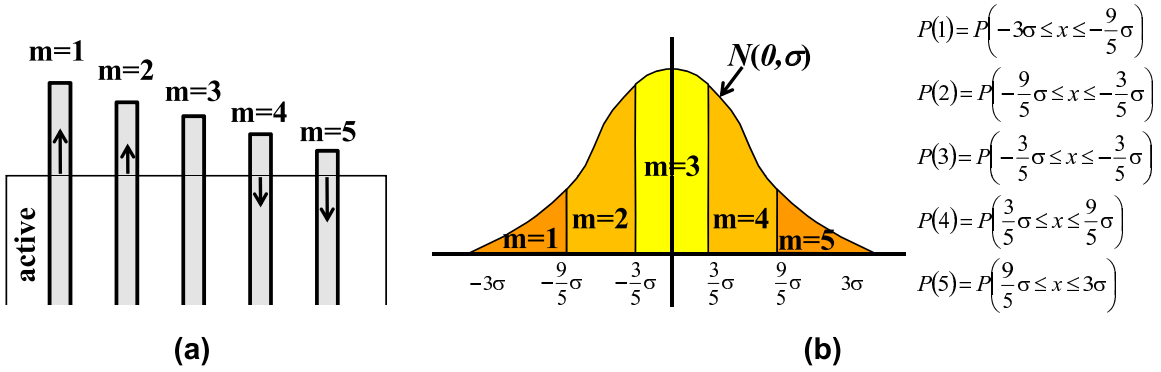

Fig. 7 Overlay error model: (a) five discretized overlay errors, and (b) probability $P(m)$ calculation for each overlay error m.

4.1 *Model Accuracy*

We apply our proposed model to an ideal rectangular line-end shape. Table 1 shows the comparisons of our model and the TCAD simulation. We measure I_{on} and I_{off}, changing the line-end extension length. Columns 1 and 2 show the drawn transistor width and line-end extension length, respectively. Columns 3 and 4 show the I_{on} and I_{off} values without considering the line-end effects. Comparing column 5 with 7, and 6 with 8, shows the accuracy of our model. Maximum errors of our I_{on} and I_{off} models are 0.66% and 2.50%, respectively.

Columns 9 and 10 show the impact of overlay error with 3σ=10 nm. When we reduce the line-end extension, we can see the decreasing trends of I_{on} and I_{off}, since small line-end extension results in small gate capacitance and hence higher threshold voltage. This result implies that an

Table 1 Model accuracy and impact of overlay error on rectangular line-end extension.

		Drawn		Model without overlay error		Sentaurus		Model with overlay error	
Width (nm)	LEE (nm)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)
100	100			105.260	51.291	104.956	50.484	105.191	51.257
	70			105.147	50.998	104.891	50.292	105.078	50.964
	50	104.956	50.484	105.042	50.720	104.797	50.007	104.972	50.684
	30			104.885	50.292	104.551	49.464	104.814	50.251
	10			104.556	49.334	103.870	48.102	104.423	48.748
200	100			209.064	97.013	209.277	96.921	208.927	96.949
	70			208.889	96.488	209.222	96.794	208.753	96.423
	50	209.277	96.921	208.728	95.989	209.129	96.488	208.590	95.922
	30			208.486	95.221	208.879	95.829	208.346	95.145
	10			207.978	93.503	208.157	94.089	207.744	92.450
300	100			312.080	138.318	311.365	136.726	311.876	138.226
	70			311.872	137.608	311.340	136.714	311.668	137.515
	50	311.365	136.726	311.679	136.934	311.318	136.563	311.475	136.838
	30			311.392	135.896	311.192	136.254	311.184	135.789
	10			310.788	133.575	310.239	134.307	310.467	132.149

Table 2 I_{on} and I_{off} changes with line-end extension and sharpness for 200-nm width NMOS.

	Super-ellipse exponent (n)											
	2.5		3.0		3.5		4.0		4.5		5.0	
Lee (nm)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)
100	208.91	***96.91***	208.92	***96.92***	208.92	***96.93***	208.92	***96.93***	208.92	***96.94***	208.92	***96.94***
90	208.87	***96.80***	208.87	***96.77***	208.87	***96.77***	208.87	***96.78***	208.87	***96.78***	208.87	***96.78***
80	208.85	***96.99***	208.82	***96.72***	208.81	***96.64***	208.81	***96.62***	208.81	***96.61***	208.81	***96.61***
70	208.93	***98.15***	208.82	***97.05***	208.78	***96.67***	208.76	***96.52***	208.75	***96.46***	208.75	***96.43***
60	209.20	***101.70***	208.91	***98.39***	208.79	***97.18***	208.73	***96.66***	208.70	***96.42***	208.69	***96.31***
50	209.77	111.53	209.18	***102.18***	208.90	***98.90***	208.76	***97.47***	208.69	***96.77***	208.64	***96.40***
40	210.85	141.91	209.77	112.71	209.22	***103.71***	208.93	***99.97***	208.76	***98.13***	208.66	***97.14***
30	212.72	274.60	210.89	148.55	209.92	118.38	209.36	107.41	209.02	***102.37***	208.80	***99.70***
20	—	—	212.95	372.79	211.29	187.85	210.29	137.34	209.66	118.09	209.29	109.01

unnecessarily large line-end rule is not desirable from the electrical point of view. Note that since the shape is perfectly rectangular, overlay error does not cause linewidth variation in the channel. Hence, the impact of overlay error is negligibly small for the ideal rectangular line-end shape.

4.2 *Evaluation of Line-End Shapes*

We also evaluate the line-end shapes generated by the proposed super-ellipse model. Tapering is a typical shape in the post-OPC silicon image. As noted earlier, corner rounding is represented by the super-ellipse parameter n. Larger n results in less corner rounding but increases mask cost in terms of mask writing time and mask inspection since aggressive OPC needs to be applied. Bulging may be caused by inaccurate OPC and may be amplified under defocus. The degree of bulge shape is determined by a and by having positive k. Necking is a reduction in linewidth that is caused by an excessive OPC hammerhead—i.e., the hammerhead results in narrow linewidth at the channel edge under defocus, even if the hammerhead can compensate for corner rounding error at a best-focus condition.

For each shape generated from a super-ellipse, as shown in Fig. 5, we change the line-end extension length by shifting the entire poly shape, and calculate I_{off} for each shape. (We limit the minimum line-end extension length to 20 nm, to avoid line-end shortening by overlay error.) When we reduce the line-end extension length, since the line-end part of the poly gate becomes enclosed by the diffusion, segments in the line-end extension turn into gate segments in the channel.

Table 2 shows the dependence of I_{on} and I_{off} on the super-ellipse exponent and the line-end extension length, i.e., on the *sharpness* of the line-end extension. In this case, the super-ellipse semiminor and semimajor axes are fixed at 22.5 nm and 100 nm, respectively. The bold italic entries in the table show the cases where I_{off} remains within 10% of the 100-nm LEE cases. As we increase n, the tapering becomes more rectangular, so that the I_{off} variation due to line-end extension length is reduced. As a result, LEE can be reduced further with larger n when 10% I_{off} increase is allowed. For example, for n=2.5, LEE can be reduced from 100 nm to 60 nm, but for n=4, LEE length can be reduced from 100 nm to 40 nm. As noted earlier, increased n requires more complex OPC and can increase OPC and mask costs. Note that in the table, some cases are out of the boundary of our model, but it is obvious that those cases must be avoided in design, so as to avoid excessive leakage current.

Table 3 shows the I_{on} and I_{off} dependence on the *fatness* of the bulge shape and the line-end extension length. The super-ellipse exponent is fixed at n=3.0. Since we use a contour that passes through three points in Fig. 5(b), if we change the semiminor axis a, the other parameters b and k are determined automatically by solving the super-ellipse equation. For the bulge shape line-end extension, I_{off} variation is small compared to the tapering (sharpness) case. We also observe that I_{on} and I_{off} are reduced by 7% and 38% when we reduce the line-end length from 100 nm to 20 nm with semiminor axis length of 28 nm. Typically, I_{on} and I_{off} decrease when line-end extension length decreases, since large-width line-end segments due to the bulge shape are turned into channel segments.

Table 4 shows the I_{on} and I_{off} dependence on the location of necking and the line-end extension. For this simulation, we use a super-ellipse with 100-nm line-end extension length. By changing the semimajor axis, we control the necking location where the linewidth is minimized. We shift the entire poly shape downward to model the reduc-

Table 3 I_{on} and I_{off} changes with line-end extension length and fatness for 200-nm width NMOS.

	Super-ellipse semiminor axis (a) (nm)											
	23		24		25		26		27		28	
Lee (nm)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)
100	208.91	96.87	208.91	96.80	208.90	96.74	208.89	96.69	208.88	96.65	208.87	96.61
90	208.76	96.00	208.60	95.09	208.50	94.47	208.30	94.00	208.16	93.64	208.01	93.35
80	208.50	94.45	208.00	92.09	207.56	90.69	207.13	89.77	206.72	89.14	206.33	88.68
70	208.20	92.72	207.29	88.71	206.47	86.54	205.70	85.24	204.97	84.39	204.28	83.82
60	207.90	90.98	206.54	85.24	205.32	82.31	204.18	80.63	203.12	79.60	202.11	78.92
50	207.63	89.48	205.80	81.80	204.16	78.07	202.65	76.01	201.24	74.79	199.92	74.02
40	207.49	89.00	205.12	78.60	203.05	73.89	201.15	71.41	199.38	69.98	197.73	69.10
30	207.66	92.47	204.68	76.50	202.13	70.11	199.81	66.96	197.67	65.23	195.68	64.20
20	208.50	123.06	204.79	81.93	201.69	69.07	198.91	63.61	196.36	60.94	194.00	59.48

tion of the line-end design rule. The table shows that necking makes the device leaky and that leakage current increases or decreases with line-end extension length. In particular, when the necking occurs near the channel edge—e.g., y_{min}=0 or 10 nm—I_{off} increases substantially for all line-end extension lengths. This is because the minimum linewidth of the necking is already enclosed by the channel as a result of overlay error.

The bold italic entries in Table 4 show the cases where the I_{off} increase remains within 10% of the 100-nm LEE

Table 4 I_{on} and I_{off} changes with line-end extension and necking for 200-nm width NMOS.

	Necking location [$y_{l_{min}}$ in Fig. 5(c)] from gate edge (nm) for 100-nm LEE. l_{min}=40 nm.											
	0		10		20		30		40		50	
Lee (nm)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)	I_{on} (μA)	I_{off} (nA)
100	210.13	***115.79***	209.23	***100.30***	208.95	***97.16***	208.92	***96.93***	208.92	***96.94***	208.92	***96.94***
90	210.89	130.13	209.95	113.58	209.11	***96.29***	208.88	***96.88***	208.87	***96.78***	208.87	***96.78***
80	211.14	133.49	210.67	126.81	209.77	111.35	208.98	***98.37***	208.82	***96.63***	208.81	***96.61***
70	211.15	133.88	210.86	129.48	210.43	123.34	209.58	109.07	208.86	***97.55***	208.75	***96.41***
60	211.08	133.63	210.83	129.59	210.56	125.33	210.17	119.70	209.38	106.73	208.74	***96.84***
50	211.00	133.33	210.75	129.26	210.50	125.20	210.24	121.02	209.89	115.84	209.17	***104.33***
40	210.96	133.54	210.66	129.09	210.40	124.85	210.14	120.72	209.89	116.55	209.58	111.73
30	211.12	136.49	210.71	130.52	210.35	125.26	210.04	120.53	209.76	116.13	209.50	111.88
20	211.82	157.95	211.21	143.61	210.65	132.59	210.16	124.05	209.73	117.30	209.37	111.79

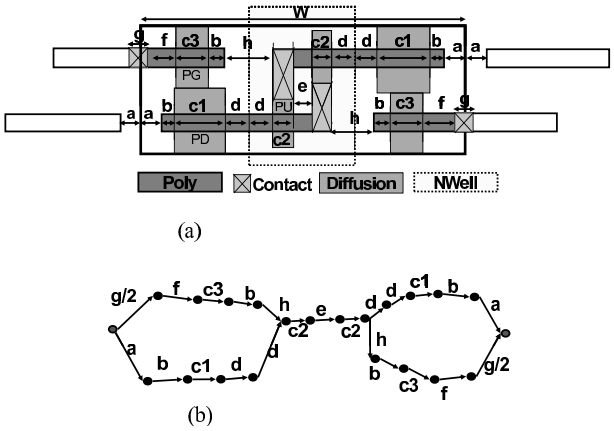

Fig. 8 SRAM layout and width constraint graph. (a) 6-T SRAM bitcell layout. (b) Width-constraint graph.

cases. As the necking location moves farther from the channel edge, we can reduce LEE further. Table 4 implies that if we cannot avoid necking shapes, the necking location must be placed at least as far as the maximum overlay error from the channel edge.

From all our experiments, we observe that as line-end extension length is reduced from 100 nm, I_{on} and I_{off} are also reduced, due to reduced line-end capacitance. However, with tapering or necking effects, if the small linewidth of the line-end segments is situated within the channel area due to overlay error, I_{off} increases significantly. We also observe that the impact of line-end extension itself is negligibly small due to the electrical characteristics, but that in combination with line-end pullback and overlay error, small-linewidth line-end segments lead to large variation in I_{on} and I_{off}.

From our observations, the desirable attributes of line-end shapes can be summarized as follows:

- Larger n is preferred to suppress I_{off} variation. With larger n, we can further reduce the line-end extension length.
- Bulge may be the best line-end extension shape for I_{off}, since it can reduce I_{off} of the most leaky part (near gate edge) of a gate.
- Necking shape always increases I_{off}. Hence, necking should be avoided in line-end shaping. If we cannot avoid necking, the necking location must be away from the channel edge, although increasing line-end extension length.

5 Case Study 1: Area versus Leakage Trade-off

We now analyze how line-end shaping affects design area and leakage current.

5.1 *SRAM Bitcell*

Figure 8(a) shows an example of a 6-T SRAM bitcell layout, while Fig. 8(b) shows the corresponding layout constraint graph that defines the width of the bitcell. In the figure, a is half the line-end gap; b is the length of the line-end extension; and $c1$, $c2$, and $c3$ are the respective widths of pulldown (PD), pullup (PU), and passgate (PG) transistors. Also, d is the space rule between diffusion and N-well, e is the space between diffusion patterns, f is the space between contact and diffusion, g is the width or height of a contact, and h is the space between poly and contacts of a different net. Since the line-end extension (b) occurs twice in the critical path of this width constraint graph, when we reduce the length of the line-end extension by x, the bitcell width decreases by $2x$, and this will reduce the bitcell area.

Table 5 Design rules from the Nangate 45-nm Open Cell library (Ref. 19) and the width of transistors in an SRAM bitcell.

Rule name	Minimum rule
Half line-end gap (a)	50 nm
Diffusion-to-N-well space (d)	55 nm
Diffusion-to-diffusion space (e)	80 nm
Contact-to-diffusion space (f)	60 nm
Contact width (height) (g)	50 nm
Poly-to-contact space (h)	90 nm
Transistor	**Minimum width**
Pull-up ($c2$)	60 nm
Pull-down ($c1$)	120 nm
Pass-gate ($c3$)	60 nm

We evaluate the area and leakage current of a bitcell by changing the sharpness as well as the length of the line-end extension. Table 5 shows the design rules for a 45-nm technology that we use,[19] along with the assumed transistor width values. Figure 9 shows the trade-off curve under the given design rules.

The I_{off} value in the figure is the total leakage current of all transistors, i.e., two PD, two PG and two PU transistors, in the bitcell. To calculate PU (PMOS) leakage current, we assume that unit-width leakage of the PMOS is half that of NMOS. We also assume that the line-end extension length of PUs is fixed, since it is determined by other fixed design

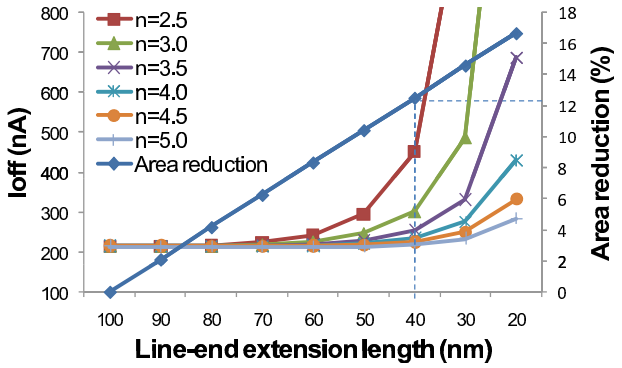

Fig. 9 Area-leakage trade-off for an SRAM bitcell.

Table 6 SRAM bitcell area reduction (%) under allowed leakage increase (%).

	Allowed leakage increase (%)					
n	10	30	60	100	200	300
2.5	6.25	8.33	10.42	10.42	12.50	12.50
3.0	8.33	10.42	12.50	12.50	14.58	14.58
3.5	10.42	12.50	14.58	14.58	14.58	16.67
4.0	12.50	14.58	14.58	16.67	16.67	16.67
4.5	12.50	14.58	16.67	16.67	16.67	16.67
5.0	14.58	14.58	16.67	16.67	16.67	16.67

rules—i.e., *e* and *d*—and cannot be reduced further without disconnecting electrodes. Table 6 shows SRAM bitcell area reduction due to the line-end extension reduction under given leakage power constraints. If we permit a factor of 2 leakage increase as shown in column 5, we can reduce the line-end design rule to approximately 40 to 20 nm, and reduce the bitcell size by 10.42% to 16.67%, depending on the super-ellipse exponent.

5.2 *Standard Cell Logic*

Similar to the SRAM bitcell, we analyze the standard cell logic area and leakage current based on the line-end extension length and the sharpness of tapering. We take an inverter cell as being representative of standard cells. Figure 10(a) shows the basic layout structure of a standard inverter cell; Fig. 10(b) shows the corresponding height constraint graph. The notation is the same as that given for the SRAM bitcell except that *c*1 and *c*2 are the gate widths of NMOS and PMOS transistors, respectively. Figure 11 shows the trade-off curve under the given design rules for 45-nm technology. We assume NMOS and PMOS widths of 400 nm and 600 nm, respectively, and that unit-width leakage current of PMOS is half that of NMOS. Unlike in the SRAM case, the line-end extension length of PMOS devices can also be reduced. Due to the relatively large transistor sizes in a logic cell, impact of line-end extension length is smaller than in a bitcell. Table 7 shows standard cell area reduction due to the line-end extension length reduction under given leakage power constraints. In general, each logic cell has its own width but shares a common cell height with all other cells. Hence, the area reduction due to cell height reduction observed in the inverter example applies equally to all standard cells. From Fig. 11 and Table 7, if a factor of 2 leakage increase is allowed, 9.52% to 10.88% of the logic area can be reduced by line-end design rule relaxation.

6 Case Study 2: Design-Rule versus OPC/Litho Cost versus Leakage Trade-off

Our electrical models also enable fast analysis of the post-litho line-end shapes, and thus can be used to evaluate various design rules and OPC/litho parameters in terms of the resulting area and leakage current.

6.1 *Experimental Setup*

OPC cost can be measured by the runtime and data size resulting from the number of fragmentations. The following parameters from the "Calibre Model-Based OPC User's Manual,"[20] shown in Fig. 12, control the fragmentation of the line-end extension OPC treatment:

- **lineEndLength.** This parameter defines the distance criteria used to determine whether a fragment is a line

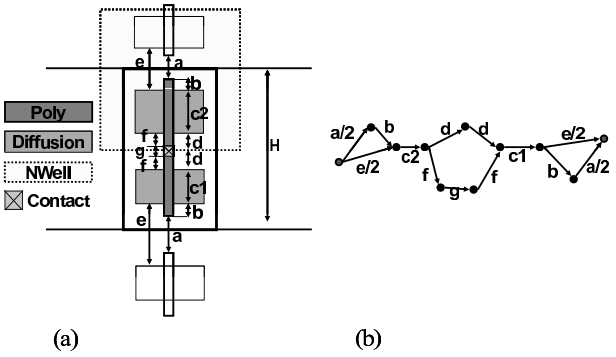

Fig. 10 Inverter cell layout and height constraint graph. (a) Standard logic layout. (b) Height constraint graph.

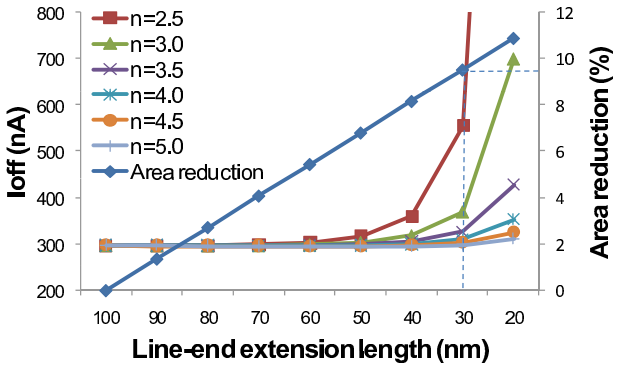

Fig. 11 Area-leakage trade-off for a logic cell.

Table 7 Logic area reduction (%) under allowed leakage increase (%).

	Allowed leakage increase (%)					
n	10	30	60	100	200	300
2.5	6.80	8.16	8.16	9.52	9.52	9.52
3.0	8.16	9.52	9.52	9.52	10.88	10.88
3.5	9.52	9.52	10.88	10.88	10.88	10.88
4.0	9.52	10.88	10.88	10.88	10.88	10.88
4.5	10.88	10.88	10.88	10.88	10.88	10.88
5.0	10.88	10.88	10.88	10.88	10.88	10.88

end. A line end is defined as an edge that is shorter than or equal to *lineEndLength* and between two convex corners, each of which is longer than or equal to the *lineEndLength* parameter. Any line-end edge will be treated differently than others.

- **lineEndAdjDist**. This parameter specifies the distance from the line-end edge determined by *lineEndLength*. Parts of edges within the distance to the line-end specified by this parameter will be fragmented differently from other parts of the edges.
- **cornedge**. This parameter specifies detailed fragmentation locations via options **lea** *lead*1 … *leadN*. *lead*1 … *leadN* specify the fragmentation locations from line-end adjacent convex corners. The values *lead*1 … *leadN* are the distances to a vertex from the previous vertex, as shown in Fig. 12.

We use the following optical models and process corners for OPC and lithography simulation to produce 38-nm and 52-nm CD values at the best- and worst-case corner, respectively:

- **Optical model.** We use λ=193 nm, NA=1.2, and an annular-type illuminator with 0.7 and 0.5 for sigma and inner-sigma, respectively. We use a constant threshold (CTR) model of 0.25 for both OPC and lithography.

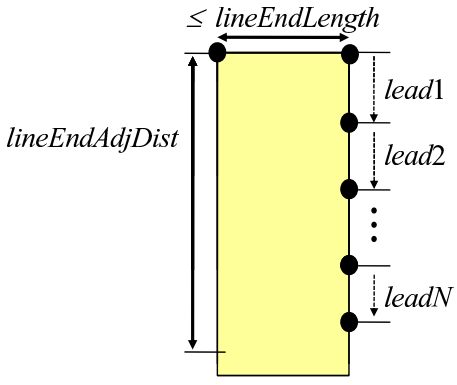

Fig. 12 OPC parameters for line-end fragmentation.

- **Process corner.** We set +10-nm (depth of focus) DOF and +2% higher dose for the best-case corner and −10-nm DOF and −3% lower dose for the worst-case corner.

We permute the following parameters for OPC/litho simulations:

- **Number of fragmentations** (N_f). This directly affects the cost of OPC and lithography. We evaluate five different numbers (i.e., 0, 1, 2, 3, and 4) of fragmentations with 100-nm *lineEndAdjDist*.
- **Fragmentation locations.** We permute all possible fragmentation locations for each number of fragmentations with 10-nm minimum fragment length. (For N_f=1, we evaluate 10 different fragmentation locations, from 10 nm to 100 nm. For N_f=2, we sweep the location of the first fragmentation (*lead*1) from 10 nm to 90 nm, and we sweep the location of the second fragmentation (*lead*2) from 10 nm to '100 nm−*lead*1' from the first fragmentation location. Similarly, we examine all possible different combinations of fragmentation locations for N_f=3 or 4. The numbers of different cases are 1, 10, 45, 120, and 210 for N_f=0, 1, 2, 3, and 4, respectively.)

We implement a layout that contains various cases of line-end extension (LEE) length and line-end gap (LEG) values and apply different OPC parameters as explained earlier. The layout contains 100 (10×10) different combinations of line-end extension length and line-end gap. The distance between patterns from different LEE and LEG combinations is approximately 10 μm to suppress interference between them. Each pattern consists of two groups of 11 parallel poly lines, as shown in Fig. 13, and the shape of the center line among the 11 lines is our concern. The separation distance between the two groups follows specified line-end gap values varying from 10 μm to 100 μm. Patterns are designed based on the design rules used in the "NanGate 45 nm Open Cell Library;"[19] poly-to-poly pitch is 190 nm, gate length (CD) is 45 nm, and poly length is

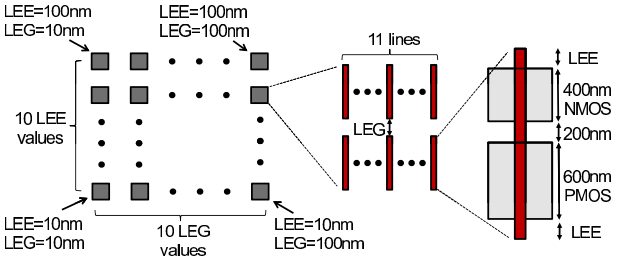

Fig. 13 Layout of the test patterns for OPC/litho simulation.

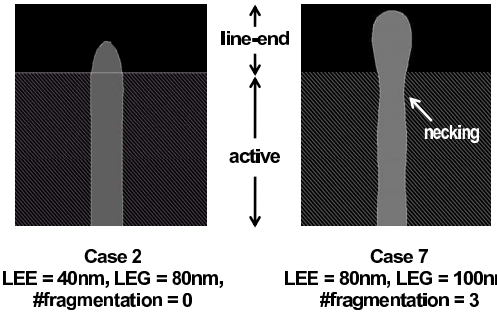

Fig. 14 Litho images for cases 2 and 7 in Table 8.

determined by the sum of 1200 nm (400-nm NMOS, 600-nm PMOS, and 200 nm of diffusion space between NMOS and PMOS) and 2× LEE.

6.2 *Experimental Results and Discussion*

We analyze results from a total of 115,800 cases (=3 process corners × 100 different design rules × 386 different fragmentations) in this section.

6.2.1 *Evaluation of traditional line-end shape metrics*

Our first analysis evaluates the electrical characteristics of traditional line-end shape metrics, such as linewidth at the gate edge (*LW0*) and corner rounding of line-end. *LW0* has long served as the most important parameter in the traditional line-end metric. However, *LW0* is not a sufficient metric to estimate electrical characteristics of a device. Table 8 shows how I_{off} can vary for the same *LW0* value, i.e., 45 nm. The large I_{off} variation in Table 8 is caused by the different shapes, especially necking location, due to the different design rules and fragmentations in OPC. Figure 14 shows the shapes of poly lines corresponding to cases 2 and 7 in Table 8. Necking in the channel can significantly increase I_{off}, even when *LW0* matches the target linewidth.

We note that I_{off} of case 7 is larger than that of case 2, although case 7 has higher OPC cost due to the larger number of fragmentations and has better corner rounding compared to case 2. In other words, less tapering, which is regarded as good in the traditional line-end metric, does not necessarily correspond to better electrical characteristics.

6.2.2 *I_{off} variation versus process variation*

We also evaluate I_{off} variation at different process corners. Figure 15 shows I_{off} variations at best/nominal/worst-case process corners with respect to LEG design rules. I_{off} values increase by an order of magnitude from worst-case to nominal-case and from nominal-case to best-case corner. This I_{off} increase can be explained from Fig. 16, which shows the litho contours for best-case (red), nominal-case (yellow), and worst-case (green) process corners, for 10-nm, 50-nm, and 100-nm LEG rules (color online only). We can observe that litho contours shrink when the process corner changes from worst-case to best-case, and this results in continuous I_{off} increase.

We observe a 2× increase in I_{off} at the best-case corner for the 50-nm LEG rule in Fig. 15, although nominal-or worst-case corners do not show significant I_{off} variation.

Table 8 I_{off} variation for the same 45 nm of linewidth at the gate edge (LW0).

	Design rule				
Case	LEE (nm)	LEG (nm)	No. fragmentations	LW0	I_{off} (nA)
1	80	30	0	45	151
2	40	80	0	45	115
3	90	100	1	45	153
4	100	90	1	45	164
5	100	80	2	45	144
6	100	80	3	45	152
7	80	100	3	45	191
8	90	90	4	45	162
9	100	100	4	45	121

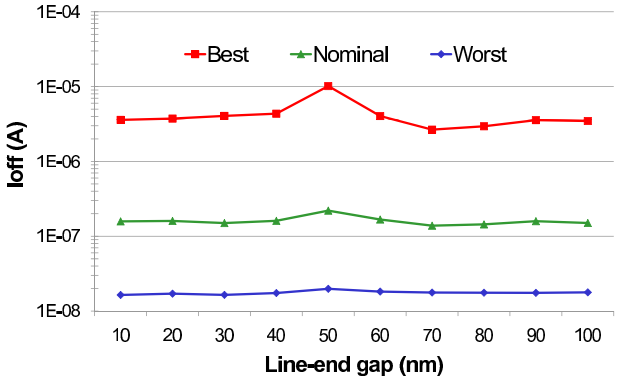

Fig. 15 I_{off} variations at best/nominal/worst-case process corners with respect to LEG design rules.

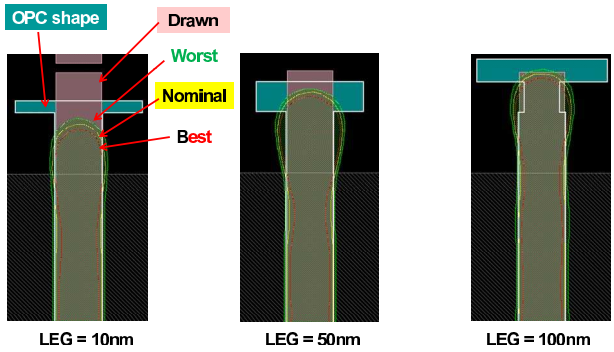

Fig. 16 Litho contours at best-case (red), nominal-case (yellow), and worst-case (green) process corners, for 10-nm, 50-nm and 100-nm LEG rules. (Color online only.)

Again, even though 100-nm LEG shows the smallest *LW0*, 50-nm LEG results in the largest I_{off}. Ignorable necking for 50-nm LEG at the nominal- and worst-case corners becomes severe at the best-case corner, as shown in Fig. 16.

6.2.3 *Optimal OPC setup*

As explained earlier, traditional line-end metrics do not correctly represent the electrical characteristics of transistors. For better electrical characteristics, we evaluate various OPC parameters and seek to find the OPC setup that has the best electrical performance—e.g., least I_{off}.

For each number of fragmentations (N_f), we find the optimal fragmentation location that has the minimum I_{off} under given design rules—i.e., LEE=100 nm and LEG =100 nm. Table 9 shows the best fragmentation locations—i.e., with smallest I_{off}—for different N_f. We observe that a larger number of fragmentations results in smaller I_{off} for a given design rule. We can also observe that fragmentations near the gate edge are better to minimize I_{off} for 100-nm LEE and LEG design rules.

However, a larger number of fragmentations leads to larger OPC runtime (as well as larger post-OPC data). Figure 17 shows a near-linear relationship between the number of fragmentations and the runtime. For this experiment, we generate a test case that contains 100 K poly lines, and perform OPC/litho simulations by changing the number of fragmentations for only the line-end extension from 1 to 10. We do not introduce any fragmentation for edges that are not in the line-end extension. From Table 9 and Fig. 17, designers can explicitly trade OPC cost and I_{off}.

6.2.4 *Optimal design rules and OPC setup*

Last, to quantify the cost of design rule parameters—i.e., LEE and LEG—we introduce as a metric the normalized area of a logic cell, parameterized with LEE and LEG values, as

$$C_{v_1,v_2} = H_{v_1,v_2}/H_{100,100}$$

where H_{v_1,v_2} represent the height of a single logic cell when LEE and LEG are v_1 and v_2. Logic cell height is a function of LEE and LEG; the height is calculated as a sum of NMOS width, PMOS width, space between NMOS and PMOS, two times LEE, and one LEG. $H_{100,100}$ is 1500 (=400+600+200+2×100+100), which is used as a reference area value. According to the LEE and LEG ranges in our experiment, C_{v_1,v_2} is calculated in Table 10. From the

Table 9 Best fragmentation locations when I_{off} for LEE=100 nm and LEG=100 nm.

Best fragmentation locations					I_{off}
	*lead*1	*lead*2	*lead*3	*lead*4	(nA)
No. frag.	(nm)	(nm)	(nm)	(nm)	
0	—	—	—	—	151
1	80	—	—	—	148
2	90	10	—	—	140
3	70	20	10	—	133
4	60	10	10	20	121

Table 10 Normalized area (%), $C_{LEE,LEG}$ according to LEE and LEG design rules, relative to the area when both LEE and LEG are 100 nm.

	LEG									
LEE	10	20	30	40	50	60	70	80	90	100
100	94	95	95	96	97	97	98	99	99	100
90	93	93	94	95	95	96	97	97	98	99
80	91	92	93	93	94	95	95	96	97	97
70	90	91	91	92	93	93	94	95	95	96
60	89	89	90	91	91	92	93	93	94	95
50	87	88	89	89	90	91	91	92	93	93
40	86	87	87	88	89	89	90	91	91	92
30	85	85	86	87	87	88	89	89	90	91
20	83	84	85	85	86	87	87	88	89	89
10	82	83	83	84	85	85	86	87	87	88

table, we can easily obtain the area reduction from LEE and LEG design rule changes.

Although we find the best OPC parameters for given LEE and LEG values in the previous section, the best OPC parameters can vary with the applied design rules. We evaluate the best combinations of design rules and OPC parameters. From our all simulation results, we again find the best OPC parameters (i.e., fragmentation options) that result in the smallest I_{off} in any combination of LEE and LEG design rules. Table 11 shows arrays of I_{off} values that contain smallest I_{off} value among all different fragmentation locations for different number of fragmentations. I_{off} values are obtained at the nominal-case corner, but the best fragmentation locations do not change at worst-case or best-case corners. We do not calculate I_{off} for catastrophic error cases, such as bridging, line-end shortening, and broken lines, when those errors appear in any of our best/nominal/worst-case process corners and in any of 11 parallel lines in our test block, as shown in the center of Fig. 13. Figure 18 shows examples of these catastrophic errors. In general, a bridging error occurs when LEG is very small and not enough fragmentations are performed. Line-end shortening is mainly due to small LEE. Broken lines are an extreme case of necking that occurs when large hammerhead OPC serifs are generated. (However, it is difficult to categorize the exact mechanisms of these errors, since the errors do not occur consistently with monotonic variation of OPC/litho and design rule parameters.) In Table 11, B, S, and F denote bridging, line-end shortening, and broken lines, respectively. O is used when a too-small linewidth that is out of bounds for our model is introduced in the channel.

Our observations are summarized as follows:

- The minimum I_{off} value is 115, 108, 102, 108, and 103 nA, for N_f=0, 1, 2, 3, and 4, respectively.
- Considering OPC cost, a larger number of fragmentations does not effectively reduce the I_{off}. Especially, there is an 8× increase in I_{off} when the number of fragmentations is 4 and LEG is 20 nm, compared to

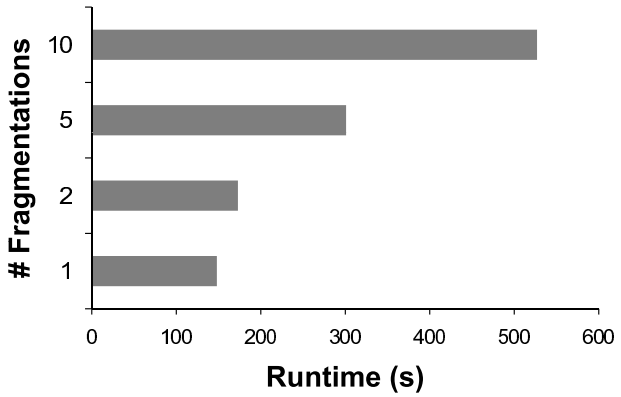

Fig. 17 OPC/litho simulation runtime due to the number of fragmentations.

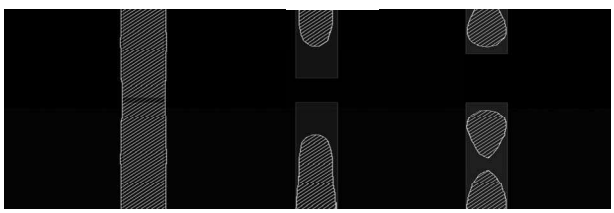

Fig. 18 Lithographic errors at the line-end. (a) Bridging, (b) line-end shortening, and (c) broken.

Table 11 I_{off} (nA) with respect to the LEE and LEG design rules for the best fragmentation location cases that lead to smallest I_{off} for each number of fragmentations, 0, 1, 2, 3, and 4, respectively. B, S, and F denote bridging, line-end shortening, and broken lines, respectively. O represents too small linewidth, which is out of our modeling boundary.

Number of fragmentations (N_f)=0

	LEG									
LEE	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
100	B	153	156	B	B	B	159	121	141	151
90	B	150	153	B	B	B	155	120	140	150
80	B	148	151	B	B	B	152	120	137	149
70	B	165	154	B	B	B	149	119	134	147
60	B	S	O	B	B	B	147	117	131	144
50	B	S	S	B,S	B,S	B	145	116	128	141
40	B	S	S	B,S	B,S	B,S	145	**115**	125	138
30	B	S	S	B,S	B,S	B,S	O	O	O	O
20	B	S	S	B,S	B,S	B,S	S	S	O	O
10	B	S	S	B,S	B,S	B,S	S	S	S	S

Number of fragmentations (N_f)=1 (*lead*1=60 nm)

	LEG									
LEE	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
100	B	224	220	376	189	181	145	162	164	152
90	B	220	212	340	185	176	146	159	162	153
80	B	216	213	370	180	172	140	156	159	150
70	B	209	207	330	175	168	140	151	156	148
60	B	204	200	353	172	164	136	147	153	145
50	B,S	O	O	310	162	160	132	142	148	142
40	B,S	S	S	347	161	151	**108**	138	144	139
30	B,S	S	S	342	O	O	O	135	O	O
20	B,S	S	S	S	O	O	O	O	O	O
10	B,S	S	S	S	S	S	S	S	S	S

Table 11 (*Continued.*)

Number of fragmentations (N_f)=2 (*lead*1=10 nm, *lead*2=30 nm)

	LEG									
LEE	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
100	B	160	150	161	220	167	139	144	159	150
90	B	157	148	159	216	165	136	142	158	156
80	B	152	149	154	208	164	135	138	156	157
70	B	147	145	151	203	161	131	136	154	162
60	B	O	O	O	198	156	128	132	148	158
50	B,S	S	S	S	194	145	123	132	148	161
40	B,S	S	S	S	187	130	114	122	144	149
30	B,S	S	S	S	S	126	109	117	138	145
20	B,S	S	S	S	S	O	**102**	O	130	140
10	B,S	S	S	S	S	S	S	O	S	O

Number of fragmentations (N_f)=3 (*lead*1=10 nm, *lead*2=10 nm, *lead*3=20 nm)

	LEG									
LEE	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
100	B	155	160	173	181	135	149	152	156	166
90	B	154	157	169	179	135	146	150	167	183
80	B	149	154	165	178	132	145	149	159	191
70	B	145	147	161	173	129	142	147	163	194
60	B	352	186	186	168	125	138	142	160	191
50	B,S	S	S	S	163	119	133	137	155	188
40	B,S	S	S	S	S	116	123	134	146	182
30	B,S	S	S	S	S	110	117	130	142	178
20	B,S	S	S	S	S	**108**	113	122	137	173
10	B,S	S	S	S	S	O	O	O	O	O

Table 11 (*Continued.*)

Number of fragmentations (N_f)=4 (*lead*1=60 nm, *lead*2=10 nm, *lead*3=10 nm, *lead*4=20 nm)

	LEG									
LEE	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
100	B	831	F	F	F	370	207	175	160	121
90	B	821	F	F	F	403	223	181	162	122
80	B	831	F	F	F	412	223	180	162	119
70	B,S	858	F	F	F	416	222	177	163	116
60	B,S	S	F	F	F	416	216	174	160	112
50	B,S	S	F,S	F	F	408	209	170	160	109
40	B,S	S	F,S	F,S	F	404	206	164	157	107
30	B,S	S	F,S	F,S	F	410	207	162	151	103
20	B,S	S	F,S	F,S	F,S	O	552	204	155	109
10	B,S	S	F,S	F,S	F,S	S	S	S	S	S

the minimum I_{off}. This is due to very narrow tapering, as shown in Fig. 19.

- The minimum I_{off} is found when the number of fragmentations is 2 with *lead*1=10 nm and *lead*2 =30 nm.
- Optimal LEE and LEG design rules corresponding to the minimum I_{off} are 20 nm and 70 nm respectively, which can result in 13% area reduction according to Table 10. However, it may be risky to adopt a design rule that is near values resulting in catastrophic errors.

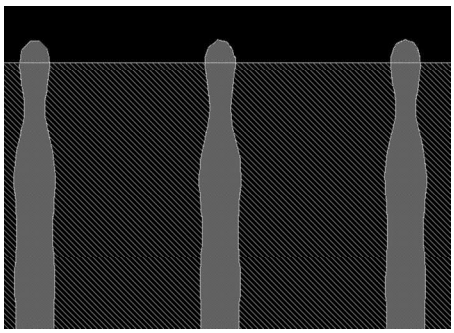

Fig. 19 Significant tapering when the number of fragmentations is 4 and LEG is 20 nm.

If we add 20 nm of margin to the LEE design rule to avoid risky design rules, we still reduce the area by around 10%.

- Larger LEE and LEG do not always result in smaller I_{off}. The LEG values that produce smallest I_{off} are 80, 70, 70, 60, and 100 nm for N_f=0, 1, 2, 3, and 4, respectively.

7 Conclusions and Ongoing Work

We have proposed a novel modeling framework to model the electrical impact of line-end shapes. We model a line-end shape by a general super-ellipse equation. We model the capacitance between the line-end and the gate channel and derive I_{on} and I_{off} models from it, considering overlay error in the manufacturing process. Our model accuracy is within 0.47% and 1.28% for I_{on} and I_{off}, respectively, compared to 3-D TCAD simulation. Our results show that different line-end extension lengths can affect I_{on} and I_{off} by 4.5% and 30%, respectively, and that different line-end shapes, combined with overlay error, can increase I_{off} by several times compared to the ideal line-end shape.

Our electrical model enables fast and accurate evaluations of various line-end shapes, given the results of large-sized design of experiments. Applying our model to SRAM bitcell and inverter cell layout, we observe that the tradi-

tional line-end extension design rule can be reduced further without affecting electrical characteristics of circuits. We also evaluate the trade-offs among design rules and the resulting area, OPC/litho parameters, and I_{off}. From the analyses, we show the potential for optimal design rules and OPC/litho parameters that can minimize I_{off} and reduce layout area by more than 10%.

Our next goals are (1) to find a systematic methodology for small-sized design of experiments to derive the optimal OPC and design rules, and (2) to provide rules of thumb for the optimal line-end shaping so that designers and lithographers can easily find optimal solutions according to their own OPC/lithography/design rules and device characteristics.

Acknowledgments

A preliminary version of this work appeared in Ref. 9, where an electrical model of post-litho transistor shapes including line-end shapes was proposed based on Synopsys DaVinci[TS] simulations for 65-nm gate length transistors. Extensions beyond Ref. 9 include accurate capacitance characterization using a 3-D RC extractor Synopsys Raphael, new simulation results for 45-nm gate length transistors using Synopsys Sentaurus, and electrical and lithographic evaluations of OPC/litho parameters and line-end design rules using the proposed 45-nm line-end models.

References

1. A. P. Balasinski, L. Karklin, and V. Axelrad, "Impact of subwavelength CD tolerance on device performance," in *Design, Process Integration and Characterization for Microelectronics*, *Proc. SPIE* **4692**, 361–368 (2002).
2. R. Giacomini and J. A. Martino, "Modeling silicon on insulator MOS transistors with nonrectangular-gate layouts," *J. Electrochem. Soc.* **132**, G218–G222 (2006).
3. F.-L. Heng, J.-F. Lee, and P. Gupta, "Toward through-process layout quality metrics," in *Design and Process Integration for Microelectronic Manufacturing*, *Proc. SPIE* **5756**, 161–167 (2005).
4. S. D. Kim, H. Wada, and J. C. S. Woo, "TCAD-based statistical analysis and modeling of gate line-edge roughness effect on nanoscale MOS transistor performance scaling," *IEEE Trans. Semicond. Manuf.* **17**(2), 192–200 (2004).
5. K. Koike, K. Nakayama, K. Ogawa, and H. Ohnuma, "Optimization of layout design and OPC by using estimation of transistor properties," in *Photomask and Next-Generation Lithography Mask Technology*, *Proc. SPIE* **6183**, 62830O (2006).
6. R. C. Pack, V. Axelrad, A. Shibkov, V. V. Boksha, J. A. Huckabay, R. Salik, W. Staud, R. Wang, and W. D. Grobman, "Physical and timing verification of subwavelength-scale designs: I. lithography impact on MOSFETs," in *Design and Process Integration for Microelectronic Manufacturing*, *Proc. SPIE* **5042**, 51–62 (2003).
7. W. J. Poppe, L. Capodieci, J. Wu, and A. Neureuther, "From poly line to transistor: building BSIM models for non-rectangular transistors," in *Design and Process Integration for Microelectronic Manufacturing IV*, *Proc. SPIE* **6156**, 61560P (2006).
8. C. Pacha, M. Bach, K. V. Arnim, R. Brederlow, D. S. Lansiedel, P. Seegebrecht, J. Berthold, and R. Thewes, "Impact of STI-induced stress, inverse narrow width effect and statistical V_{th} variations on leakage current in 120 nm CMOS," in *Proc. European Solid-State Device Research Conference*, pp. 397–400 (2004).
9. P. Gupta, K. Jeong, A. B. Kahng, and C.-H. Park, "Electrical metrics for lithographic line-end tapering," in *Photomask and Next-Generation Lithography Mask Technology XV*, *Proc. SPIE* **7028**, 70283A (2008).
10. P. Gupta, A. B. Kahng, Y. Kim, S. Shah, and D. Sylvester, "Modeling of non-uniform device geometries for post-lithography circuit analysis," in *Design Process Integration for Microelectronic Manufacturing IV*, *Proc. SPIE* **6156**, 61560U (2006).
11. R. Singhal, A. Balijepalli, A. Subramaniam, F. Liu, S. Nassif, and Y. Cao, "Modeling and analysis of non-rectangular gate for post-lithography circuit simulation," in *Proc. Design Automation Conference*, pp. 823–828 (2007).
12. P. Gupta, A. B. Kahng, Y. Kim, S. Shah, and D. Sylvester, "Investigation of diffusion rounding for post-lithography analysis," in *Proc. Asia and South Pacific Design Automation Conference*, pp. 480–485 (2008).
13. Synopsys, Inc., "Raphael user's guide," version V-2004.06, available at http://www.synopsys.com/.
14. Synopsys, Inc., "Sentaurus user's guide," version A-2007.12-SP1, available at http://www.synopsys.com/.
15. Synopsys, Inc., DaVinci, version 2006.06. SP1, available at http://www.synopsys.com/.
16. The MathWorks, Inc., MATLAB, version 7.2.0.294 (R2006a), available at http://www.mathworks.com/.
17. "BSIM4.6.4 user's manual," available at http://www-device.eecs.berkeley.edu/~bsim3/BSIM4/BSIM464/BSIM464_Manual.pdf.
18. International Technology Roadmap for Semiconductors, available at http://public.itrs.net/.
19. Nangate, Inc., "45 nm Open Cell Library," available at http://www.nangate.com/.
20. Mentor Graphics, "Calibre model-based OPC user's guide," version 2008.3_34.24, available at http://www.mentor.com/.

Puneet Gupta is currently a faculty member of the Electrical Engineering Department at UCLA. He received his B.Tech degree in electrical engineering from the Indian Institute of Technology, Delhi, in 2000 and his PhD in 2007 from the University of California, San Diego. He cofounded Blaze DFM, Inc. (acquired by Tela, Inc.) in 2004 and served as its product architect until 2007. He has authored over 60 papers, six U.S. patents, and a book chapter. He is a recipient of the NSF Career Award, ACM/SIGDA Outstanding New Faculty Award, and IBM PhD Fellowship and European Design Automation Association Outstanding Dissertation Award. Dr. Gupta has given tutorial talks at the DAC, ICCAD, International VLSI Design Conference, and SPIE Advanced Lithography Symposium. He has served on the technical program committees of DAC, ICCAD, ASP-DAC, ISQED, ICCD, SLIP, and VLSI Design. He served as the program chair of the IEEE DFM&Y Workshop in 2009 and 2010. Dr. Gupta's research has focused on building high-value bridges between physical design and semiconductor manufacturing for lowered cost, increased yield, and improved predictability of integrated circuits.

Kwangok Jeong received BS and MS degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1997 and 1999, respectively. He worked on the Computer-Aided Engineering Team at Samsung Electronics from 1999 to 2006. During his work at Samsung Electronics, he received three Best Paper Awards at the Samsung Technical Conference in 2001, 2002, and 2004, respectively, and an Honorable Outstanding Researcher Award in 2005. He joined the VLSI CAD Laboratory at UC San Diego as a PhD student in 2006. His research interests include physical design and the VLSI design-manufacturing interface.

Andrew B. Kahng received his AB degree in applied mathematics (physics) from Harvard College and MS and PhD degrees in computer science from the University of California at San Diego, La Jolla. He joined the UCLA Computer Science Department as an assistant professor in 1989 and became an associate professor in 1994 and a full professor in 1998. In 2001, he joined UCSD as a professor in the CSE and ECE Departments. He served as associate chair of the UCSD CSE Department from 2003 to 2004. Professor Kahng was the founding general chair of the 1997 ACM/IEEE International Symposium on Physical Design and cofounder of the ACM Workshop on System-Level Interconnect Prediction, and he defined the physical design roadmap as a member of the Design Tools and Test Technology Working Group (TWG) for the 1997, 1998, and 1999 renewals of the International Technology Roadmap for Semiconduc-

tors. From 2000 through 2003, he was chair of both the U.S. Design Technology Working Group and of the Design International Technology Working Group, and he continues to serve as cochair of the Design ITWG. He has been an executive committee member of the MARCO Gigascale Systems Research Center since its inception in 1998. In 2004, Professor Kahng cofounded Blaze DFM, Inc., and served as CTO of the company until resuming his duties at UCSD in 2006. Professor Kahng has published over 300 journal and conference papers. He has received NSF Research Initiation and Young Investigator Awards, 13 Best Paper nominations, and 6 Best Paper Awards. Since 1997, his research in IC design for manufacturability has pioneered methods for automated phase-shift mask layout, variability-aware analyses and optimizations, CMP fill synthesis, and parametric yield-driven, cost-driven methodologies for chip implementation.

Chul-Hong Park is a principal engineer at the Semiconductor R&D Center of Samsung Electronics. He currently leads the Integration of Design and Technology (IDT) team, which has developed computational design rule and computational lithography solutions. He received BS and MS degrees in mathematics from Kyung Hee University, and his PhD degree in electrical and computer engineering from the University of California at San Diego, La Jolla. He received a 1998 Honorable Outstanding Researcher Award and two Best Paper Awards at Samsung Electronics. He also received a 2009 SRC Inventor Recognition Award. He has published over 40 journal and conference papers and is the holder of 7 patents. His research interests mainly include nanometer physical design, design for manufacturing, integration of transistor/layout/circuit, and design/lithography for emerging technologies.