Subwavelength Optical Lithography: Challenges and Impact on Physical Design*

A. B. Kahng and Y. C. Pati†

UCLA Department of Computer Science, Los Angeles, CA 90095-1596 USA
†Numerical Technologies, Inc., Santa Clara, CA 95051 USA

Abstract

We review the implications of subwavelength optical lithography for new tools and flows in the interface between layout design and manufacturability. After discussing the necessity of corrections for optical process effects (i.e., use of optical proximity correction (OPC) and phase-shifting masks (PSM)), we focus on the implications of OPC and PSM for layout and verification methodologies. Our discussion addresses the necessary changes in the design-to-manufacturing flow, including infrastructure development in the mask and process communities as well as opportunities for research and development in physical layout and verification.

1 Introduction

As CMOS technology advances according to the SIA NTRS [34], manufacturing cost increasingly drives design [23]. Process engineers must achieve predictability and uniformity of manufactured device and interconnect attributes, e.g., dopant concentrations, channel lengths, interconnect dimensions, contact shapes and parasitics, and interlayer dielectric thicknesses. To achieve a design solution at a reasonable point on the price-performance curve, a total *variability budget* for the design must be distributed among such attributes. In very deep submicron technologies, attaining large process windows and uniform manufacturing is difficult [1] [8] [31] [14] [23] [4], and the manufacturing process has an increasingly constraining effect on physical layout design and verification. Of course, many physical design methods have been proposed to address various manufacturing issues such as registration errors, photolithographic random effects, random spot defects, plasma and charging effects ("antenna effect"), etc.; see such works as [22] [4] for reviews.

Several aspects of the heightened impact of design-manufacturing links can be traced to a fundamental *crossover point* in the evolution of VLSI technology. This crossover point occurs when minimum feature dimensions and spacings decrease below the wavelength of the light source. Pattern fidelity deteriorates markedly in this *subwavelength lithography* regime, leading to the use of compensation mechanisms [15] that either perturb the shape (via *optical proximity correction* (OPC)) or the phase (via *phase-shifting masks* (PSM)) of transmitting apertures in the reticle. As can be seen in Figure 1, at least the next several process generations are likely to rely on subwavelength lithography.[1]

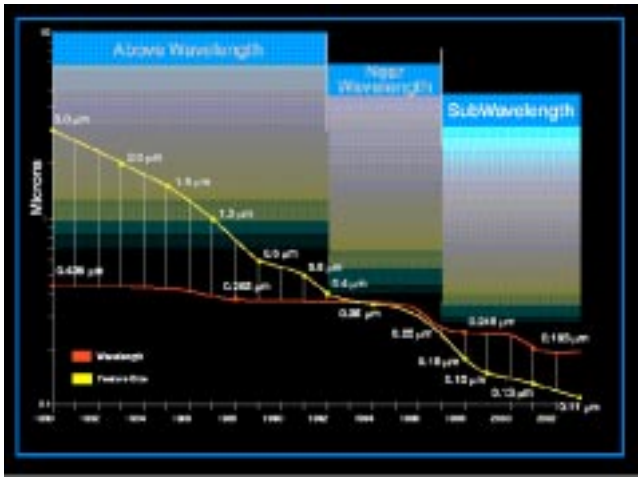

Figure 1: Shift to subwavelength optical lithography since the 0.35-micron process generation.

A key consequence of compensation mechanisms for subwavelength optical lithography is that the layout geometries being optimized in a polygon layout tool (e.g., place-and-route or custom layout) are no longer consistent with the actual mask geometries, and these in turn are no longer consistent with actual geometries on fabricated silicon. Figure

* Research at UCLA was supported by a contract and grant from Cadence Design Systems, Inc.

[1] A second crossover point in process evolution occurs when interconnect delays dominate device switching delays in deep-submicron CMOS technology [34]. Interconnect process optimization must achieve more delicate balances, e.g., affording simultaneous distribution of signal, clock and power with adequate performance and reliability while minimizing die area. Also, more interconnect layers are required at each successive node in the technology roadmap [34, 9, 11, 37], leading to a strong requirement for, e.g., *planarized* interconnect processes that rely on chemical-mechanical polishing (CMP). Manufacturing steps involving CMP have varying effects on device and interconnect features, depending on local characteristics of the layout. This link between layout and manufacturability has grown in importance with the move to very deep-submicron (especially shallow-trench isolation and inlaid-metal) processes [12] [35] [36] [2].

2 shows the SEM of a printed resist pattern for an 0.22-micron process superimposed on the IC layout design; the line end shortening and corner rounding, along with local context-dependent linewidth variations, are all fundamentally consequences of subwavelength lithography. With the disappearance of the "WYSIWYG" regime, new challenges for verification, and new constraints on layout design, must be recognized and addressed.

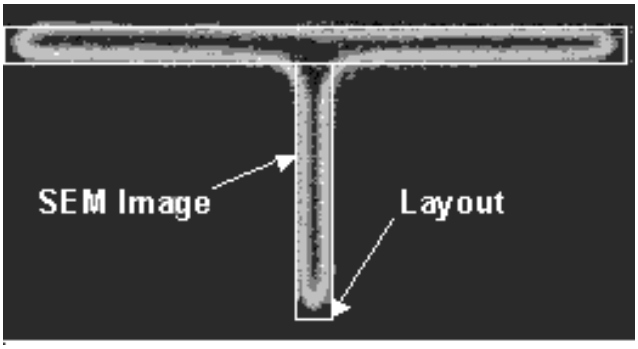

Figure 2: SEM image and superimposed layout design (solid line) for an 0.22-micron process, showing pronounced line end shortening and corner rounding.

In this paper, we assess the prospects for new tools and flows in the interface between layout design and manufacturability, focusing on layout design and verification for OPC and PSM. We will highlight necessary changes in the design-to-manufacturing flow, including infrastructure development in the mask and process communities, and opportunities for research and development in physical layout and verification.

2 Optical Proximity Correction

Optical proximity correction perturbs the shapes of transmitting apertures in the mask to address optical lithography distortions. The technique dates back to the early 1970s; see [17, 32, 3, 5, 24] for reviews. The goal of OPC is to produce smaller features in an IC using a given equipment set, by enhancing lithographic resolution. OPC is based on systematic corrections that compensate for the nonlinear feature distortions arising from optical diffraction and resist process effects; typically, these corrections are made according to a predetermined rule set ("rule-based OPC") or else according to the results lithography simulations that are iterated within the correction algorithm ("model-based OPC"). The OPC corrections themselves can be of several forms, including (i) serifs and hammerheads to eliminate corner rounding and line-end shortening; (ii) notches to control linewidth in the face of iso-dense effects; and (iii) subresolution assist features ("outriggers", or "scattering bars" [3]) for narrow gate geometries.[2] Figure 3 conveys the flavor of a layout after OPC has been applied. We observe that determining the optimal type, location, size and (a)symmetry of the corrections is highly complex and context-dependent. Furthermore, after OPC the "number of features" is no longer correlated to the "number of connected shapes", and the complexity of the geometry description is greatly increased.

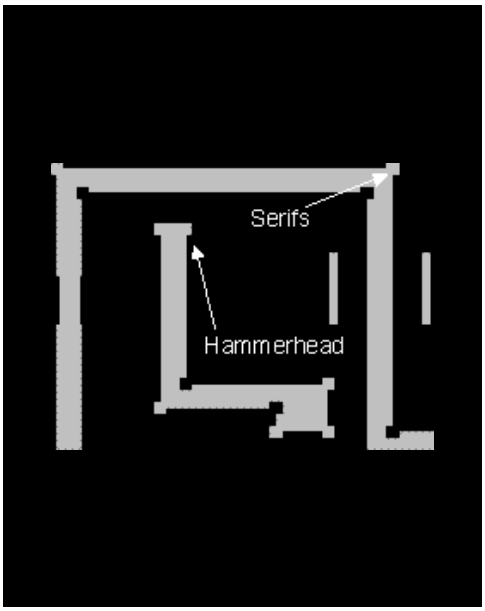

Figure 3: Aggressive OPC with subresolution gate assist features ("outriggers"), hammerheads, and serifs.

OPC is very much a fact of life in deep-submicron (subwavelength) lithography, both today and into the future. OPC is also somewhat more "mature" than filling and phase-assignment, in terms of available software solutions. At the same time, the ability of OPC to extend the life of optical lithography equipment is limited: the technique only compensates for distortions of features that can be printed, and if a feature does not print, it cannot be corrected (e.g., attempting to manufacture gates below 180nm using 248nm equipment typically results in features that do not print). An additional challenge to use of OPC below 180nm lies in actually making the mask, e.g., with current mask manufacturing equipment, tolerances are not sufficient to reliably create sub-180nm OPC masks. Due to these considerations, OPC-related developments (in contrast to PSM-related developments) are aimed at disconnects within an existing and comparatively well-understood infrastructure. In the remainder of this section, we highlight two disconnects in particular: (i) application of OPC in hierarchical and reuse-centric methodologies, (ii) application of OPC without regard to functional requirements implicit in a feature, and

[2] More formally, a *serif* is a small L-shaped geometry added to (subtracted from) a convex (concave) corner to compensate for rounding; a *hammerhead* is a U or inverted-U geometry that compensates for line-end shortening; a *notch* is a local thinning of a feature to compensate for linewidth variation; and an *outrigger* is a disconnected, non-printing geometry that uses diffraction effects to enhance linewidth control.

(iii) application of OPC without regard to verifiability (e.g., at the mask writing step).

2.1 OPC for Hierarchical and Reuse-Centric Methodologies

In hierarchical (e.g., cell-based) design methodologies, the layout context for any given instance is not known *a priori*. If OPC introduces corrections (e.g., subresolution assist features) that are outside the original cell layout, instances may not be freely composable and the key assumption of the hierarchical methodology becomes invalid. Furthermore, if the OPC applied to a given feature depends on characteristics of features in a local neighborhood that possibly extends outside the cell boundary, the notion of a single "master" that can be instantiated in arbibrary contexts again becomes invalid. Within a reuse-centric methodology, the key concern is that the layout design must be amenable to OPC insertion in a variety of target processes.

2.2 Integration of Functional Knowledge

A standard measure of the cost of optical proximity correction is *data volume*, i.e., the number of edges in the corrected layout (versus the number of edges in the original layout). Data volume impacts the transmission and manipulation of correct layout data, as well as the time to write a mask and the ease of verifying the mask. We note that the true purpose of OPC insertion is not to make the manufactured structure "look like" the on-screen geometry in the layout editor. Rather, the purpose of OPC is to preserve a *functional correspondence* between the designed circuit and the manufactured circuit. The complexity of the inserted OPC should be as small as possible, consistent with this purpose.

We identify three major avenues of tool development. (1) The first type of new tool that must be developed will integrate "silicon-level" modeling of the fabricated geometry, for purposes of *analysis and verification* of function. In other words, silicon-level layout parasitic extraction, layout-vs.-schematic verification, and design-rule correctness verification will be added into current design flows. An example output of such a tool is shown in Figure 4, where the layout designer may be presented with an image showing the differences (subtractions and additions) of fabricated versus laid-out geometries. (2) To compensate for the extra burden that such an added level of detail imposes, a second avenue of tool development will seek means of passing *functional intent* down to OPC insertion. The goal should be for OPC insertion to make only those proximity corrections that actually reduce the cost of the design – i.e., in the sense of reducing performance variation and the amount of guardbanding needed. (This is similar to "filtering" approaches for parasitic extraction in PV flows. For example, critical dimension (CD) control of an individual gate or individual wire jog may not be important if the gate or wire is not in any timing-critical path. On the other hand, CD control of devices and interconnects in timing-critical paths is extremely important.) Such methods for passing functional intent will be applicable in any design flow, including today's flows where OPC is a layout post-processing step that is performed in physical verification or in mask processing. (3) A third avenue for development is related to the question of how layout should best model the cost of the OPC insertion process. For example, it is not yet understood how a given geometric configuration affects the cost of the OPC needed to reliably yield a given functionality. Further study is also needed to understand how breaking hierarchy in the layout (or, in the OPC insertion) can affect data volume and verification costs at other stages of the design process.

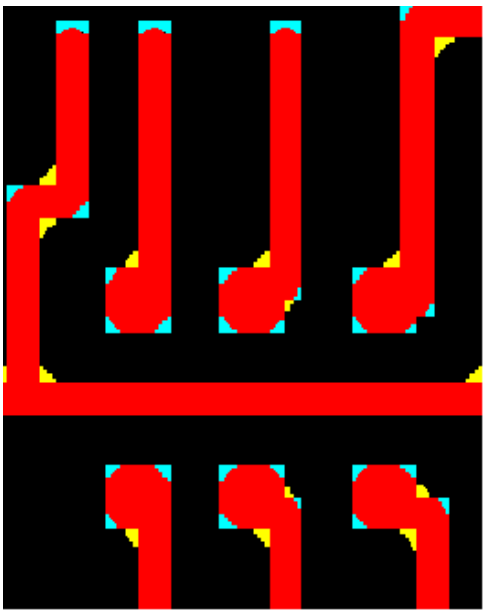

Figure 4: Output from "silicon-level" process modeling, showing the difference (subtractions, additions) between fabricated and laid-out geometries.

2.3 Integration of Mask Verifiability

With the long write times of complex masks, the cost of discarding a faulty mask (or, repairing the mask) can be substantial. Furthermore, highly contorted shapes on the mask can be difficult to inspect and verify (the inspection process itself is subject to optical distortions, increased runtime due to mask complexity, etc.). Hence, it is imperative that we investigate and understand the relationship between the type of OPC applied (e.g., serif, notch, subresolution scattering bar) and the verifiability and repairability of the mask. A modest first goal would be to develop new methods of abstracting the limitations of mask verification up to the OPC insertion stage: OPC insertion should not make corrections that cannot be manufactured or verified. Eventually, tools must abstract mask verification up to the layout design and performance optimization stages: performance-driven layout design should not create situations where very

aggressive, difficult-to-verify OPC is required to save the functionality of the circuit.

3 Phase-Shifting Masks

Phase-shifting mask (PSM) technology enables the clear regions of a mask to transmit light with prescribed phase shift. Consider two adjacent clear regions with small separation, and respective phase shifts of 0 and 180 degrees (see Figure 5). Light diffracted into the nominally dark region between the clear regions will interfere destructively; the improved image contrast leads to better resolution and depth of focus. All PSM variants employ this basic concept, which was proposed by Levenson et al. [16] in 1982. See [8] [31] [19] [33] [18] [21] for reviews of PSM technologies.

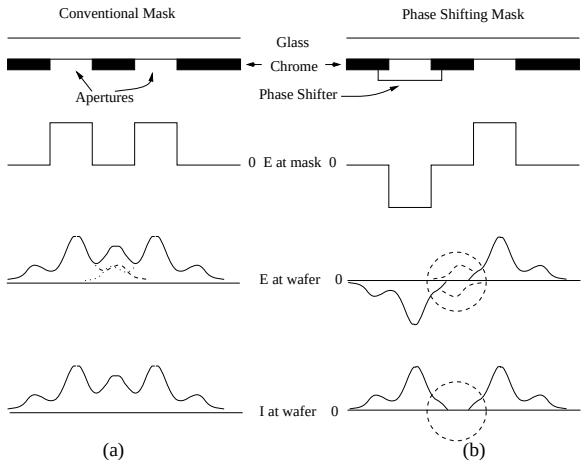

Figure 5: Comparison of diffraction optics of conventional and phase-shifting masks. E denotes electric field and I denotes intensity. With the conventional mask (a) light diffracted by two adjacent apertures constructively interferes, increasing the light intensity in the dark area of the wafer between the apertures. With the (alternating) phase-shifting mask (b), the phase shifter reverses the sign of the electric field, and destructive interference minimizes light intensity at the wafer in the dark area between apertures.

Two positive constants $b < B$ define a simplified relationship between printability and the distance between two clear regions [28]. The distance between any two features cannot be smaller than b without violating the minimum spacing design rule. If the distance between two features is at least b but smaller than B, the features are in *phase conflict*. Phase conflict can be resolved by assigning opposite phases to the conflicting features.

The Phase Assignment Problem: Assign phases to all features of a given layout such that no two conflicting features are assigned the same phase.

The Phase Assignment Problem may be stated in the context of the *conflict graph*, which is constructed by defining a vertex for each feature and introducing an edge between two vertices exactly when the corresponding features are in phase conflict. All phase conflicts are resolvable if and only if the vertices of G can be 2-colored with phase 0 and phase 180, which is possible if and only if G is bipartite (i.e., has no odd cycles). Hence, if G is not bipartite, the Phase Assignment Problem requires us to *delete* enough edges such that no odd cycles exist in the remaining modified conflict graph. Edge deletion in the conflict graph is achieved by changing the placement of layout features so that they no longer conflict (see Figure 6).

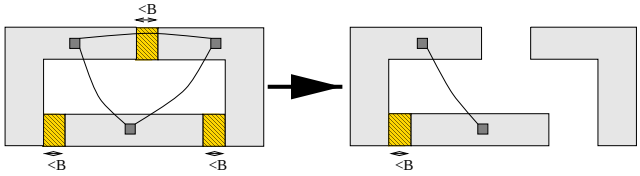

Figure 6: Edges of an odd cycle in the conflict graph (here, a triangle induced by conflicts among three features) can be removed by changing the placement of a feature.

It is important to note that the issue of phase conflict in PSM layout design may arise in very distinct contexts. Two classes of photolithographic masks are used to transfer circuit patterns onto silicon: bright field masks, and dark field masks. On a bright field mask the background (substrate) is transparent and the pattern is defined in chrome. Hence, the image projected onto silicon by a bright field mask defines circuit patterns through the formation of dark (unexposed) regions of the photoresist, a photosensitive material with which the silicon wafer is coated prior to exposure. Photoresists also come in two flavors: positive and negative. With positive photoresists, the development process following exposure removes photoresist material from all (exposed) regions that have been exposed with sufficient energy. For negative resists, the development process removes photoresist material from all unexposed areas. Today, positive photoresist is the primary vehicle for lithographic pattern transfer due to superior performance and a more advanced stage of development. The majority of critical circuit layers are imaged onto positive photoresist using bright field masks; this includes polysilicon, metal, and active layers. Dark field masks and positive photoresists are primarily used for contact and via layers.

Much of the early work on PSM design was in fact performed for dark field masks. Although this approach called for the use of negative photoresists, it was widely held that both layout design and mask manufacturing issues could be more readily solved in this case. Most commercial applications of phase shifting have on the other hand been based on bright field mask applications [7]. Although these methods have been applied in volume production, they continue to pose mask manufacturing problems that are yet unresolved. More recently, commercially viable applications of double-exposure phase shifting have used a combination of dark field phase shifting masks with positive photoresists which

has a number of significant manufacturing related benefits [19] [20] (Figures 7 and 8 show the effects of the double-exposure phase-shifting in the manufacture of an SRAM cell in 180nm process technology).

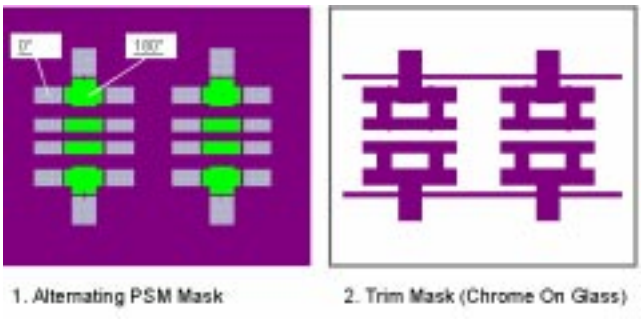

Figure 7: Double-exposure phase shifting mask design for SRAM cell in 180nm process technology.

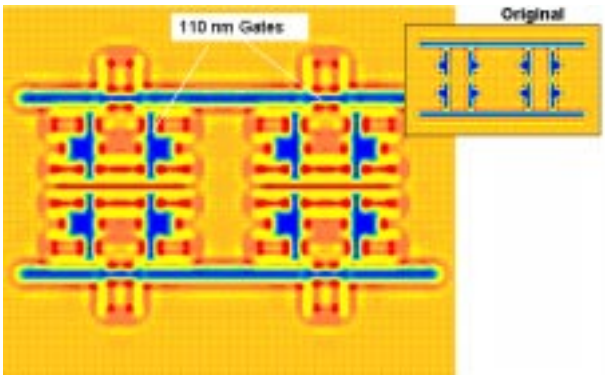

Figure 8: Effect of applying PSM technology to manufacture of SRAM cell in 180nm process technology.

From the perspective of designing phase-shifted layouts, bright field phase-shifting designs pose algorithmic problems that are substantially different from those encountered in dark-field phase shifting layout design. In both cases, the notion of phase conflicts calls for early resolution of such conflicts by introducing phase conflict verification throughout the physical design flow.

PSM Issues

The benefits of PSM include reduced gate lengths, as well as better CD (critical-dimension) control for gate lengths (see Figure 9). This results in higher-performance, lower-power circuits. Applied on the full-chip level, both performance and area gains can be realized since minimum feature spacings are reduced with appropriate phase assignments. On the other hand, the complexity of layout design and verification may increase substantially. In particular, since consistency of the phase assignment is a *global phenomenon* in the layout (as opposed to a local phenomenon such as a DRC tool might check), it is important to reconcile freedom in the (full-chip) layout design with algorithm complexity in the layout verification, or composability of instances in hierarchical design methodologies. Cost and complexity issues arise with respect to mask manufacturing and verification as well. In the remainder of this section, we will highlight two main issues: (i) approaches to layout modification for PSM, and (ii) PSM in hierarchical and reuse-centric methodologies.

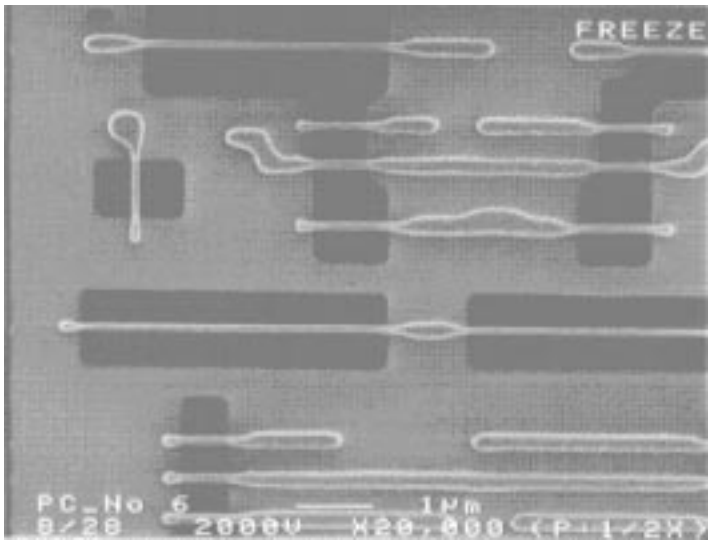

Figure 9: SEM micrograph (courtesy of Motorola) of poly gates fabricated with alternating PSM technology. Gate lengths are 90 nm.

3.1 Approaches to Layout Modification for PSM

Early methods for edge deletion in the conflict graph are due to [25, 28]. The heuristic of [26] (i) constructs the conflict graph G, (ii) creates a list of all odd cycles in G using an enumerative approach, and (iii) iteratively finds and deletes the edge that is in the greatest number of minimum-length odd cycles. Deletion is accomplished by increasing the lower bound on separation between the corresponding features, and then applying a compactor to perturb the shape or position of these features. This approach does not scale to large instances since the number of odd cycles can be exponential in the size of the layout. Moreover, it does not necessarily delete the minimum number of edges, nor will it necessarily select edges whose deletion will have minimum impact. The method of [29] (i) produces a symbolic layout from the mask layout; (ii) performs phase assignment in the symbolic layout; and (iii) compacts the symbolic layout using minimum spacing design rules consistent with the phase assignment. However, this method can significantly increase the layout area.

As discussed in [13], it is natural to seek phase-assignability using a layout modification step after detailed

routing. For example, the approaches of [29, 26] can be generalized as follows. First, initially constrain the layout only by the minimum-spacing design rule, i.e., no two features can be less than distance b apart. Then, *iteratively* apply the following three steps until the conflict graph G becomes bipartite: (i) compact the layout and find the conflict graph G; (ii) find the minimum-cost set of edges whose deletion makes the conflict graph G 2-colorable; and (iii) add a new compaction constraint for each edge in this minimum set, such that the pair of features connected by this edge must be separated by distance at least B. This approach not only requires integration of device-level compaction capability, but also requires an optimal algorithm to make the conflict graph bipartite. That is, given a planar graph $G = (V, E)$ with weighted edges, we seek the minimum-weight edge set M such that the graph $(V, E - M)$ contains no odd cycles. An exact algorithm for this problem can be traced to Hadlock [10] and Orlova et al. [30];[3] a faster algorithm was presented in [13]. We observe that the weight of an edge in the conflict graph should reflect the ease of perturbing the layout to break that particular conflict. For example, integration with a compactor allows us to use slack to determine edge weight.

A second layout modification approach is to use "splitting" of sufficiently long features into several parts. This is equivalent to splitting one vertex into several vertices in the conflict graph, and allows assignment of different phases to neighboring parts within the same feature. Introducing *partial shifters* (used for bright field PSM with positive photoresists [27]) between these parts allows gradual transitions between 0-phase and 180-phase with no dark edge being formed. The splitting technique requires a more complicated mask, but has two advantages: (i) it can only decrease the number of odd cycles, and (ii) it does not perturb the layout geometry.

Finally, it is possible to exploit *layer reassignment* to remove phase conflicts. This degree of freedom is natural for a routing tool, but unnatural for current mask optimization tools that view a given layer's geometries as immutable. With layer assignment, a problematic *wire* feature can be replaced by two vias and transferred to another layer (the approach does not apply to device layers). Such an approach will require the integration of device-level routing capability in a tight loop with the bicolorability analysis.

[3] To eliminate all odd cycles it is sufficient to eliminate odd faces of the planar graph G. Consider a graph D that is the geometric dual of G: all faces of G are vertices of D (note that there is a vertex of D that corresponds to the "outer face" of G), and each edge of D intersects with exactly one edge of G. The odd faces of G correspond to odd-degree vertices of D. Any edge elimination in G corresponds to edge contraction in D; in particular, we may remove a pair of odd faces from G by contracting edges of a (minimum-weight) path between the corresponding odd-degree vertices in D. Hence, the minimum-weight set of edges to break in the conflict graph corresponds to a minimum-weight matching of odd-degree vertices in D, which can be found in polynomial time.

3.2 PSM in Hierarchical and Reuse-Centric Methodologies

We have noted earlier that in hierarchical (e.g., cell-based) methodologies, the layout context for any given instance is not known *a priori*. With PSM layouts, this is a particularly difficult issue since a phase assignment solution for one cell instance may be incompatible with that of an abutted cell instance. An interesting research and development goal consists of methods to verify the composability of PSM layouts in a hierarchical methodology, as well as methods for hierarchical combination of alternative phase-shifting solutions (e.g., for standard-cell placement). With reuse-centric methodologies, it will be necessary to design layouts that can be phase-assigned to meet performance and area footprint constraints across multiple technologies and migrations. To this end, appropriate design rules (e.g., no T configurations, no uneven-length transistor fingers) would be beneficial. Finally, if bright-field and dark-field technologies should become simultaneous options for fabrication, then exploiting the near-duality of the respective design problems (see Figure 10) would be of interest.[4] It is possible that, despite the obvious differences between the two types of technology, there are ways in which design and verification of alternating PSM may addressed independent of the bright or dark field perspective.

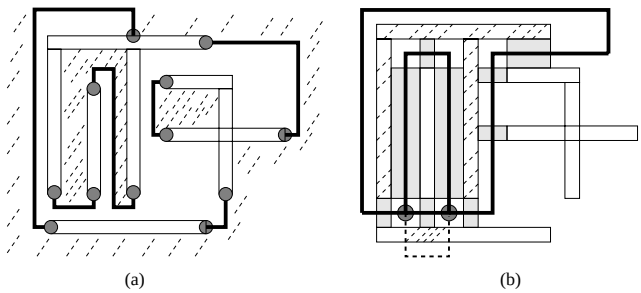

Figure 10: (a) Bright-field alternating PSM for a layout consisting of four features (eight rectangles). Crosshatched areas are 0 phase; other areas are 180 phase (features are defined by edges between 0- and 180-phase regions). Dark lines indicate phase edges (spurious features) that must be exposed away with a trim mask. (b) Dark-field alternating PSM. "Routes" between 0- and 180-phase regions (features) must cover all separations that are less than B, i.e., phase conflicts. The solution for the feature at the bottom of the figure uses the partial-shifter ("vertex splitting") approach to resolve the odd cycle in the conflict graph without changing feature placement.

[4] As noted above, several potentially viable double-exposure solutions for bright-field alternating PSM have been proposed [38, 6, 19]: (i) *phase edges* between 0- and 180-phase regions define thin features; (ii) a second *trim mask* exposure is used to erase unwanted phase edges (i.e., spurious features); and (iii) the key problem in layout design becomes one of "routing" the phase edges so that the trim mask is as simple and as tolerant to registration errors as possible. Figure 10 portrays the interesting *near-duality* of the dark field and bright field regimes.

4 Flow Changes and Futures

Figure 11 depicts the "traditional" design and manufacturing flow, as captured by attendees of the 1996 SEMATECH Litho-Design Workshop [33]. At the design-manufacturing interface, tools for design synthesis, analysis and verification must work together to enable the tremendous growth in "silicon complexity", design complexity and system complexity that is implied by the prevailing industry roadmaps. Tools and methodologies will therefore rely on the following precepts in order to achieve rapid design convergence.

- Upstream tools must pass their constraints and assumptions to downstream tools, and downstream tools must pass failure diagnoses back to upstream tools. (More generally, tools must exploit all available knowledge and all available context, whenever possible.)
- Macromodels for analysis and verification must be abstracted for use as synthesis objectives. (This enables a *prevention-centric* mindset, which is an essential companion to the "checking-centric" mindset that has dominated deep-submicron design practice.)

In the context of subwavelength optical lithography, the above precepts serve to highlight several unnatural aspects of today's separation between "ECAD" design syntheses and "TCAD" manufacturability verifications. With respect to OPC and PSM technologies, many optimizations for manufacturability are quite naturally handled as syntheses (where tools traditionally create the layout), rather than as verifications (where tools traditionally comment on, but are not empowered to change, their inputs). Thus, abstraction and understanding of manufacturing issues should be shifted up: (i) OPC- and PSM-related design rules will move up into global and detailed routing; (ii) PSM phase assignability checks and iterations with compaction will move into detailed routing; (iii) final PSM phase assignment will move up before traditional performance and physical verification; (iv) full-chip OPC insertion, full-chip aerial intensity mapping, "silicon-level" DRC/LVS/PA, and eventually function-centric DRC/LVS/PA will be added into the design flow; etc. At the same time, improved forward annotation of functional intent will ease the burden on verification tools for both layout geometry and mask geometry. Creating these new unifications and flow changes is an important challenge for industry as well as the research and development community.

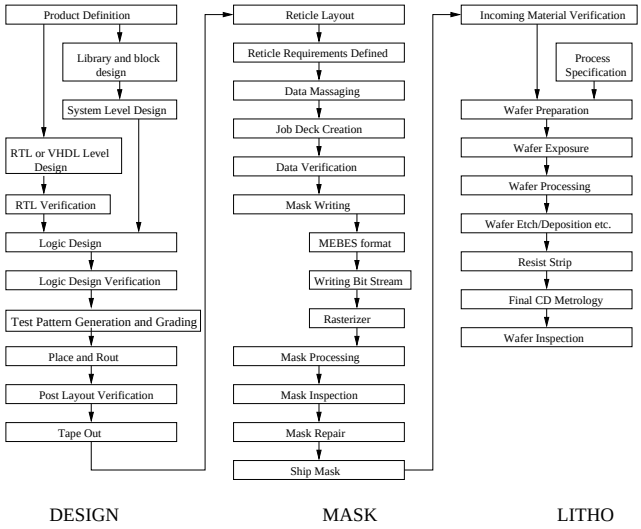

Figure 11: Process flow for IC design, mask processing, and lithography, as identified by participants in the 1995 SEMATECH Litho/Design Workshops [33].

References

[1] L. E. Camilletti, *Implementation of CMP-based Design Rules and Patterning Practices*, in 1995 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 1995, pp. 2–4.

[2] A. Chatterjee, I. Ali, K. Joyner, D. Mercer, et al., *Integration of Unit Processes in a Shallow Trench Isolation Module for a 0.25 μm Complementary Metal-Oxide Semiconductor Technology*, Journal of Vacuum Science and Technology B, 15 (1997), pp. 1936–1942.

[3] J. F. Chen, T. Laidig, K. E. Wampler, and R. Caldwell, *Practical Method for Full-Chip Optical Proximity Correction*, in SPIE, vol. 3051, 1997, pp. 790–803.

[4] V. K. R. Chiluvuri and I. Koren, *Layout-Synthesis Techniques for Yield Enhancement*, IEEE Trans. Semiconductor Manufacturing, 8 (1995), pp. 178–187.

[5] D. Dolainsky and W. Maurer, *Application of a Simple Resist Model to Fast Optical Proximity Correction*, in SPIE, vol. 3051, 1997, pp. 774–780.

[6] G. Galan, F. Lalanne, M. Tissier, and M. Belleville, *Alternating phase shift generation for complex circuit designs*, in SPIE 16th Annual BACUS Symposium on Photomask Technology, vol. SPIE 2884, 1996, pp. 508–519.

[7] P. Gilbert et al., *A High Performance 1.5V, 0.10um Gate Length CMOS Technology with Scaled Copper Metalization*, IEDM 1998, pp. 1013-1016.

[8] W. B. Glendinning and J. N. Helbert, *Handbook of VLSI Microlithography: Principles, Technology, and Applications*, Noyes Publications, 1991.

[9] L. Gwennap, *IC Vendors Prepare for 0.25-Micron Leap*, Microprocessor Report, September 16 (1996), pp. 11–15.

[10] F. O. Hadlock, *Finding a Maximum Cut of a Planar Graph in Polynomial Time*, SIAM J. Computing, 4 (1975), pp. 221–225.

[11] A. B. Kahng, S. Muddu, E. Sarto, and R. Sharma, *Interconnect Tuning Strategies for High-Performance ICs*, in Proc. Conference on Design Automation and Test in Europe, February 1998.

[12] A. B. Kahng, G. Robins, A. Singh, H. Wang, and A. Zelikovsky, *Filling and Slotting : Analysis and Algorithms*, in Proc. International Symposium on Physical Design, 1998, pp. 95–102.

[13] A. B. Kahng, H. Wang, and A. Zelikovsky, *Automated Layout and Phase Assignment Techniques for Dark Field Alternating PSM*, in Proc. SPIE 18th Annual BACUS Symposium on Photomask Technology, 1998.

[14] H. Landis, P. Burke, W. Cote, W. Hill, C. Hoffman, C. Kaanta, C. Koburger, W. Lange, M. Leach, and S. Luce, *Integration of Chemical-Mechanical Polishing into CMOS Integrated Circuit Manufacturing*, Thin Solid Films, 220 (1992), pp. 1–7.

[15] M. D. Levenson, *Wavefront engineering from 500 nm to 100 nm CD*, in Proceedings of the SPIE - The International Society for Optical Engineering, vol. 3049, 1997, pp. 2–13.

[16] M. D. Levenson, N. S. Viswanathan, and R. A. Simpson, *Improving Resolution in Photolithography with a Phase-Shifting Mask*, IEEE Trans. on Electron Devices, ED-29 (1982), pp. 1828–1836.

[17] L. Liebmann, A. Molless, R. Ferguson, A. Wong, and S. Mansfield, *Understanding Across Chip Line Width Variation: The First Step Toward Optical Proximity Correction*, in SPIE, vol. 3051, 1997, pp. 124–136.

[18] L. W. Liebmann, T. H. Newman, R. A. Ferguson, R. M. Martino, A. F. Molless, M. O. Neisser, and J. T. Weed, *A Comprehensive Evaluation of Major Phase Shift Mask Technologies for Isolated Gate Structures in Logic Designs*, in SPIE, vol. 2197, 1994, pp. 612–623.

[19] H.-Y. Liu, L. Karklin, Y.-T. Wang, and Y. C. Pati, *The Application of Alternating Phase-Shifting Masks to 140 nm Gate Patterning (II): Mask Design and Manufacturing Tolerances*, in SPIE Optical Microlithography XI, vol. 3334, Feb. 1998, pp. 1-14.

[20] H.-Y. Liu, L. Karklin, Y.-T. Wang, and Y. C. Pati, *The Application of Alternating Phase-Shifting Masks to 140 nm Gate Patterning: Line Width Control Improvements and Design Optimization*, in SPIE 17th Annual BACUS Symposium on Photomask Technology, vol. SPIE 3236, 1998, pp. 328–337.

[21] Y. Liu, A. Zakhor, and M. A. Zuniga, *Computer-Aided Phase Shift Mask Design with Reduced Complexity*, IEEE Transactions on Semiconductor Manufacturing, 9 (1996), pp. 170–181.

[22] W. Maly, *Computer-aided design for VLSI circuit manufacturability*, Proceedings of IEEE, 78 (1990), pp. 356–392.

[23] W. Maly, *Moore's Law and Physical Design of ICs*, in Proc. International Symposium on Physical Design, Monterey, California, April 1998. special address.

[24] A. Misaka, A. Goda, K. Matsuoka, H. Umimoto, and S. Odanaka, *Optical Proximity Correction in DRAM Cell Using a New Statistical Methodology*, in SPIE, vol. 3051, 1997, pp. 763–773.

[25] A. Moniwa, T. Terasawa, N. Hasegawa, and S. Okazaki, *Algorithm for Phase-Shift Mask Design with Priority on Shifter Placement*, Jpn. J. Appl. Phys., 32 (1993), pp. 5874–5879.

[26] A. Moniwa, T. Terasawa, K. Nakajo, J. Sakemi, and S. Okazaki, *Heuristic Method for Phase-Conflict Minimization in Automatic Phase-Shift Mask Design*, Jpn. J. Appl. Phys., 34 (1995), pp. 6584–6589.

[27] J. Nistler, G. Hughes, A. Muray, and J. Wiley, *Issues Associated with the Commercialization of Phase Shift Masks*, in SPIE 11th Annual BACUS Symposium on Photomask Technology, vol. SPIE 1604, 1991, pp. 236–264.

[28] K. Ooi, S. Hara, and K. Koyama, *Computer Aided Design Software for Designing Phase-Shifting Masks*, Jpn. J. Appl. Phys., 32 (1993), pp. 5887–5891.

[29] K. Ooi, K. Koyama, and M. Kiryu, *Method of Designing Phase-Shifting Masks Utilizing a Compactor*, Jpn. J. Appl. Phys., 33 (1993), pp. 6774–6778.

[30] G. I. Orlova and Y. G. Dorfman, *Finding the Maximum Cut in a Graph*, Engr. Cybernetics, 10 (1972), pp. 502–506.

[31] P. Rai-Choudhury, *Handbook of Microlithography, Micromachining, and Microfabrication, vol. 1: Microlithography*, SPIE Optical Engineering Press, Bellingham, 1997.

[32] F. M. Schellenberg, H. Zhang, and J. Morrow, *Evaluation of OPC Efficacy*, in Proc. Intl. Symp. on Aerospace/Defense Sensing and Dual-Use Photonics, vol. 2726, 1996, pp. 680–688.

[33] SEMATECH, *Workshop Notes*, in 3rd SEMATECH Litho-Design Workshop, Skamania Lodge, February 1996.

[34] SIA, *The National Technology Roadmap for Semiconductors*, Semiconductor Industry Association, December 1997.

[35] B. E. Stine, D. S. Boning, J. E. Chung, and L. Camilletti, *The Physical and Electrical Effects of Metal-fill Patterning Practices for Oxide Chemical-Mechanical Polishing Processes*, IEEE Transactions on Electron Devices, 45 (1998), pp. 665–679.

[36] B. E. Stine, V. Mehrotra, D. S. Boning, J. E. Chung, and D. J. Ciplickas, *A Simulation Methodology for Assessing the Impact of Spatial/Pattern Dependent Interconnect Parameter Variation on Circuit Performance*, in IEDM Technical Digest, 1997, pp. 133–136.

[37] D. Sylvester and K. Keutzer, *Getting to the Bottom of Deep-Submicron*, in Proc. IEEE Intl. Conf. Computer-Aided Design (to appear), November 1998.

[38] T. Waas, H. Hartmann, and W. Henke, *Automatic Generation of Phase Shift Mask Layouts*, Microelectronic Engineering, 23 (1994), pp. 139–142.