# Improved Effective Capacitance Computations for Use in Logic and Layout Optimization

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# Motivations

- Logic and layout optimization must accurately model interconnect effects
  - accurate delay estimation in floorplanning and pre-layout stages
  - efficient post-layout delay estimation within incremental mapping, layout, in-place optimization loop
- Accurate estimation of gate delays, slew times depends on accurate effective capacitance model for interconnect load

# Contributions of This Work

- Novel iterationless effective capacitance computation
- Fast; suitable for performance-driven layout optimization loop
- Applicable to step and ramp input waveforms, complex gates
- Delay estimates within 10% of HSPICE

# Outline of Talk

- Review of previous gate load models
- Review of previous effective capacitance methods
- New iterationless effective capacitance model
- Experimental validation
- Conclusions

# Review of Gate Load Models

- Lumped C model
  - ignores interconnect resistance (shielding), pessimistic delay estimate
- Lumped RC model
  - total interconnect resistance shields total capacitance, optimistic delay estimate
- Higher-order Π model [O'Brien-Savarino89]
  - computed from first three moments of driving point admittance of gate load; captures resistance shielding
  - disadvantages: requires four dimensional delay/slew tables, linear (but non-trivial) computational expense

# Review of Gate Load Models (cont.)

- RC Π model (Kahng and Muddu ‘96)
  - approximate RC or RLC interconnect tree by open-ended line; distributed nature of interconnect still considered
  - reduce load to Π model by matching first three moments
  - Π model parameters depend only on lumped (total) values of interconnect tree
  - several advantages
    - fast computation time (avoids computing  moments)
    - no knowledge of detailed interconnect topology needed
    - delay/slew times accurately computed

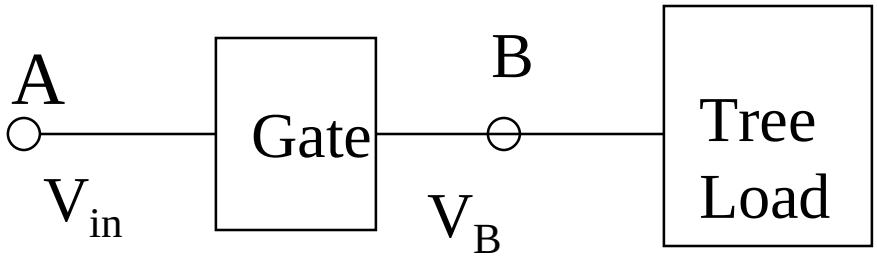
# Generic Effective Capacitance Model

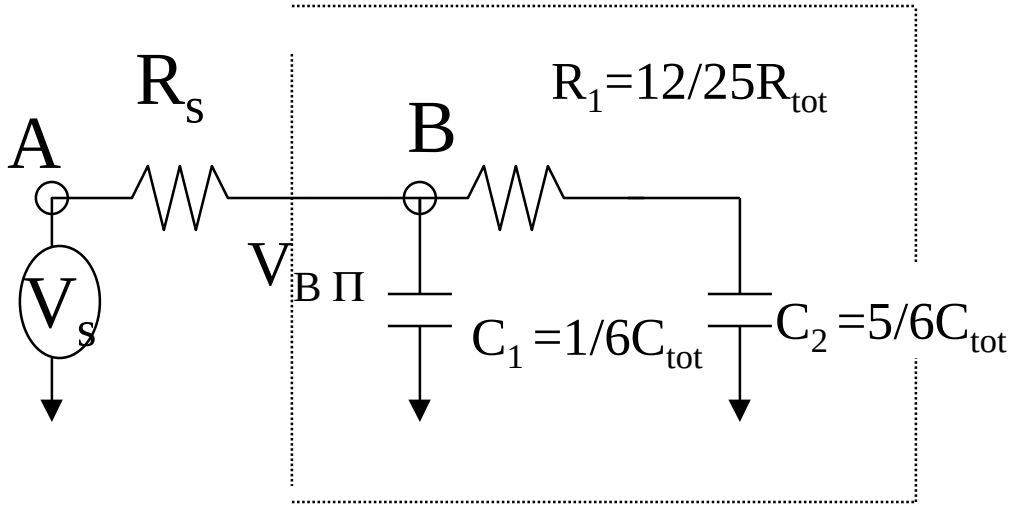
- Key concept:  reduce Π model to a single effective capacitance [QianPP94]
- Suited to 2-dimensional nonlinear table models for gate delay, output slew
- Output voltage approximated as two-piece waveform through iterative procedure
- Significant time for computation of both moments and two-piece waveform

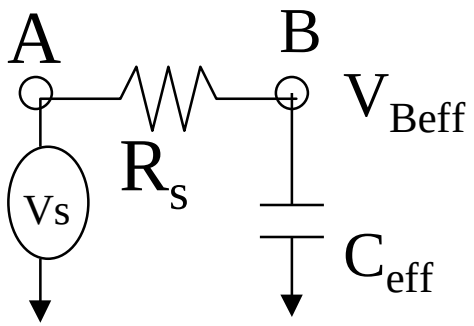
# Previous Effective Capacitance Approaches

- [McCormick ‘89]
  - $C_{eff}$ is function of total capacitance, gate output slew time and Elmore delay of gate load assuming step input
- [Pillage et al. ‘92,’94]
  - equate (i) current at gate output with Π model load and (ii) current at gate output with single effective load capacitor
  - start with initial $C_{eff}$ equal to total load capacitance, and compute gate delay/slew time
  - compute new $C_{eff}$ using empirical effective capacitance formula and threshold delay values
  - repeat this iteration until $C_{eff}$ converges
  - costly (5 to 10 iterations), requires interconnect topology

# Improved Effective Capacitance Approach: Equivalent Circuit Model



# New Effective Capacitance Computation

- Model gate with linear resistance $R_S$ and ramp input source $v_S$
- Model load with [KM96] RC Π model
- Compute response at gate output

$$v_B(t) = V_0/T_R \left[ t - R_d(C_1+C_2) + (1+s_1R_1C_2)/(b_2s_1^2(s_1-s_2))\, e^{s_1 t} - (1+s_2R_1C_2)/(b_2s_2^2(s_1-s_2))\, e^{s_2 t} \right] \text{ for } t \leq T_R$$

$$= V_0/T_R \left[ T_R + (1+s_1R_1C_2)(1-e^{-T_R s_1})/(b_2s_1^2(s_1-s_2))\, e^{s_1 t} - (1+s_2R_1C_2)\,)(1-e^{-T_R s_2})/(b_2s_2^2(s_1-s_2))\, e^{s_2 t} \right] \text{ for } t > T_R$$

# New Effective Capacitance Computation

- Equate (i) output slew with $\Pi$ load and (ii) output slew of simple capacitive load under ramp input
- If $T_{out}^{\Pi}$ is the gate output slew time, then the single effective capacitance has form $C_{ramp} = T_{out}^{\Pi} / k_2 R_d$
- Gate resistance $R_d$ is $R_d = r_{dn}/W_n$ or $R_d = r_{dp}/W_p$
  - $r_{dn}$ , $r_{dp}$ are resistances of 1um NMOS , PMOS devices
- $C_{eff}$ is between $C_{ramp}$ and $C_{tot}$
  - $C_{eff} = C_{ramp} + (C_{tot} - C_{ramp})/(1+ D_{LD}/D_{NL})$
  - $D_{LD}$ = gate delay with $C_{tot}$ as load
  - $D_{NL}$ = output slew time under no-load condition

# Summary of $C_{eff}$ Algorithm

- Compute $T_{out}^{\Pi}$ from gate output response with $\Pi$ model as load
- Compute $C_{ramp}$ by using $R_d$ and matching output slew $T_{out}^{\Pi}$ with that of a single load capacitance
- Use delay/slew tables to obtain gate delay $D_{LD}$ with $C_{tot}$ as load and slew time $D_{NL}$ with no-load
- Compute $C_{eff}$ in range between $C_{ramp}$ and $C_{tot}$ using empirical formula

# Complex Gates

- Computing accurate driver resistance is difficult for complex gate structures (channel-connected components)
  - non-zero voltage on intermediate nodes
  - variation in threshold voltage because of source-bulk voltage differences
- Complex gate drive strength proportional to K*W/L
  - K is body effect coefficient

# Effective Driver Resistance Modeling

- Model complex gates by computing effective driver strength, multiplying by body effect coefficient
  - $W_{neff} = K_{pd}/[L_1/W_1 + \ldots + L_n/W_n]$
  - $W_{peff} = K_{pu}/[L_1/W_1 + \ldots + L_n/W_n]$
  - $K_{pd}$ ($K_{pu}$) = pull-down (pull-up) body effect coefficient
- Effective driver resistance
  - $R_{deff} = r_{dn}/W_{neff}$ ($r_{dp}/W_{peff}$) for NMOS (PMOS)
- Use effective driver resistance $R_{deff}$ when computing response and slew time at gate output
  - same $C_{eff}$ equation as for simple gates

# Experimental Results

- 0.25um CMOS process
- Experimental configuration
  - two INV/NAND2 gates in series
  - interconnect load connected to second gate
- Use different RC topologies
- Slew time = 400ps to first gate
- Size of first INV is $W_p/W_n$ = 100/50um
- All dimensions are drawn dimensions; actual dimensions are 64% shrink of drawn

# Comparison of INV Delays

| INV size (Wp/Wn)um | HSPICE Delay (ps) | Estimated Delay (ps) | Total R/C (ohms/pf) |
|---|---|---|---|
| 24/12 | 130 | 110 | 260/0.5 |
| 100/50 | 80 | 90 | 260/0.5 |
| 100/50 | 115 | 125 | 710/1.4 |
| 80/40 | 130 | 120 | 150/0.4 |
| 80/40 | 140 | 160 | 300/0.8 |
| 200/100 | 55 | 65 | 1000/1.4 |

# Comparison of NAND2 Delays

| NAND2 size (Wp/Wn)um | HSPICE Delay (ps) | Estimated Delay (ps) | Total R/C (ohms/pf) |
|---|---|---|---|
| 100/100 | 94 | 103 | 260/0.5 |
| 100/100 | 129 | 142 | 710/1.4 |
| 80/80 | 147 | 159 | 150/0.4 |
| 200/200 | 63 | 70 | 1000/1.4 |

# Conclusions

- Novel iterationless approach for effective capacitance computation
- Applicable to both step and ramp input regimes
- Computationally more efficient than previous methods; usable within tight optimization loops
- Accurate delay estimates compared to HSPICE
  - within 15% for INV
  - within 10% for NAND2
- Better driver modeling reduces gate delay errors