IC Layout and Manufacturability: Critical Links and Design Flow Implications

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VLSI-99

Key Trends: ECAD View

- Silicon complexity and design complexity
  - many opportunities to leave major $$$ on the table
  - awareness of manufacturability, migratability
  - device-level layout opts even in cell-based methodologies
- Cost of verification
- Prevention is as important as checking
- Successive approximation = design convergence
  - upstream tools pass intentions, assumptions downstream
  - downstream tools must be predictable
  - analysis/verification macromodels == synthesis objectives

ECAD-to-TCAD Interface

- Physical design
  - RTL / floorplan / Boolean logic / mapping (gates) / block place-and-route
- Physical verification
  - RLC extraction / reduced-order models / gate-interconnect delay calculation / timing-noise-reliability-power analysis
  - DRC (geometry) / LVS (connectivity)
- Tape out GDSII
- Little or no awareness of reticle, lithography, deposition, etch, ...

TCAD Awareness of ECAD

Until 1994, there was no design or test component in the SIA Roadmap.

In 1997, Design and Test was one out of eleven component areas in the Roadmap.

ECAD Awareness of TCAD

- Where does design leave margin ($$$) on table?
  - cross-coupling delay uncertainty 300%
  - top vs. bottom NAND2 input switch 25%
  - temperature gradients 20%
  - Vdd change (IR drop, ground bounce) 18%
  - ACLV 10%
  - SOI history-dependence 8%
- Plus coupling noise, reliability, …
- Arguably, bigger and more tractable fish to fry

ECAD Awareness of TCAD

- Antennas, vias
  - solved problem (detailed routing)
- Critical area (defect-related yield loss)
  - solved problem (de-compaction)
- CMP
- OPC
- PSM
- Many interactions, but ECAD traditionally wants to know as little as possible

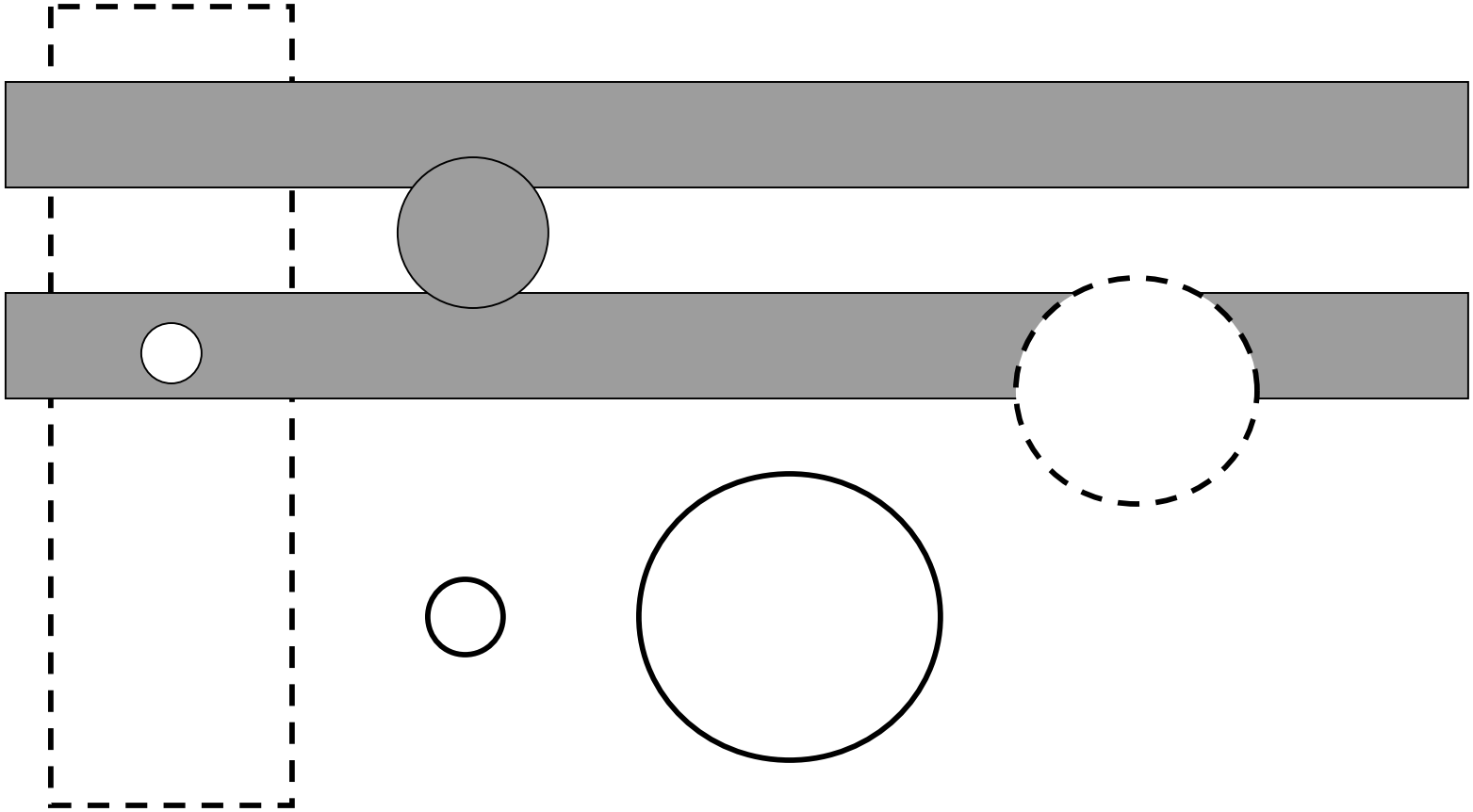
Antennas

- Charging in semiconductor processing
  - many process steps use plasmas, charged particles
  - charge collects on conducting poly, metal surfaces
  - capacitive coupling: large electrical fields over gate oxides cause damage or complete breakdown
  - induced V_t shifts affect device matching, e.g., in analog
- Standard solution: limit antenna ratio
  - antenna ratio = $(A_{poly} + A_{M1} + A_{M2} + ...) / A_{gate\text{-}ox}$
  - A_{mx} = metal x area electrically connected to node without using m(x+1), not connected to an active area
- Solved by routing or protection diodes

Defect-Related Yield Loss

- High susceptibility to spot defect-related yield loss, particularly in metallization stages of process
- Most common failure mechanisms: shorts or opens due to extra or missing material between metal tracks
- Design tools fail to realize that values in design manuals are **minimum** values, not **target** values
- Again, will see that proper solution is in layout

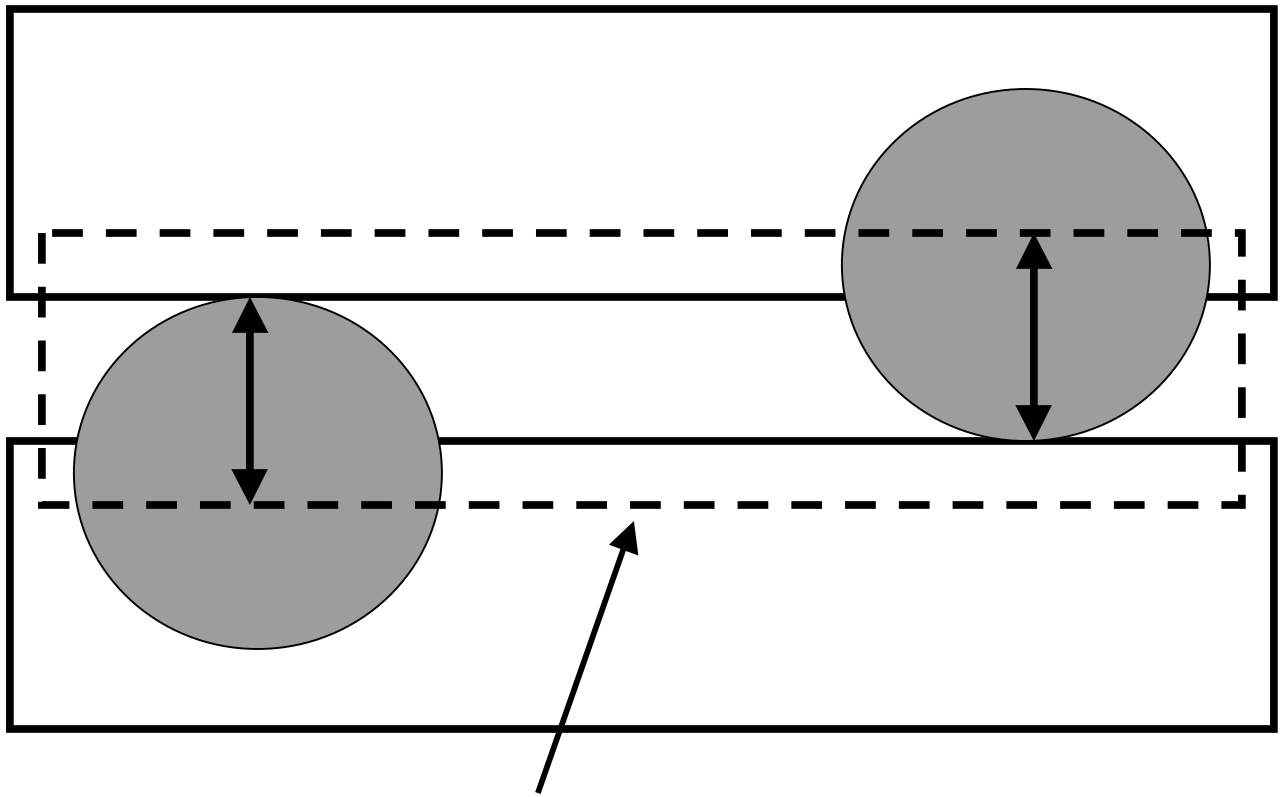
Fatal Defect Types



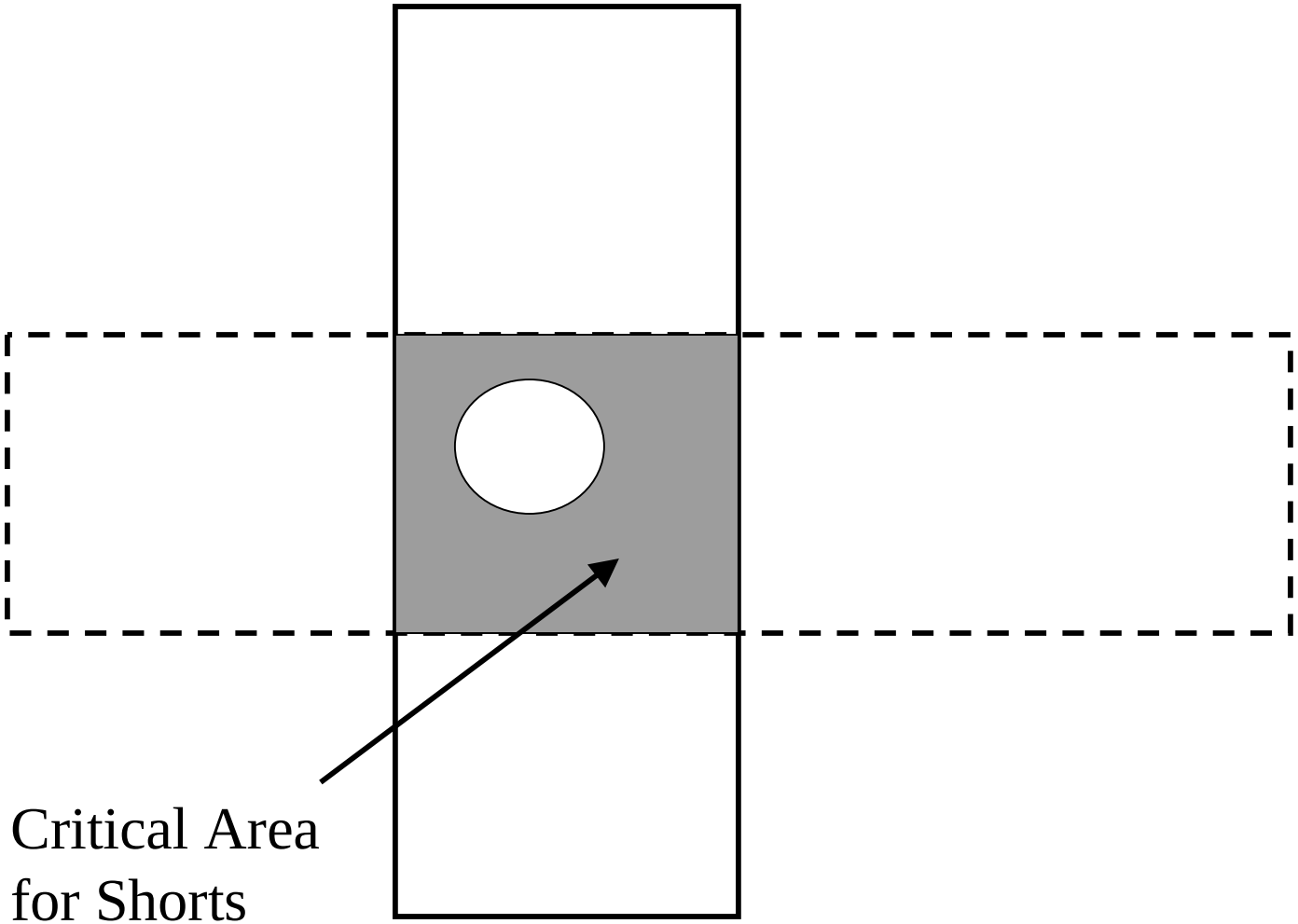
Two types of short circuits

One type of open circuit

Critical Area for Short Circuits



Critical Area for Short Circuits



Solutions to Spot Defect Yield Loss

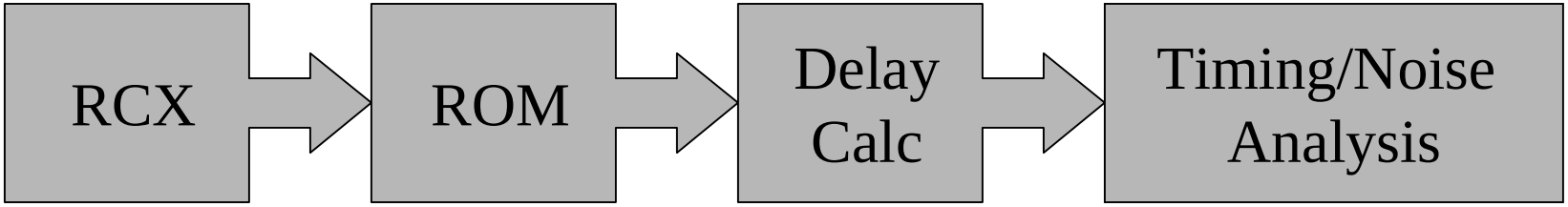
- Modify wire placements to minimize critical area
- Properly addressed in router
  - router understands critical-area analyses, optimizations
  - spread, push/shove (gridless, compaction technology)
  - layer reassignment, via shifting (standard capabilities)
  - related: via doubling when available, etc.
- Post-processing approaches in PV are awkward
  - breaks performance verification in layout (if layout has been changed by physical verification)
  - no easy loop back to physical design: convergence problems

CMP Variability

- Chemical-mechanical polishing (CMP)
  - applied to interlayer dielectrics (ILD), STI, inlaid metals
- CMP variability
  - pad deforms over metal feature
    - ILD thickness proportional to feature density (dishing, etc.)
  - huge part of chip variability budget
- Solution: density control
  - uniform density by insertion of dummy fill features
  - must be accounted for in physical design/verification

Need for Density Awareness in Layout

- Performance verification flow:



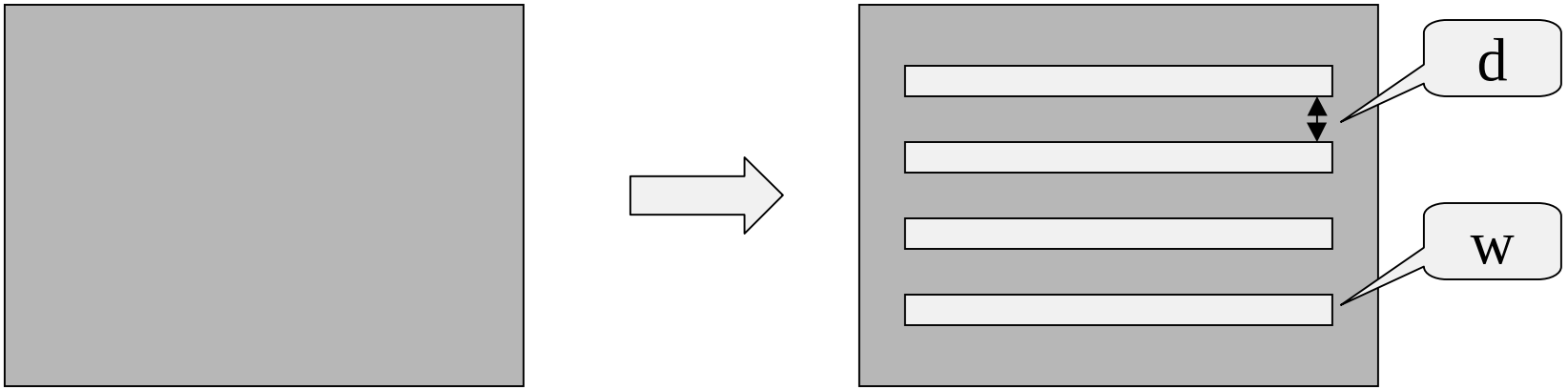
- Filling/slotting geometries affect RC extraction

VICTIM LAYER TOTAL CAPACITANCE (10^{-15} F)			
Same layer-i neighbors?	Fill layers i-1, i+1?	$\varepsilon = 3.9$	$\varepsilon = 2.7$
N	N	2.43 (1.0)	1.68 (1.0)
N	Y	3.73 (1.54)	2.58 (1.54)
Y	N	4.47 (1.84)	3.09 (1.84)
Y	Y	5.29 (2.18)	3.66 (2.18)

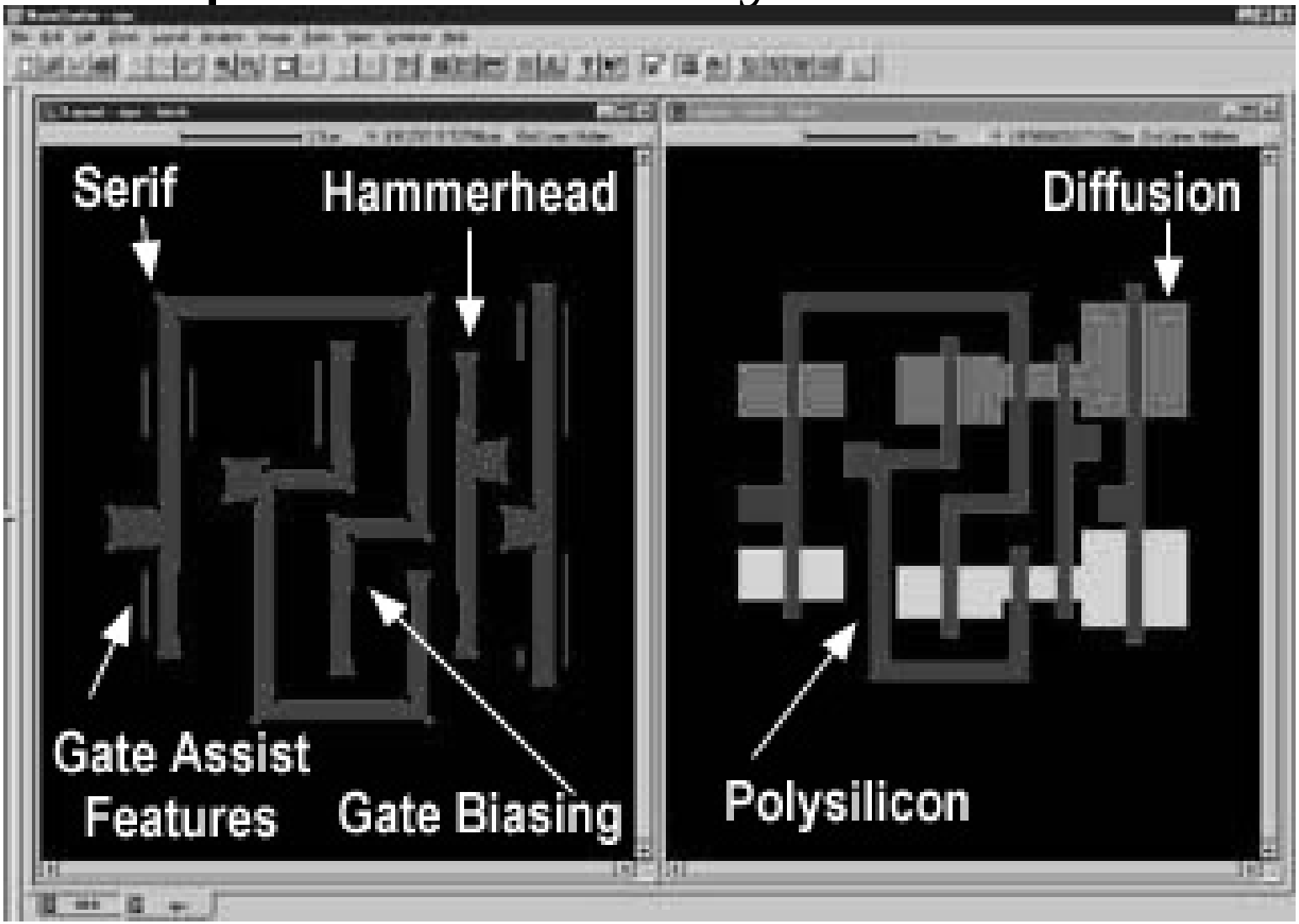
- Up to 54% error in extracted capacitance

Another Layout Modification: Slotting

- E.g., I/O, power buses: want to prevent lift-off or distortion during dicing
  - slot rectangle lengthwise, parallel to current flow
  - slots have prescribed width *w* and separation *d*
- Again, breaks performance verification flow



Optical Proximity Correction



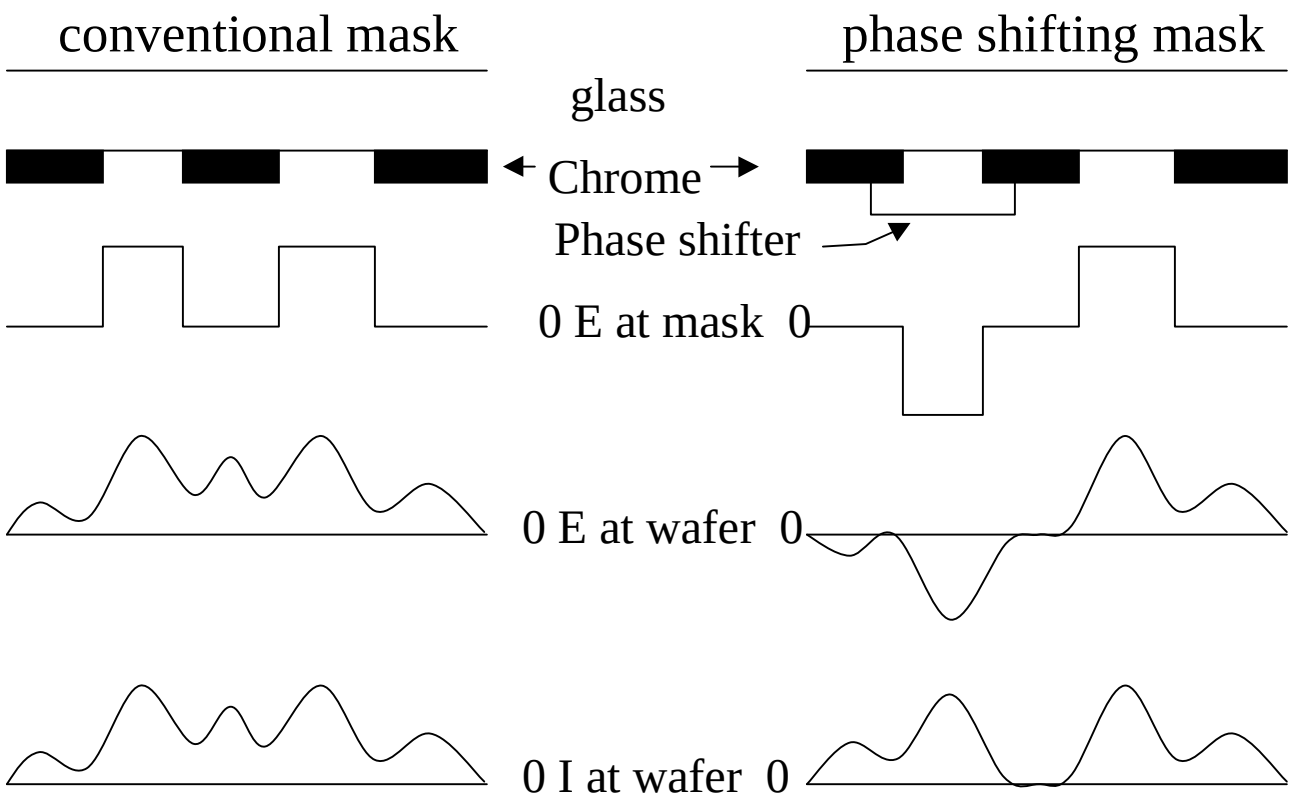
Proximity Effects in Lithography

- Contact shape distortion (isolated vs. arrayed)
- Line end shortening, iso-dense effects
- Small process windows (exposure, defocus)
- OPC mediates proximity effects by changing shapes of apertures in mask

OPC Issues

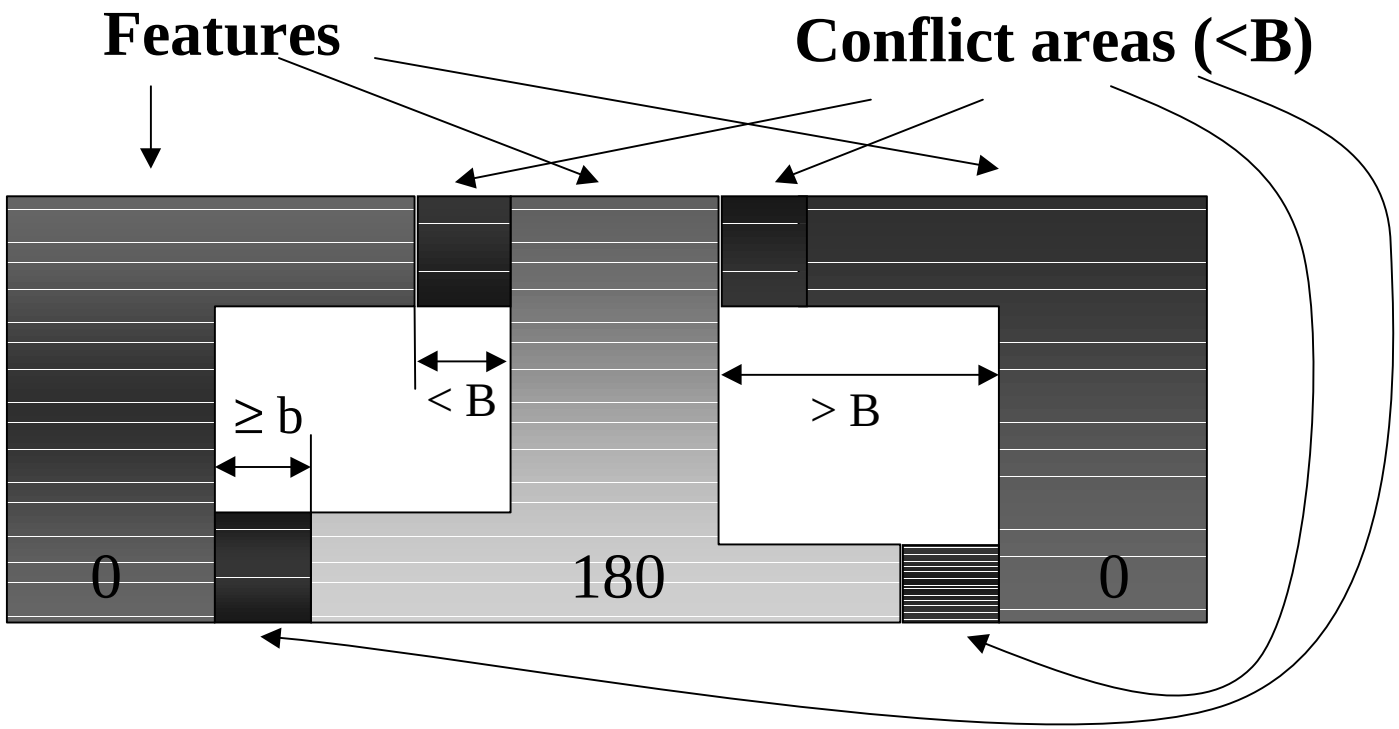
- Pass functional intent down to OPC insertion
  - make corrections that win $$$, reduce performance variation
  - OPC insertion is for predictable circuit performance, function
- Pass limits of mask verification up to layout
  - don’t make corrections that can’t be manufactured or verified
- Layout needs models of OPC insertion process
  - geometry effects on cost of required OPC to yield function
  - costs of breaking hierarchy (beyond known verification, characterization costs)

Alternating Phase-Shifting Masks



Phase Assignment Problem

Assign phases 0, 180 to all features such that pairs with separation < B have opposite phases



b ≡ minimum separation

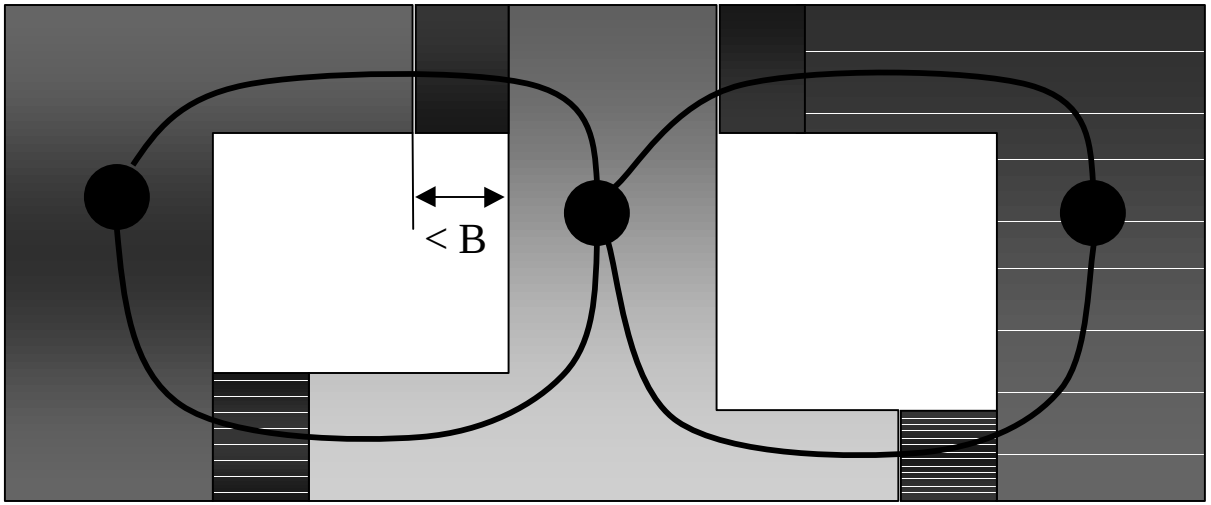
B ≡ minimum separation between same-phase features

Conflict Graph

Vertices: features

Edges: conflicts

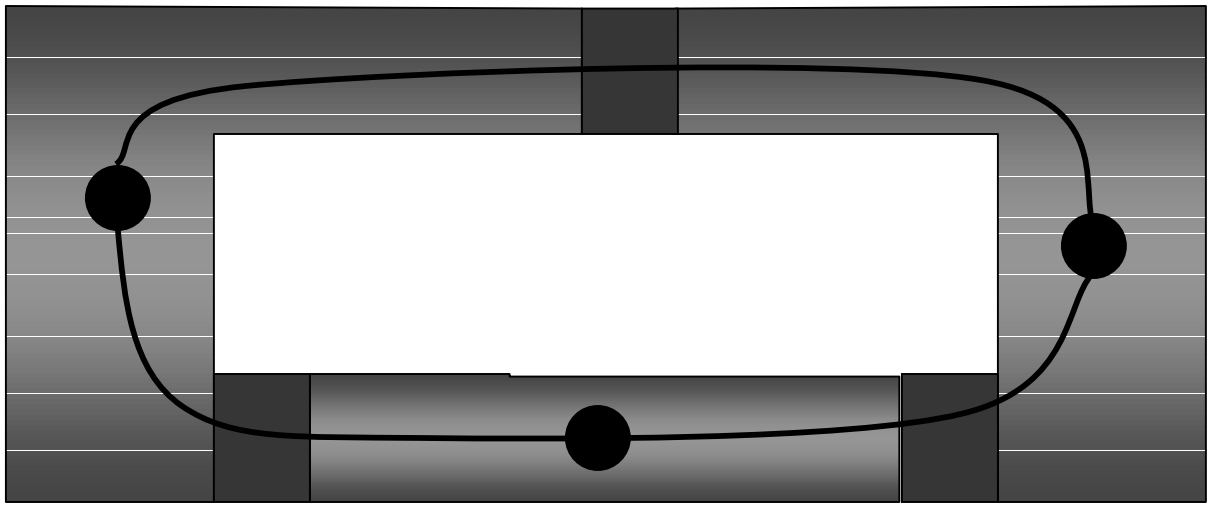
(feature pairs with separation < B)



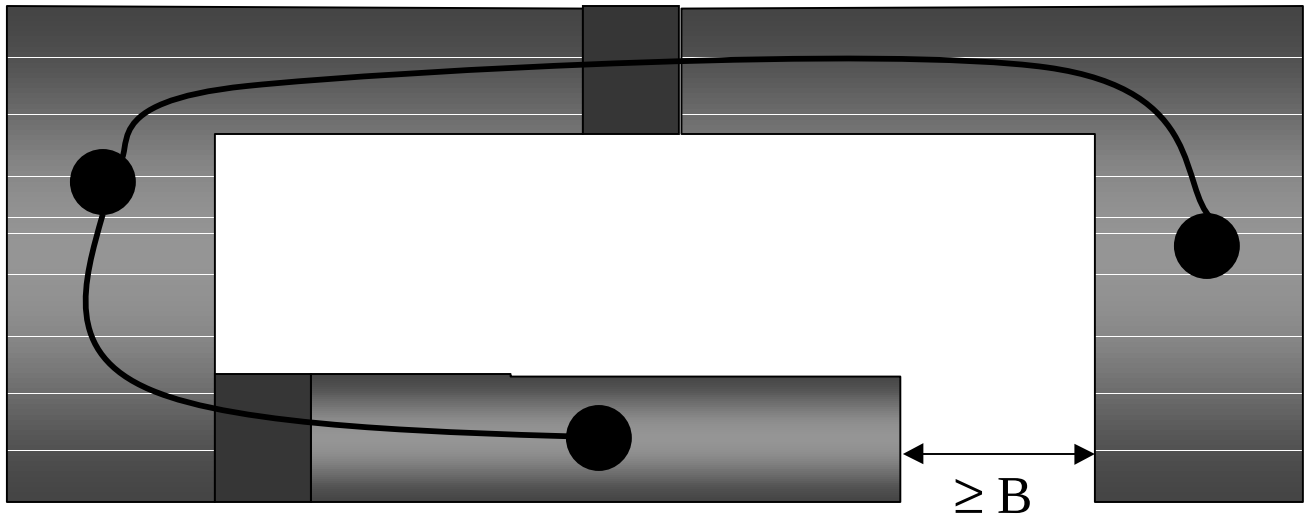
Odd Cycles in Conflict Graph

No **valid** phase assignment exists, because of odd cycle (triangle) in conflict graph

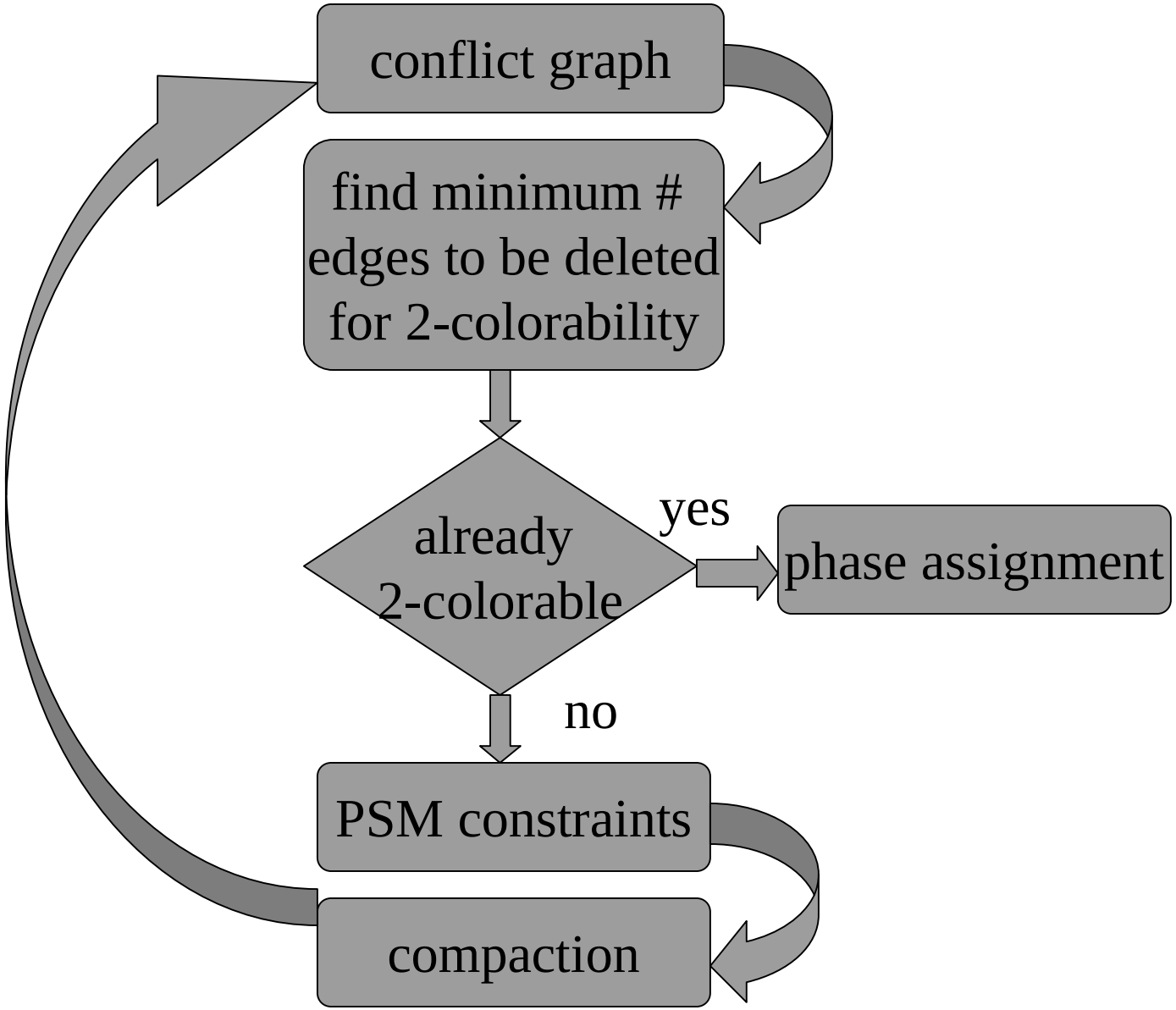
Valid assignment ≡ 2-colorable ≡ bipartite ≡ no odd cycles



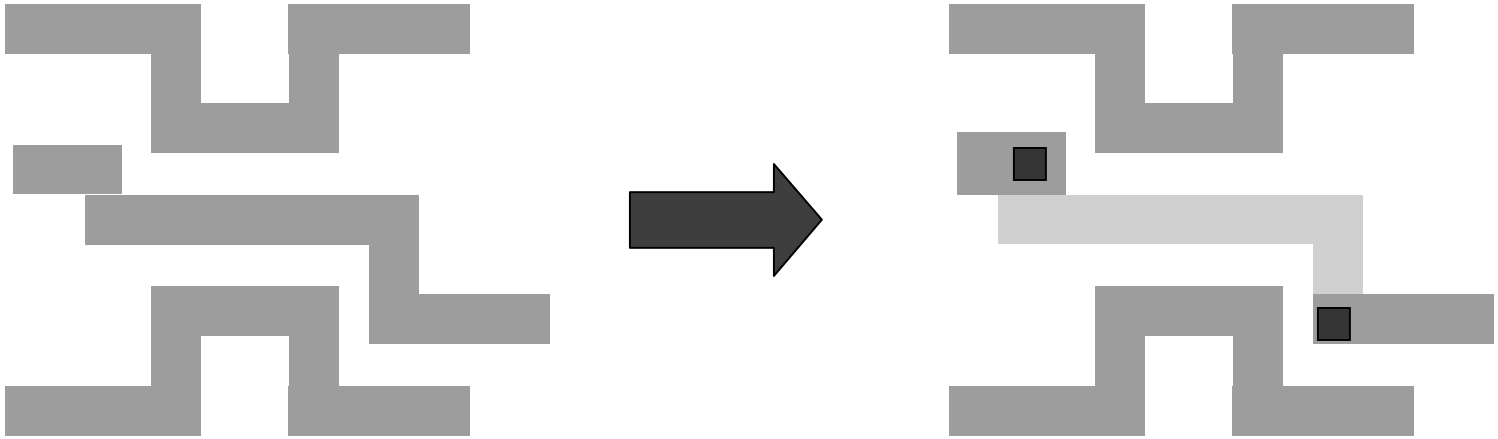
Breaking an Odd Cycle



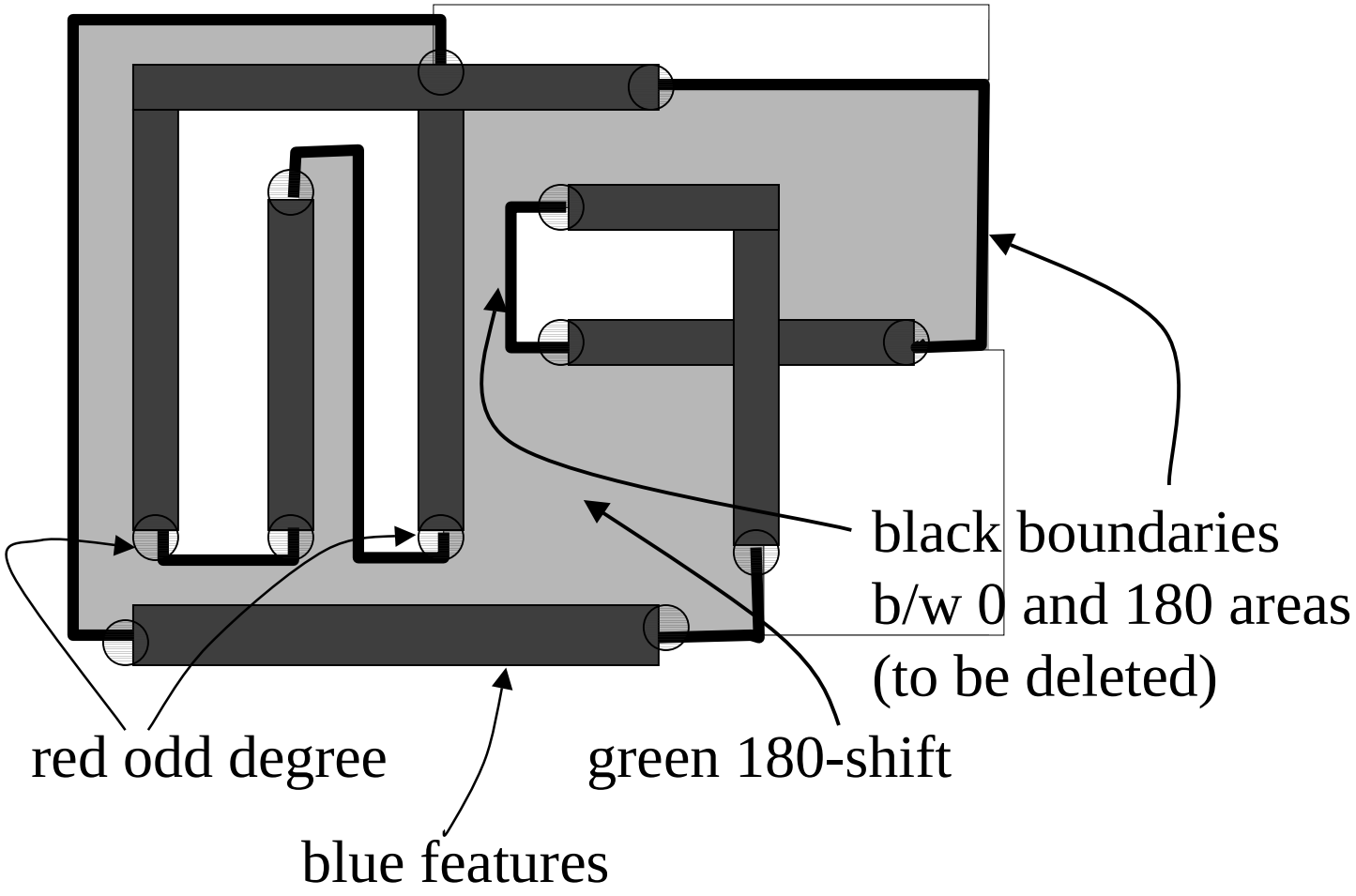
Iterative Phase Assignment and Compaction



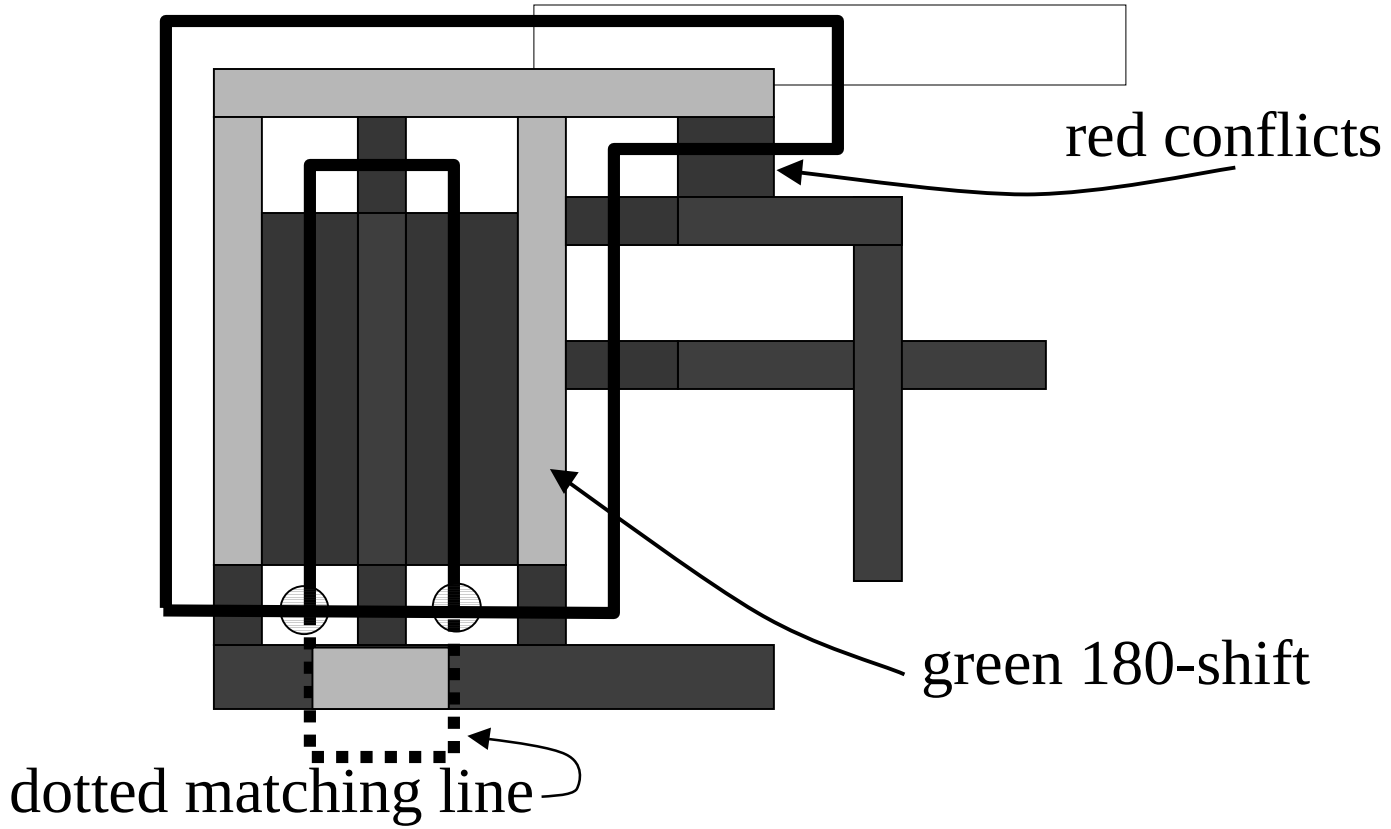
Layer Assignment



PSM for Bright Field



Similar PSM for Dark Field



any path matching odd nodes of dual graph should go through features - split into different phases

Layout for PSM: Many Solutions

- Iterative coloring and compaction
- One-shot phase assignment
- Conflict edge weight
- Splitting of features
- Layer assignment
- Routing-type approaches
- All of them belong in layout design

Gap Analysis

- Hierarchy, data volume, verification, ...
- Objectives and constraints for design
  - cost of reducing variability for each circuit/layout construct
- Requirements for mask, litho, verification
  - functional intentions and assumptions from design process
- ECAD-TCAD mutual understanding, information flows

Integrated Layout Flow

- Gate-level netlist, performance constraint budgeting, cell placement
- Post-placement density check; CMP-fill estimation based on estimated routes
- Post-placement density-aware performance analysis
  - issues: floating vs. grounded fill; encapsulating fill rules
- global and detailed routing, cell resynthesis on fly
  - delay, noise, reliability assumptions = constraints
  - OPC- and PSM-aware min-cost layout synthesis subject to constraints
  - fill abstractions in constraint-driven routing

Integrated Layout Flow

- Density analysis, CMP-fill estimation based on detailed routing
- Post-detailed routing performance analysis
- PSM phase assignability check for all layers
  - new compaction constraints as necessary
  - layout compaction or incremental detailed routing
  - until pass phase assignability, performance analysis
- Actual dummy fill insertion
  - issues: data volume
- Detailed physical verification (geom, conn, perf)

Integrated Layout Flow

- Full-chip OPC insertion
  - issues: min-cost OPC that achieves required function
  - issues: data volumes, metrics, intermediate formats
  - issues: tools stepping on each other (line extensions in DSM router rules are “zeroth-order OPC”, for example)
- Full-chip printability check
- Silicon-level DRC/LVS/performance analysis