# Interconnect Tuning Strategies for High-Performance ICs

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A. B. Kahng, S. Muddu, E. Sarto and R. Sharma

Silicon Graphics, Inc., Mountain View, CA 94039
UCLA Computer Science Dept., Los Angeles, CA 90095
{muddu,sarto,ashu}@mti.sgi.com, abk@cs.ucla.edu

# Interconnect Tuning

- *Design-specific* interconnect process optimization
  - per-layer default line dimensions and pitch
  - interlayer dielectrics (ILD) and interconnect materials
  - vertical interconnection schemes
- Many balances
  - local/global signaling vs. clock vs. power/ground
  - density vs. performance, signal integrity
  - density vs. manufacturability, reliability
  - must fit interconnect design/optimization methodology
- Examples: local/global, airbridges, M3/M6 power planes

# This Work

- Global wiring layers (e.g., M4 in a 5LM process)
- Focus on bus routing, repeater insertion, shielding/spacing
- Driving criteria: signal integrity, signal delay
- Four questions
  - Width/spacing for optimum performance w/fixed pitch?
  - Optimum interval for repeater insertion?
  - Should shielding be used?
  - Optimum repeater insertion strategies for buses?
- Experimental *methodology*, sample results

# Basic Testbed

- $0.25\mu m$ CMOS process with detailed dielectric profile
- Aluminum interconnect
- QuickCap for area, lateral capacitance extraction
- Switching factor ranging from 2.0 (nominal to each neighbor) to 4.0 (worst-case to each neighbor)
- HSPICE simulation for noise/delay analysis
- Not addressed: ILD, line thickness, materials (Cu, low-k)

# Optimum Width/Spacing for Given Pitch

- Study of "fast" M3 interconnect layout rule with 3.2$\mu m$ pitch
- Lengths of interest: 2500$\mu m$ to 4000$\mu m$
- Dense M2 crossunders treated as ground plane, M4 crossovers modeled explicitly
- Worst-case coupling (SF = 4.0)
- **Conclusion**: (width,spacing) = (1.2,2.0)$\mu m$ is best

# M3 Coupling Capacitances Extracted by QuickCap

| Width,Space ($\mu$m) | **Coupling Capacitance per $\mu$m (aF)** | | | |
|---|---|---|---|---|
| | Each Neighbor | Top Plane | Bottom Plane (ground) | Total |
| 1.0,2.2 | 25.20 | 54.79 | 46.84 | 152.66 |
| 1.2,2.0 | 29.00 | 56.74 | 48.22 | 163.53 |
| 1.4,1.8 | 33.33 | 57.76 | 51.53 | 177.32 |
| 1.6,1.6 | 38.71 | 59.09 | 51.90 | 188.41 |
| 1.8,1.4 | 44.75 | 60.22 | 51.52 | 200.92 |

# Delay Estimates for M3 Line Configurations

| Width,Space ($\mu$m) | **50% Threshold Rise Delay (ps)** | | | | | |
|---|---|---|---|---|---|---|
| | 4000 $\mu$m M3 length | | | 6000 $\mu$m M3 length | | |
| | Driver Load Delay | Int. Delay | Total Delay | Driver Load Delay | Int. Delay | Total Delay |
| 1.0,2.2 | 106.19 | 113.99 | 220.17 | 159.28 | 233.09 | 392.37 |
| 1.2,2.0 | 115.00 | 100.72 | 215.73 | 172.51 | 207.14 | 379.65 |
| 1.4,1.8 | 126.61 | 92.80 | 219.41 | 189.92 | 192.10 | 382.02 |
| 1.6,1.6 | 138.77 | 87.12 | 225.89 | 208.15 | 181.41 | 389.56 |
| 1.8,1.4 | 151.24 | 82.84 | 234.08 | 226.85 | 173.41 | 400.26 |

# Interval Between Repeaters

- **Goal**: equalize gate load delay and interconnect delay
- **Goal**: control slew times for signal integrity, reliability (E.g.: 400ps input slew $\rightarrow$ output rise/fall times $<$ 700ps)
- Experimental studies of delay, rise/fall times
  - "dense" (2.1$\mu m$ pitch), "fast" (3.0$\mu m$ pitch) rules
  - SF between 2.0 and 4.0
  - repeater interval between 5000$\mu m$, 10000$\mu m$
- **Conclusion**: slew time constraints determine the repeater interval for dense rule; nearly so for fast rule

# M3 Slew Times

| Width ($\mu$m) | Space ($\mu$m) | Length ($\mu$m) | SF | Delay (ps) | Rise Time (ps) | Fall Time (ps) |
|---|---|---|---|---|---|---|
| 1 | 1.1 | 9000 | 4 | 486 | 1421 | 1265 |
| 1 | 1.1 | 7000 | 4 | 310 | 975 | 847 |
| 1 | 1.1 | 5000 | 4 | 172 | **623** | **525** |
| 1.4 | 1.6 | 9000 | 4 | 303 | 963 | 832 |
| 1.4 | 1.6 | 7000 | 4 | 195 | **686** | **578** |
| 1.4 | 1.6 | 5000 | 4 | 111 | **465** | **384** |

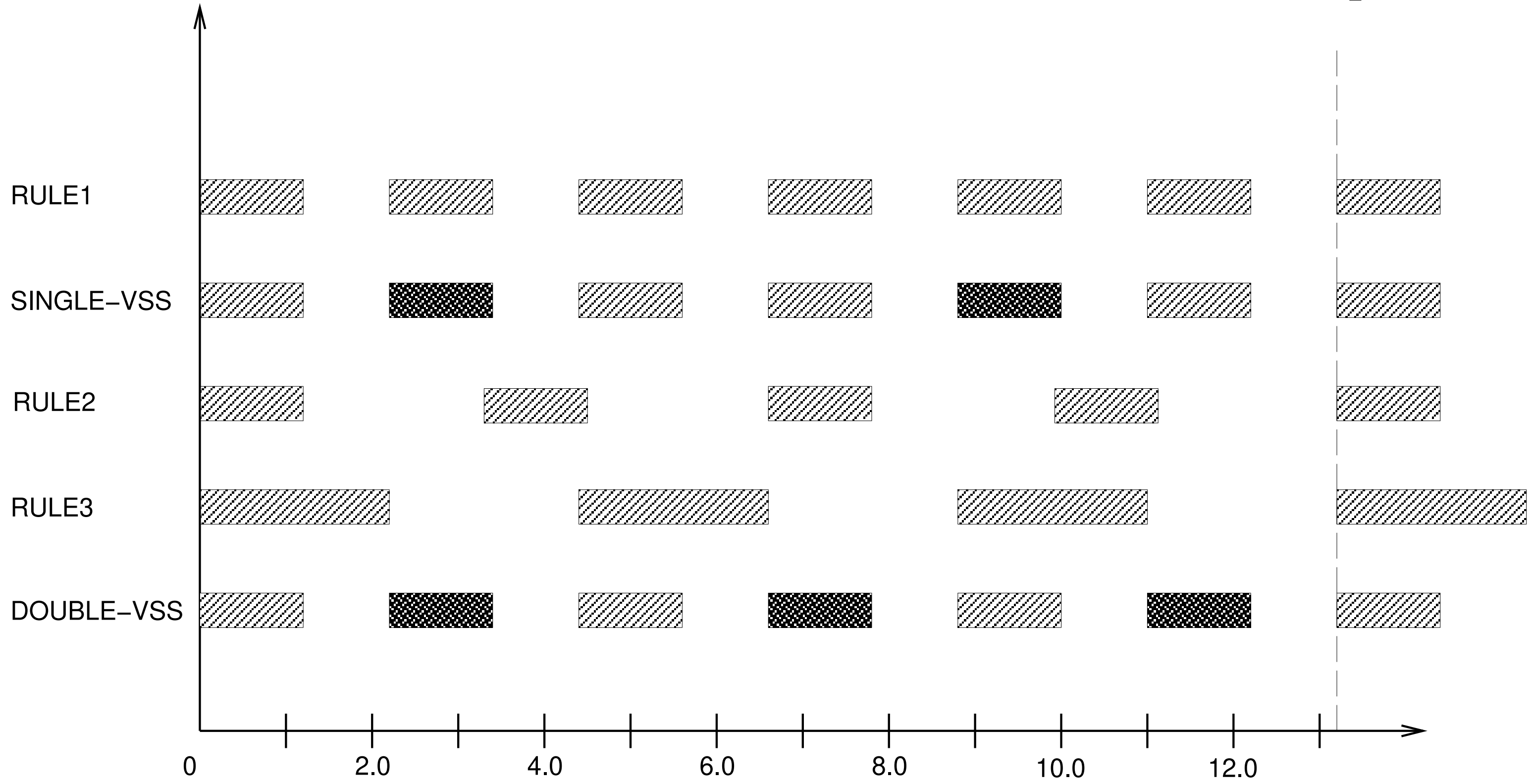
# Benefits of Shield Wiring

- **Five pitch-matched M3 layout rules**
  - **Rule 1** (“dense”, 1.2$\mu m$ width / 1.0$\mu m$ spacing)
  - **Single-**$V_{SS}$ (1.2/1.0 with every third line grounded)
  - **Rule 2** (“fast”, 1.2/2.1)
  - **Rule 3** (“super-fast”, 2.2/2.2)
  - **Double-**$V_{SS}$ (1.2/2.1 with every other line grounded)

- Slew times under 600ps $\rightarrow$ noise coupling not problematic

- **Conclusion**:
  - Rule 3 (“super-fast”) gives more than 37% delay reduction, is preferable to double-shields
  - Single-shields less effective than Rule 2 (“fast”)

# Five Pitch-Matched Width-Spacing Rules



# Delay Estimates For 4000$\mu m$ M3 Line

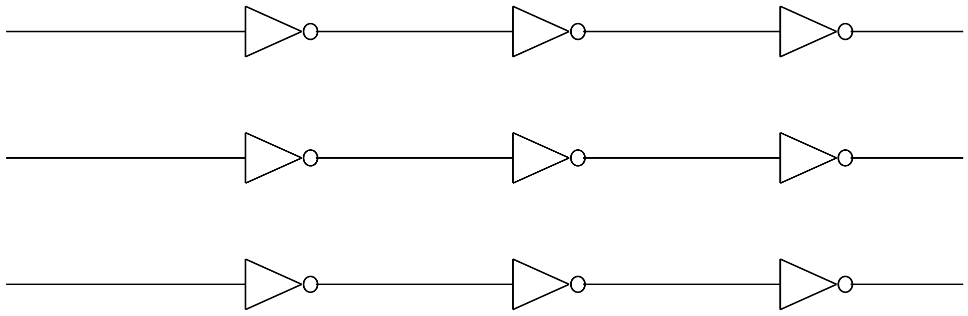
| M3 Rules | Width,Space ($\mu$m) | Neighbor Planes | 50% threshold rise delay (ps) | |
|---|---|---|---|---|
| | | | Load/Interconnect Delays | Total Delay |
| Rule1 | 1.2,1.0 | M2,M4 Line | 167.84/114.03 | 281.87 |
| Rule1 | 1.2,1.0 | M2,– | 178.03/119.62 | 297.65 |
| Rule2 | 1.2,2.1 | M2,M4 Line | 112.50/83.66 | 196.16 |
| Rule2 | 1.2,2.1 | M2,– | 119.29/87.39 | 206.68 |
| 1-VSS | 1.2,1.0 | M2,M4 Line | 136.17/96.66 | 232.83 |
| 1-VSS | 1.2,1.0 | M2,– | 139.14/98.28 | 237.42 |
| Rule3 | 2.2,2.2 | M2,M4 Line | 130.08/50.90 | 180.98 |
| Rule3 | 2.2,2.2 | M2,– | 130.40/50.99 | 181.39 |
| 2-VSS | 1.2,2.1 | M2,M4 Line | 104.34/80.83 | 185.17 |
| 2-VSS | 1.2,2.1 | M2,– | 121.14/78.53 | 199.67 |

# Repeater Offsets for Global Buses

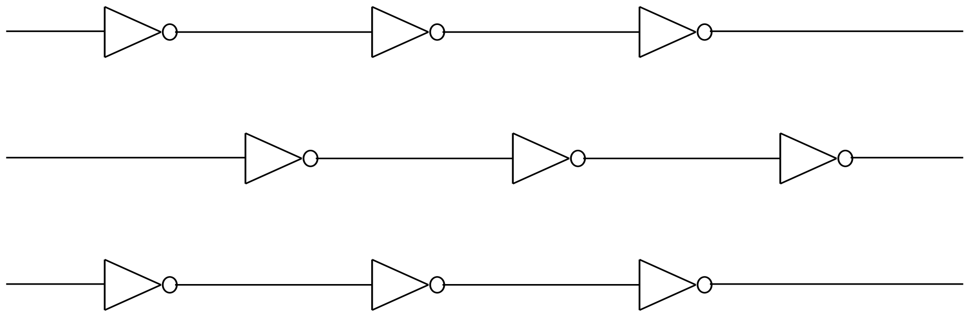
- **Motivations**
  - global interconnect dominated by wide buses
  - present methodology uses periodic repeater blocks
  - present methodology designs for worst-case SF

- **New idea**: Offset repeaters on adjacent lines (!)
  - worst-case switching over only half the period
  - best-case switching over the other half

# Phase 0 and 0.5 Repeater Offset



(a)



(b)

# Experiment Setup

- Three parallel lines, length $= 10000\mu m, 14000\mu m$
- Two "technologies" representing M3, M4
- Repeater period $= 4000\mu m$
- Distributed model of interconnect line, coupling parasitics
- Input slew time = 200ps
- Left, right aggressors have repeaters offset from victim at phases $\in \{0.0, 0.1, ..., 0.9\}$ times repeater period
- Inputs to three lines either rising (R) or falling (F)
- Offset of left, right line inputs by -100ps, 0ps, +100ps

# HSPICE Delays (ns), 10000$\mu m$ Lines

| Input waveforms (Left neighbor, victim, right neighbor) | Interconnect Delay ($ns$) | | |
|---|---|---|---|
| | Left,right neighbor buffer phases: 0,0 | | |
| | Left neighbor Delay | Victim Delay | Right neighbor Delay |
| R, R, R | 0.361 | 0.361 | 0.361 |
| R, R, F | 0.428 | 0.584 | 0.676 |
| R, F, R | 0.546 | 0.994 | 0.546 |
| R, F, F | 0.676 | 0.584 | 0.428 |
| F, R, R | 0.676 | 0.584 | 0.428 |
| F, R, F | 0.546 | 0.994 | 0.546 |
| F, F, R | 0.428 | 0.584 | 0.676 |
| F, F, F | 0.361 | 0.361 | 0.361 |

# Worst-Case Delays, Input Offsets = 0ps

| **Line length 14000 $\mu$m, Technology II** | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Right Neighbor Phase | | | | | |
| | | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 |
| Left Neighbor Phase | 0 | **2.123** | 2.108 | 2.085 | 2.052 | 2.011 | 1.983 |
| | 0.1 | 2.108 | 2.092 | 2.064 | 2.029 | 1.985 | 1.943 |
| | 0.2 | 2.085 | 2.064 | 2.036 | 1.996 | 1.947 | 1.889 |
| | 0.3 | 2.052 | 2.029 | 1.996 | 1.952 | 1.898 | 1.823 |
| | 0.4 | 2.011 | 1.985 | 1.947 | 1.898 | 1.837 | 1.743 |
| | 0.5 | 1.983 | 1.943 | 1.889 | 1.823 | 1.743 | **1.590** |
| | 0.6 | 1.925 | 1.876 | 1.816 | 1.765 | 1.703 | 1.664 |
| | 0.7 | 1.938 | 1.913 | 1.878 | 1.833 | 1.778 | 1.744 |
| | 0.8 | 1.995 | 1.974 | 1.944 | 1.903 | 1.854 | 1.823 |
| | 0.9 | 2.056 | 2.039 | 2.012 | 1.977 | 1.932 | 1.903 |

# Worst-Case Delays Over All Input Offsets

| **Line length 14000 $\mu$m, Technology II** | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Right Neighbor Phase | | | | | |
| | | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 |
| | 0 | **2.213** | 2.190 | 2.157 | 2.116 | 2.069 | 2.031 |
| | 0.1 | 2.190 | 2.161 | 2.125 | 2.081 | 2.029 | 1.982 |
| Left | 0.2 | 2.157 | 2.125 | 2.085 | 2.035 | 1.977 | 1.920 |
| | 0.3 | 2.116 | 2.081 | 2.035 | 1.980 | 1.913 | 1.846 |
| Neighbor | 0.4 | 2.069 | 2.029 | 1.977 | 1.913 | 1.837 | 1.775 |
| | 0.5 | 2.031 | 1.982 | 1.920 | 1.846 | 1.775 | **1.666** |
| Phase | 0.6 | 1.974 | 1.930 | 1.879 | 1.818 | 1.750 | 1.730 |
| | 0.7 | 2.027 | 1.991 | 1.946 | 1.893 | 1.831 | 1.804 |
| | 0.8 | 2.084 | 2.053 | 2.013 | 1.965 | 1.909 | 1.879 |
| | 0.9 | 2.147 | 2.119 | 2.084 | 2.041 | 1.989 | 1.955 |

# Summary and Ongoing Research

- Demonstration of experimental methodology
- Surprising observations
  - shield wiring not helpful
  - new offset methodology for repeaters in global buses
- Ongoing extensions
  - varying ILD and interconnect thicknesses
  - noise coupling analyses, tuning for noise margin
  - new materials (copper, low-k)
- **Ultimate goal**: full-chip interconnect tuning based on interconnect structure, PDA target