More Practical Bounded-Skew Clock Routing

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Contributions

Practical bounded-skew clock routing

- Varying layer parasitics, non-zero via parasitics
- Obstacle avoidance
- New topology design rule for prescribed-delay case
- Predictive modeling of clock routing cost

Outline of Talk

- Problem formulation
- Previous work
- Varying layer parasitics, non-zero via parasitics
- Obstacle-avoidance
- Topology generation for prescribed-delay case
- Predictive modeling of clock routing cost
- Future work

Review of Bounded-Skew Tree (BST) Problem

Given

- Sink locations $S = \{ s_1, s_2, ..., s_n \}$
- Optional source location s_0
- Optional prescribed topology G
- Skew bound B

Find: BST over S

- Total wirelength is minimized
- Max difference of source-sink delays $\leq B$

Outline of Talk

- Problem formulation
- Previous work
  - Extended DME (Ex-DME) algorithm
  - Merging regions
  - Well-behaved property
- Varying layer parasitics, non-zero via parasitics
- Obstacle-avoidance
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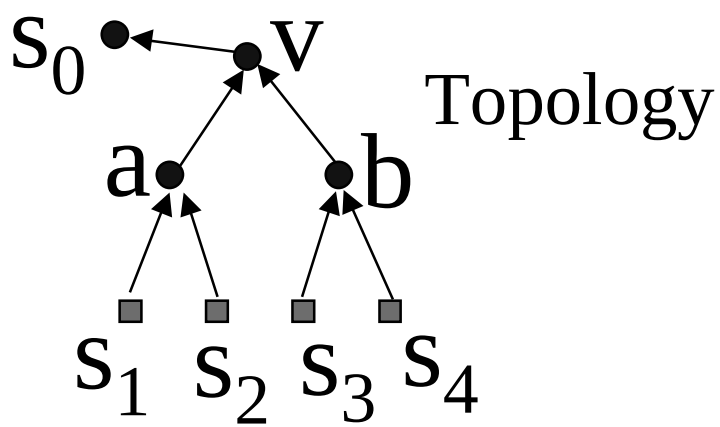
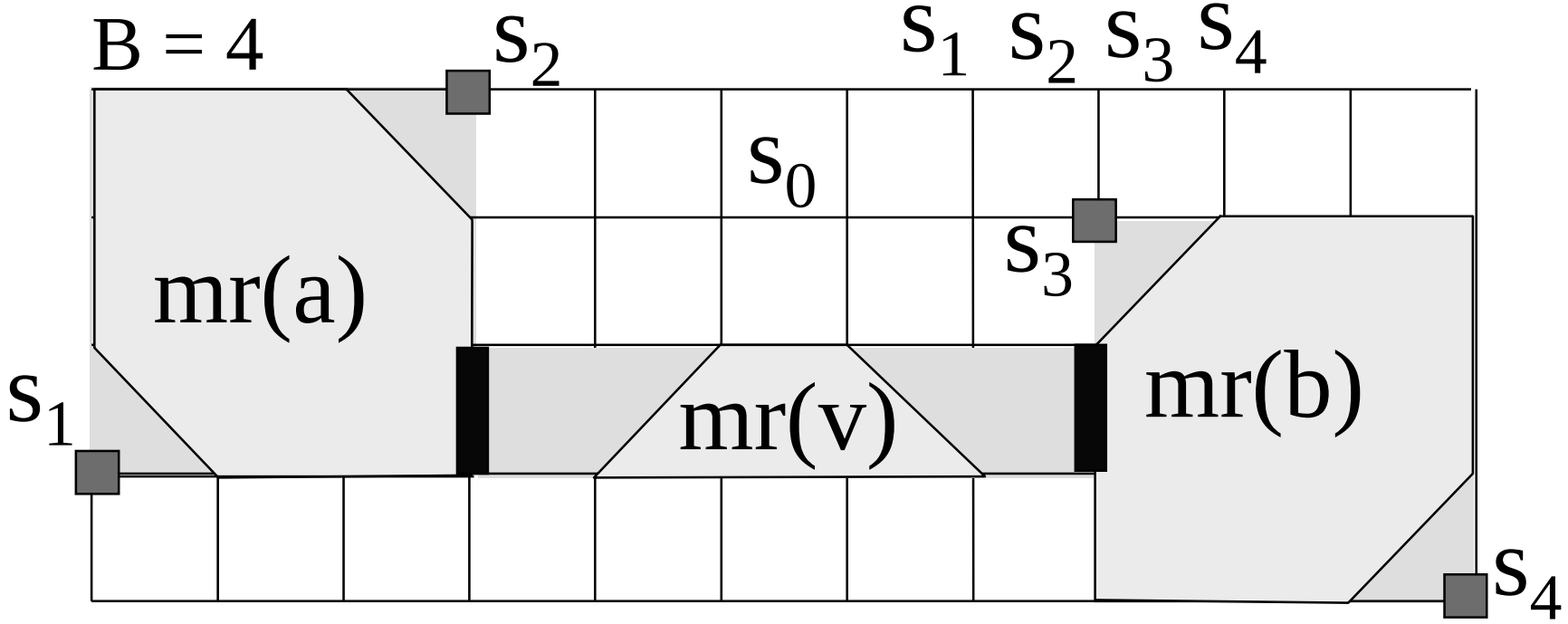
The Ex-DME Algorithm

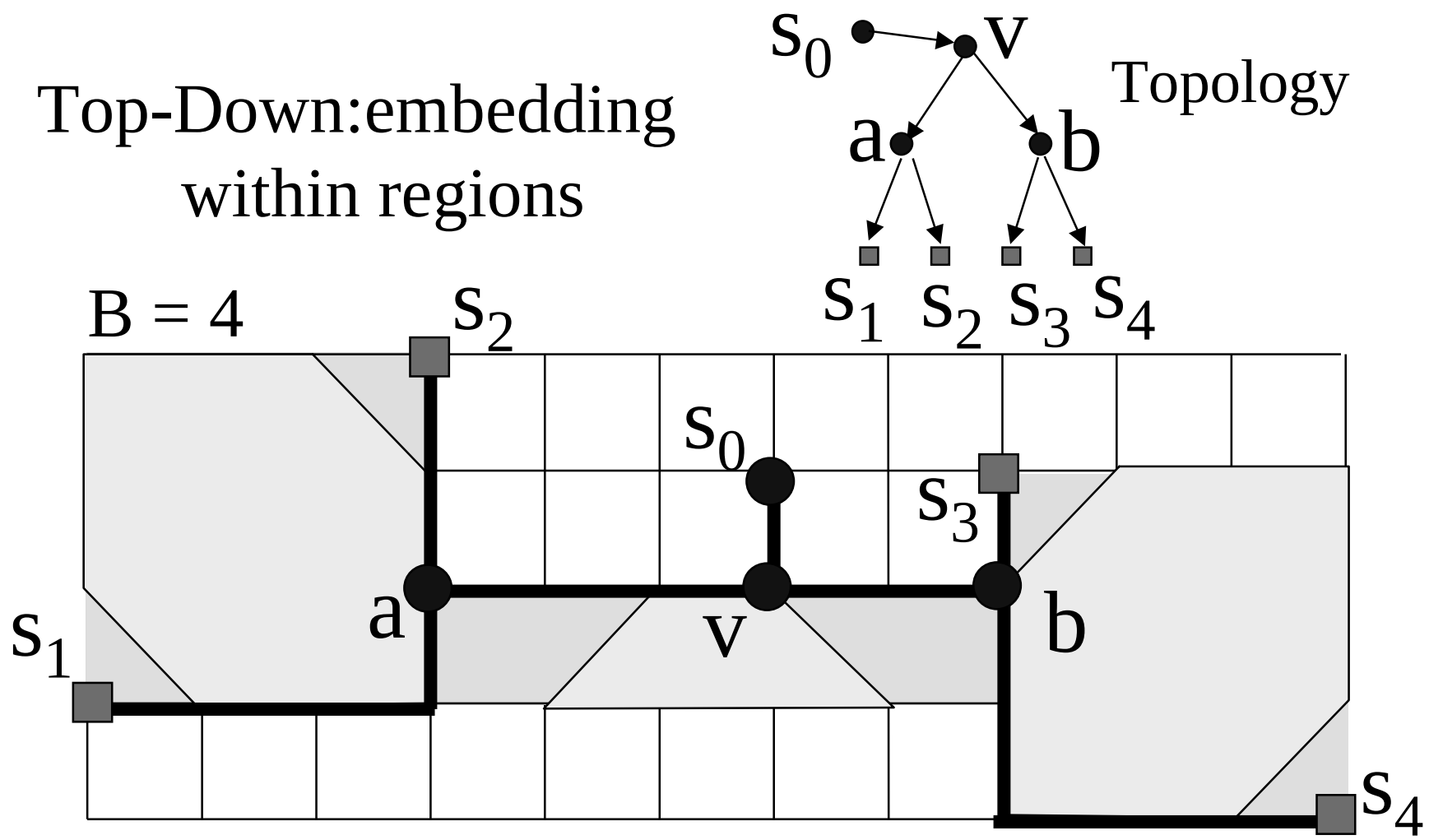
Bottom-Up: build merging regions



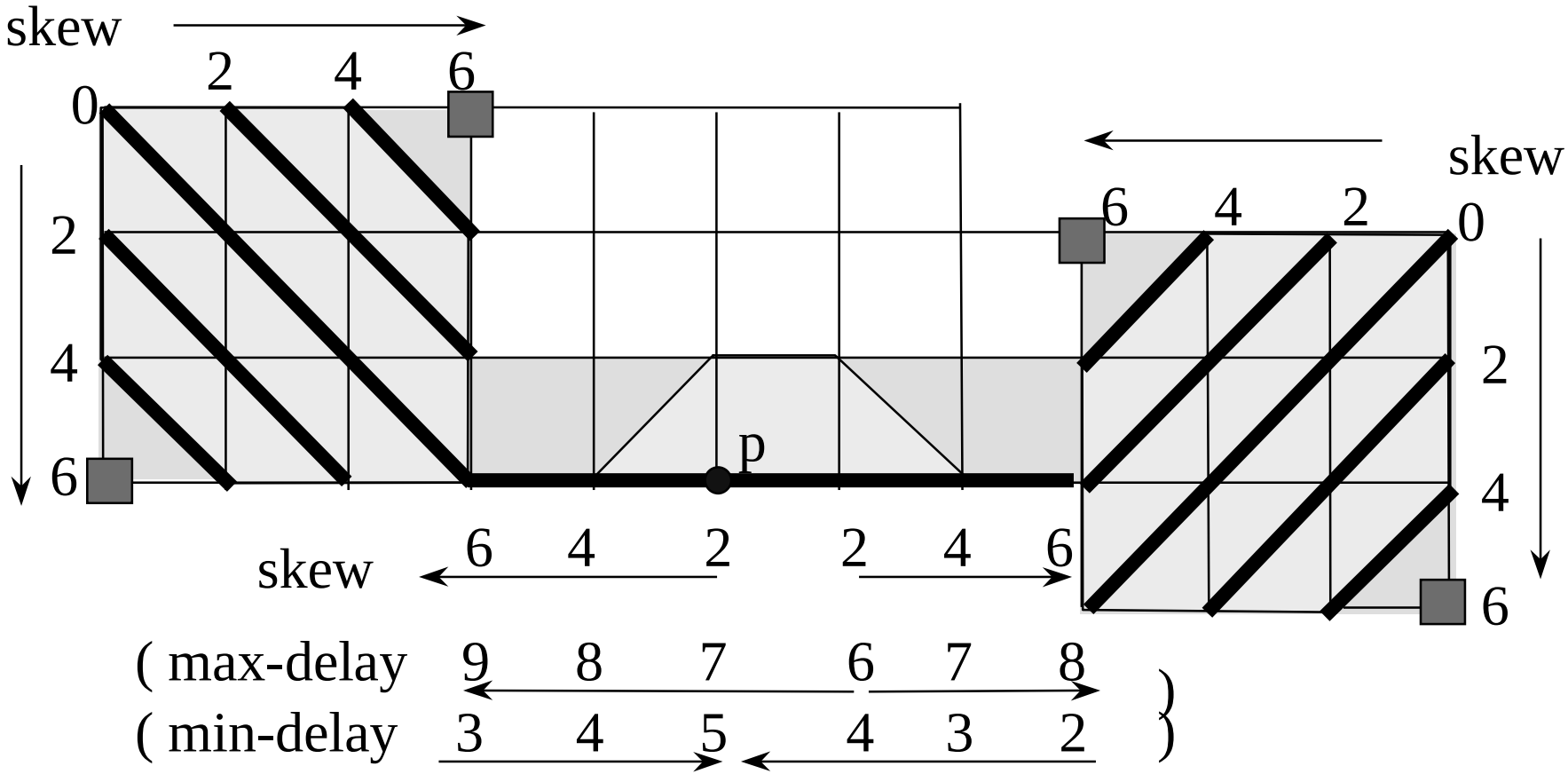


The Ex-DME Algorithm

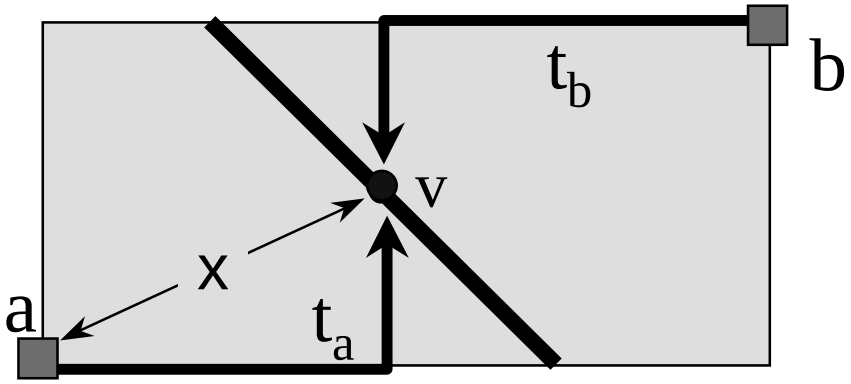
Top-Down:embedding within regions



Well-Behaved Property



Well-Behaved Elmore Property



- $K = r \cdot c/2$

- $t_a = K \cdot x^2 + \alpha \cdot x + \Phi_a$ $\quad t_b = K \cdot x^2 + \beta \cdot x + \Phi_b$
- $max_t(v) = max(t_a, t_b) = K \cdot x^2 + max(\alpha \cdot x + \Phi_a, \beta \cdot x + \Phi_b)$

  $min_t(v) = min(t_a, t_b) = K \cdot x^2 + min(\alpha \cdot x + \phi_a, \beta \cdot x + \phi_b)$

skew = max_t - min_t = piece-wise linear function of x

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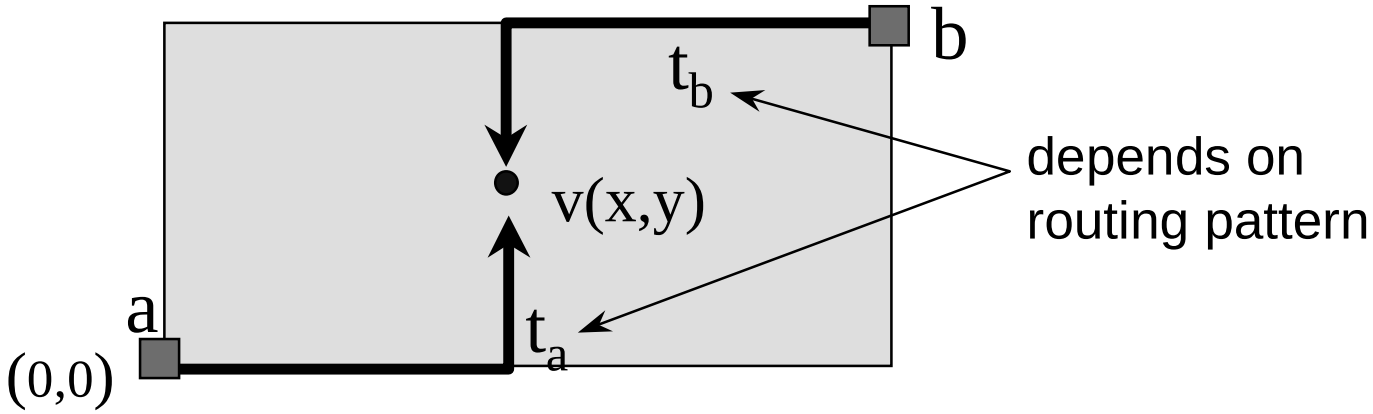
- Problem formulation
- Previous work
- Varying layer parasitics, non-zero via parasitics
- Obstacle-avoidance
- Topology generation for prescribed-delay case
- Predictive modeling of clock routing cost
- Future work

Varying Layer Parasitics



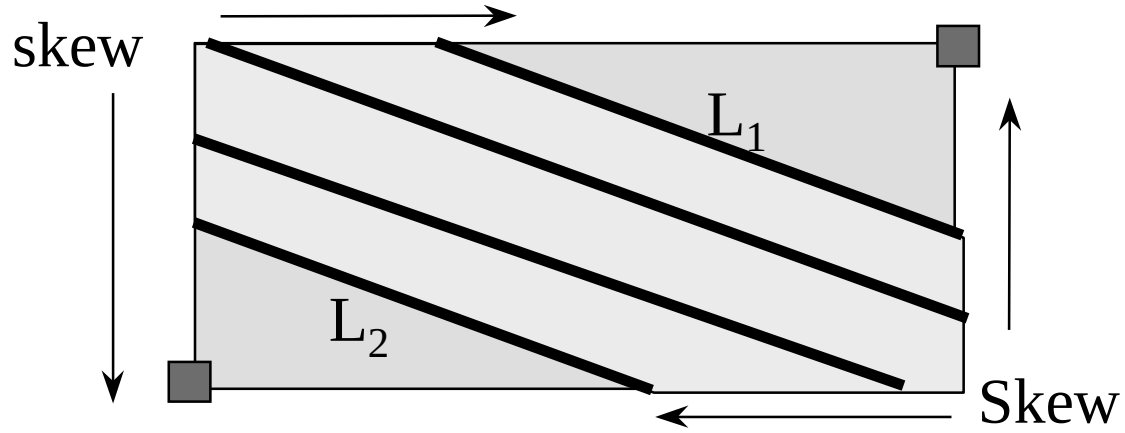
- $t_a = K_1 \cdot x^2 + K_2 \cdot y^2 + G \cdot xy + \alpha \cdot x + \gamma \cdot y + \Phi_a$
- $t_b = K_1 \cdot x^2 + K_2 \cdot y^2 + G \cdot xy + \beta \cdot x + \theta \cdot y + \Phi_b$
- $\max_t(v) = K_1 \cdot x^2 + K_2 \cdot y^2 + G \cdot xy + \max(\alpha \cdot x + \gamma \cdot y + \Phi_a , \beta \cdot x + \theta \cdot y + \Phi_b)$

  $\min_t(v) = K_1 \cdot x^2 + K_2 \cdot y^2 + G \cdot xy + \min(\alpha \cdot x + \gamma \cdot y + \phi_a , \beta \cdot x + \theta \cdot y + \phi_b)$

- $K_1 = r_1 \cdot c_1/2$
- $K_2 = r_2 \cdot c_2/2$
- $G = r_2 \cdot c_1$

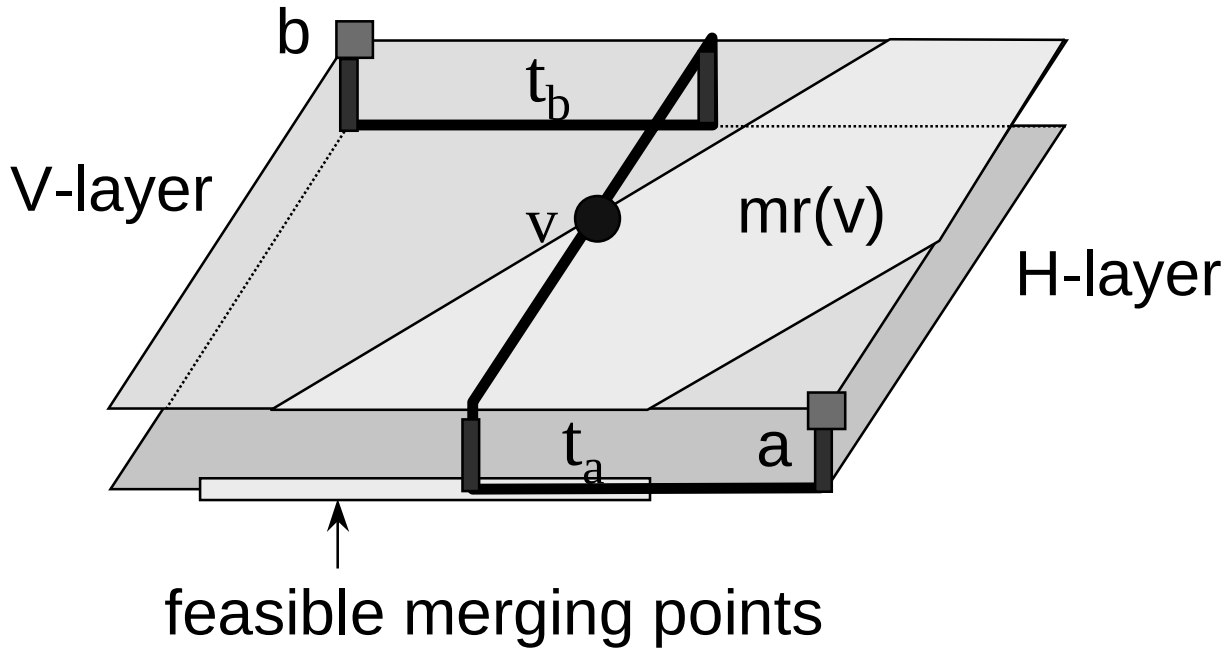
Skew = piece-wise linear function of x, y

Varying Layer Parasitics (cont.)



- L_1 , L_2 : parallel, slopes $\neq \pm 1$
  - ➪ Joining segments: slopes $\neq \pm 1$
- Rectilinear joining segments
  - ➪ treated as in case of uniform layer parasitics

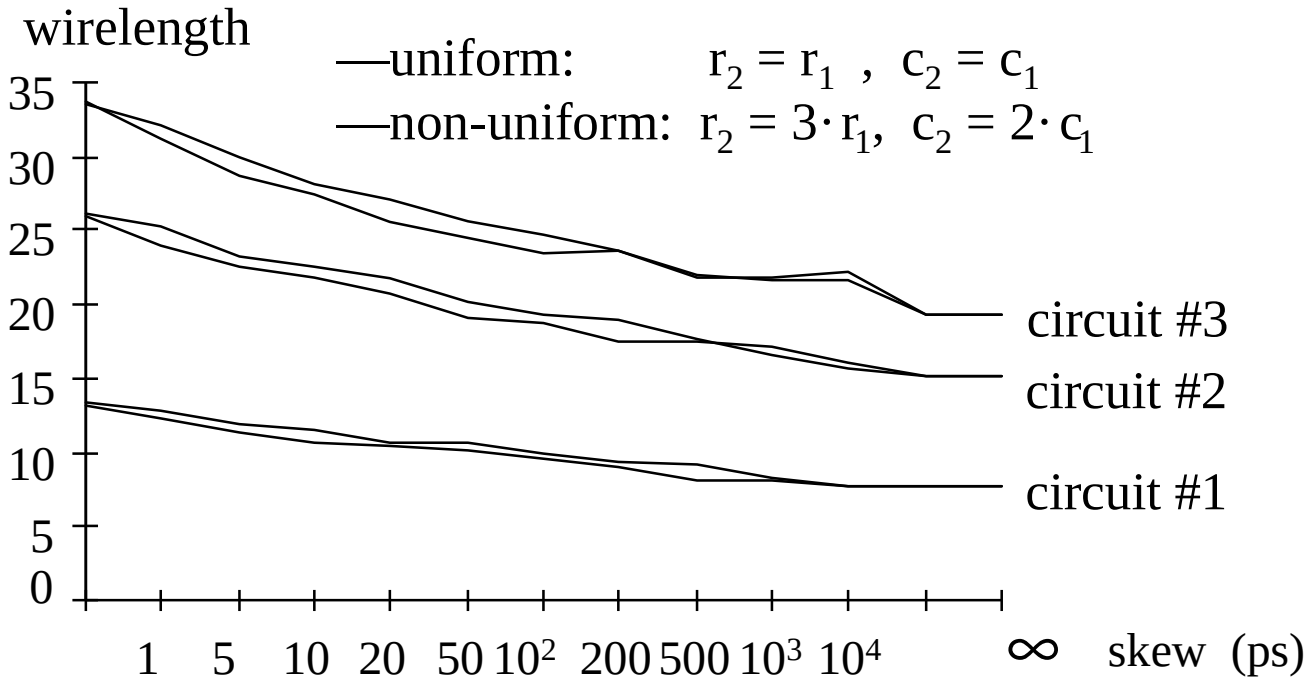
Varying Layer Parasitics With Non-Zero Via Parasitics



Delay increase of t_a , t_b due to vias ≡ linear function of x

Experiments

- Exp 1



- Exp 2： Vary $(r_2 \cdot c_2)/(r_1 \cdot c_1)$ from 1 to 10 on circuit #1
  - ➪ wirelength increase of zero-skew routing is $\leq 4\%$

Outline of Talk

- Problem formulation
- Previous work
- Varying layer parasitics, non-zero via parasitics
- Obstacle-avoidance
  - Planar merging region
  - Obstacle Expansion rules
  - Extends to varying layer parasitics
- Topology generation for prescribed-delay case
- Predictive modeling of clock routing cost
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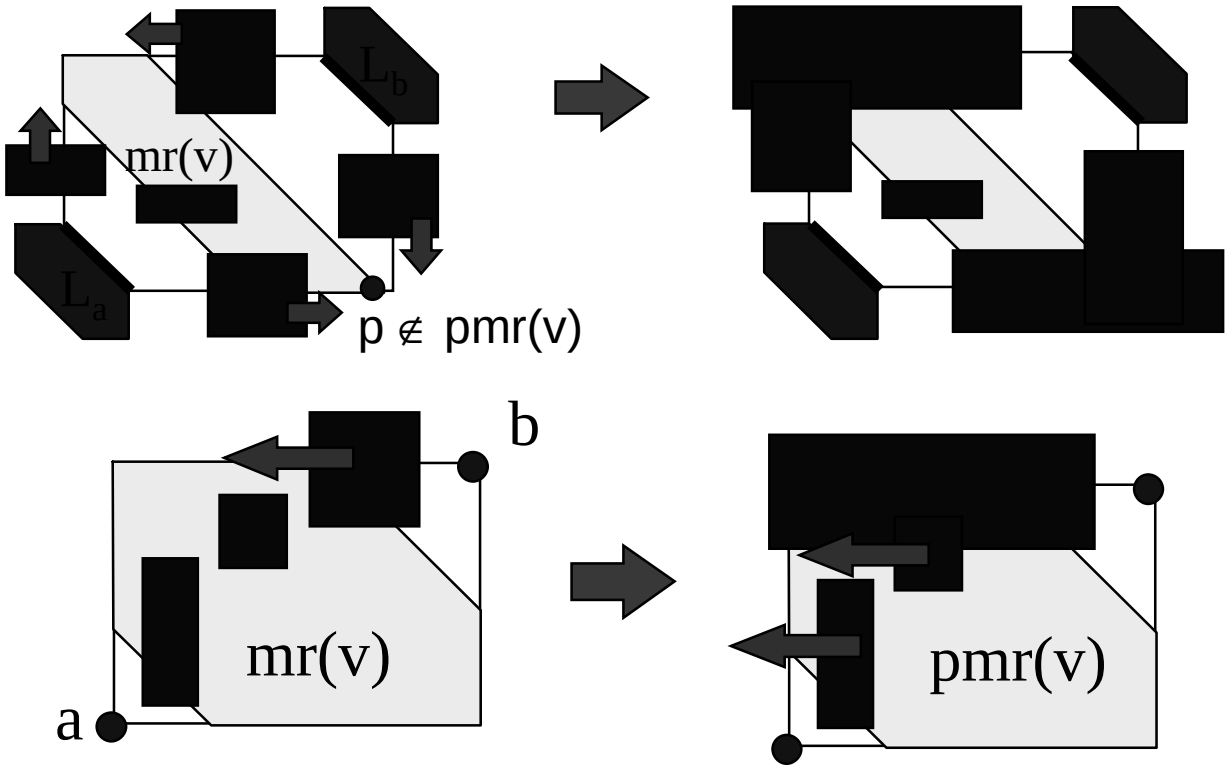
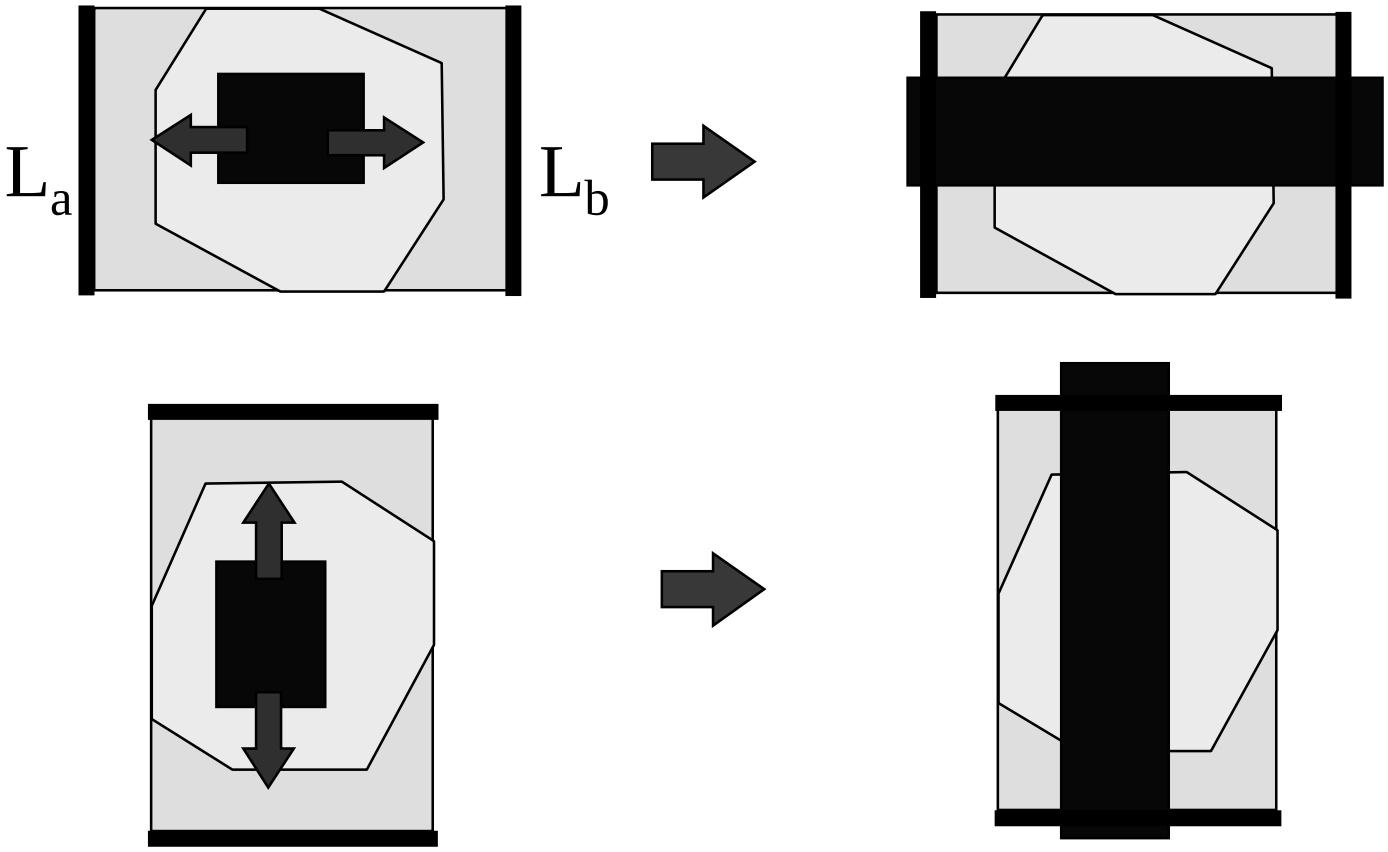
Obstacle Expansion: Case I

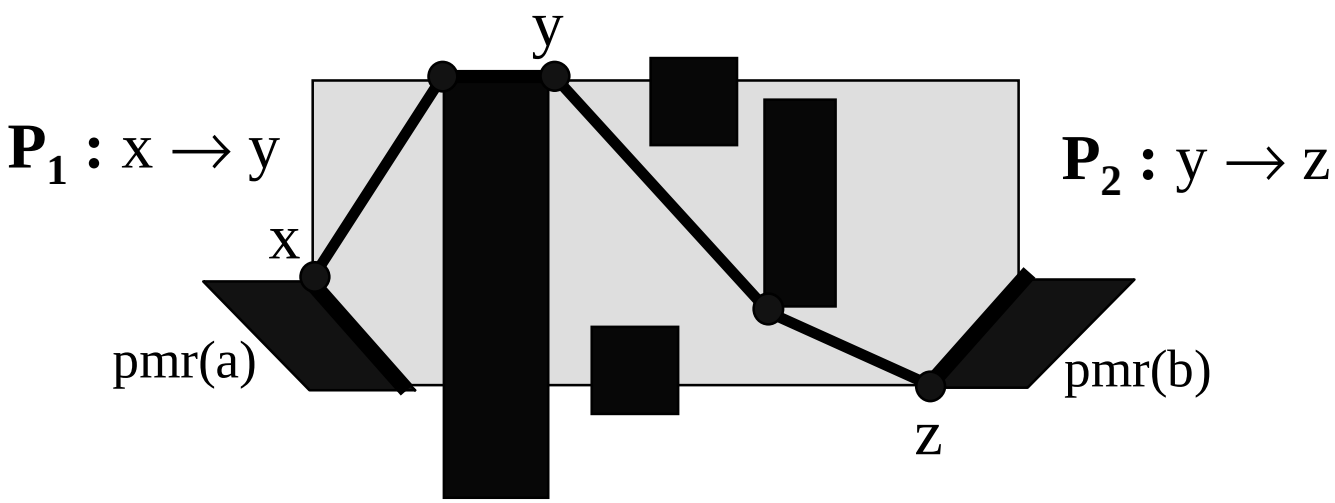


Chain reaction

Obstacle Expansion: Case II

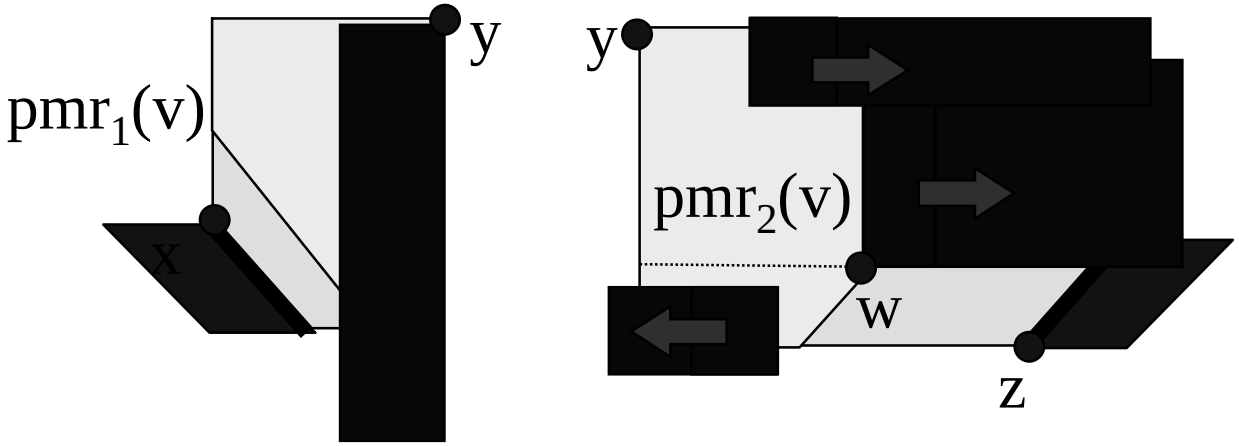


Construction of Planar Merging Regions



- Find shortest planar path **P** between child regions
- Divide **P** into min. # of subpaths $\mathbf{P_i}$: $s_i \rightarrow t_i$ with pathlength($\mathbf{P_i}$) = dist(s_i , t_i)

Construction of Planar Merging Regions (cont.)

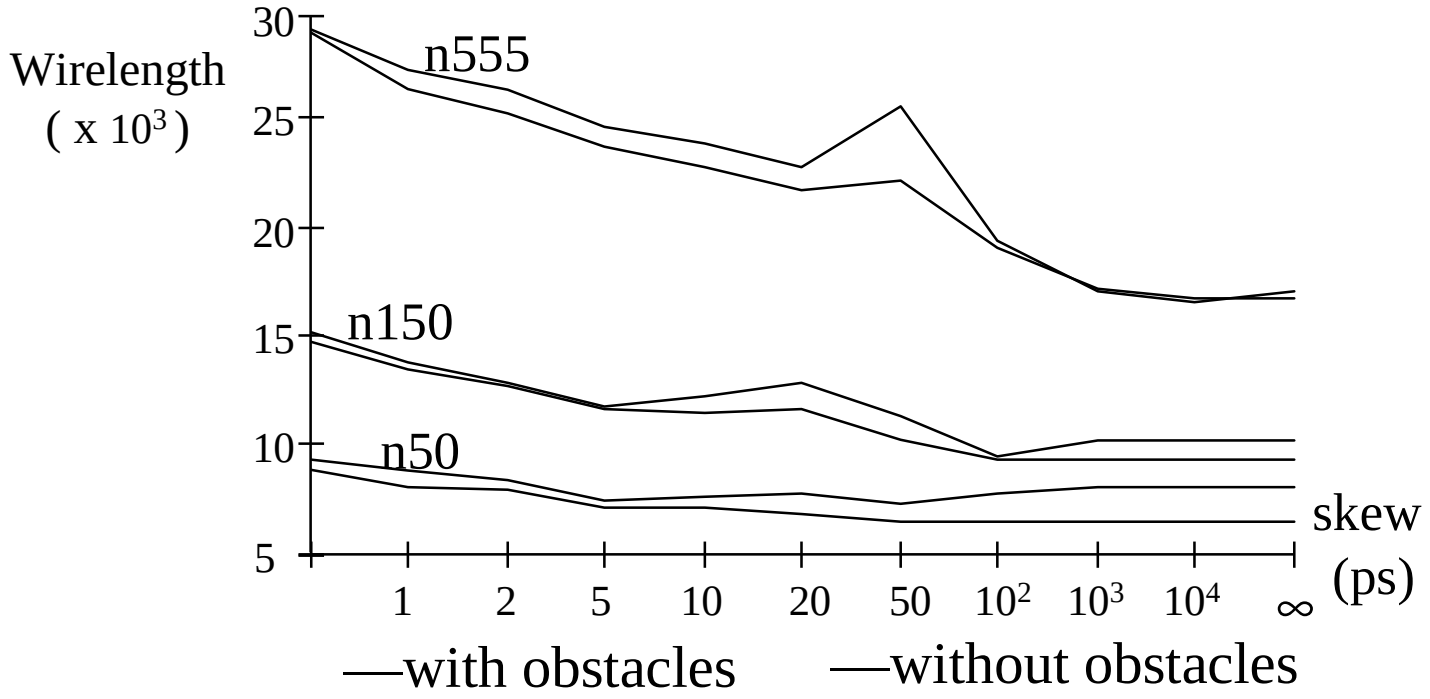


$$pmr(v) \equiv pmr_1(v) \cup pmr_2(v)$$

For each subpath $P_i : s_i \rightarrow t_i$

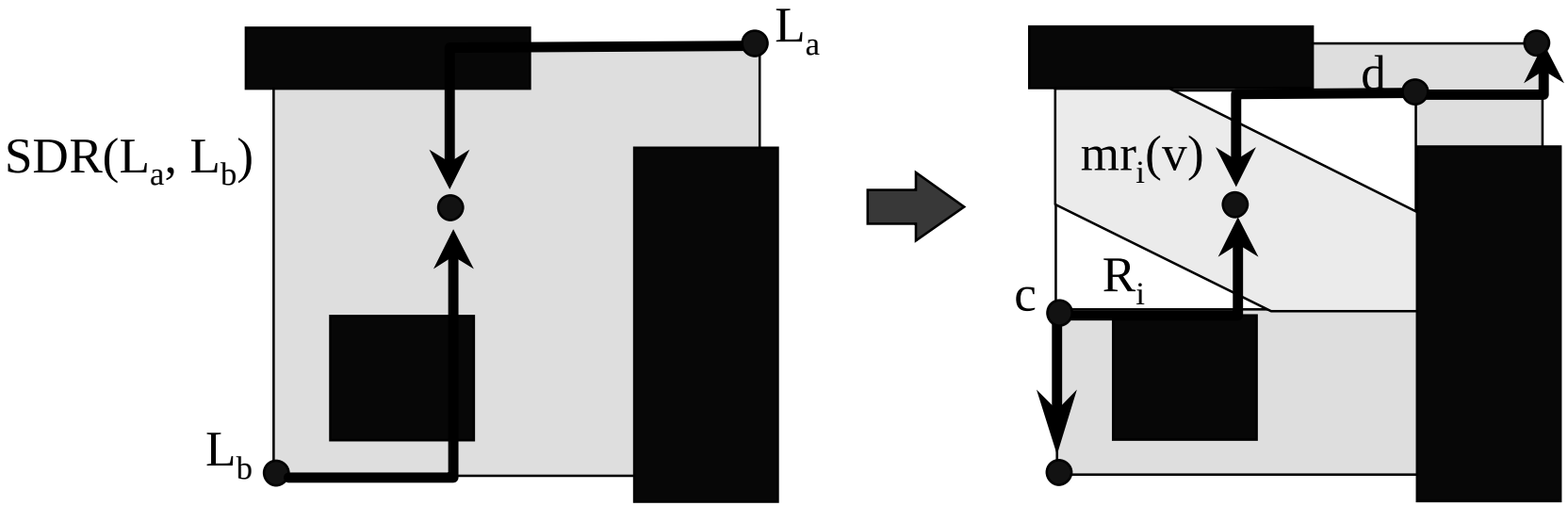
- compute $mr_i(v)$ from s_i , t_i
- compute $pmr_i(v) \equiv mr_i(v)$ - expanded obstacles

Experiments



- 40 obstacles randomly distributed in a 100 x 100 square

Extension To Varying Layer Parasitics



- Only consider the case when L_a, $L_b \equiv$ single points
- SDR(L_a, L_b) decomposed to obstacle-free R_i
- $pmr(v) \equiv \cup\, mr_i(v)$, constructed within R_i

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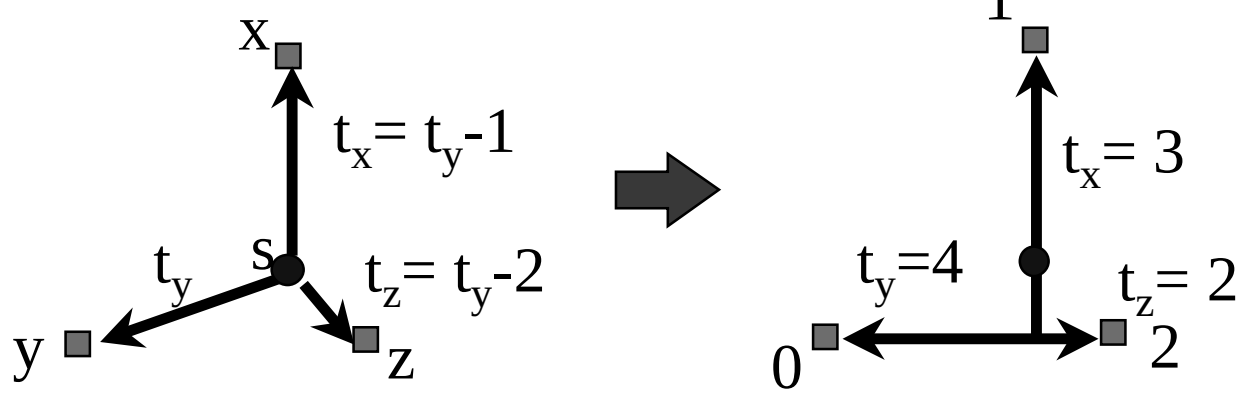
Clock Routing With Prescribed Delays At Sinks

- Sinks (FF's/buffers) in clock routing have non-uniform delays
- Prescribed (local) skew routing ≡ zero-skew routing with prescribed delays



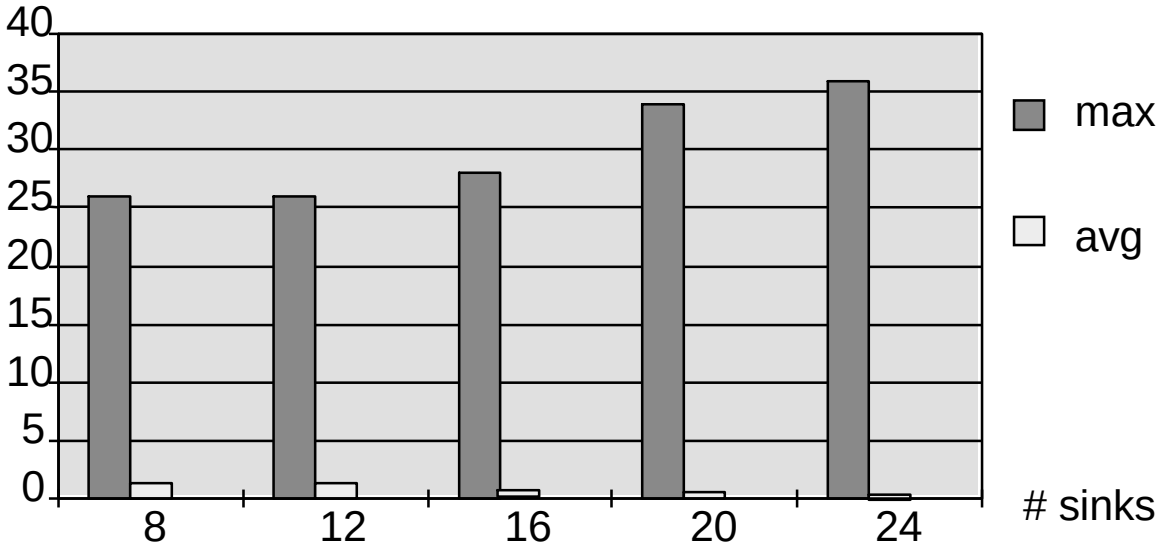
skew(x,y) ≡ $t_x - t_y = -1$

skew(y,z) ≡ $t_y - t_z = +2$

New Prescribed-Delay Topology Rules

New criterion for selecting merging pairs:

- $\alpha \cdot$ wirelength + (1- α) $\cdot$ resulting subtree delay



Improvement of Meta(Orig,New) over Orig (%)

Orig: $\alpha = 0$ New : $\alpha = 0.67$

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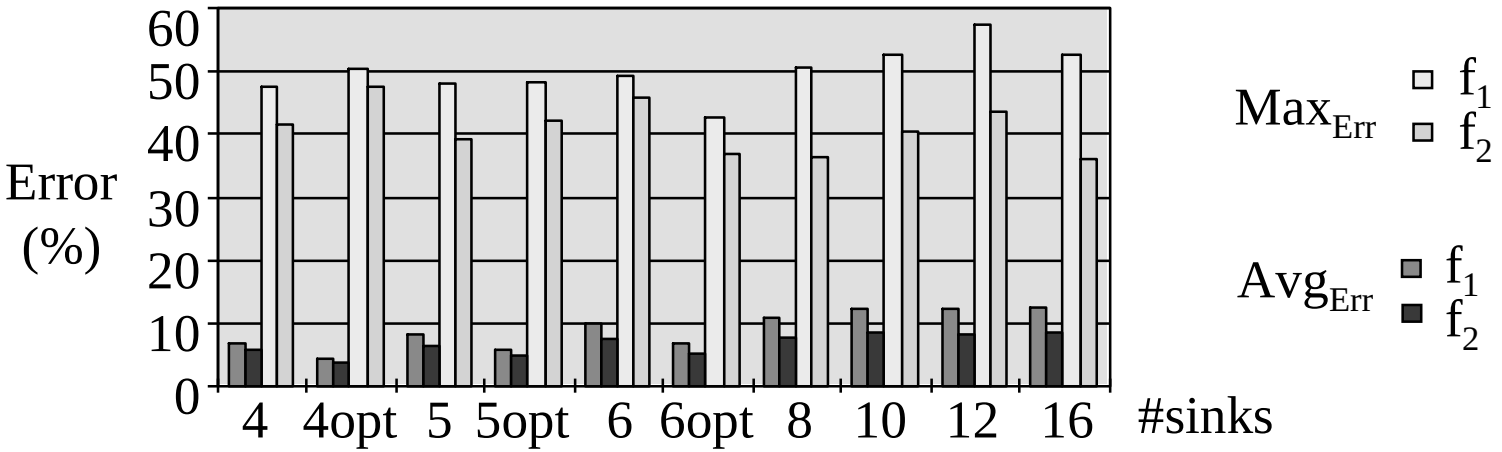
Predictive Modeling of BST Cost

- Essential for sink clustering in synthesis of buffered clock topology
- cost (BST) $\equiv c_1 \cdot p_1^{e1} + c_2 \cdot p_2^{e2} + \ldots + c_k \cdot p_k^{ek}$

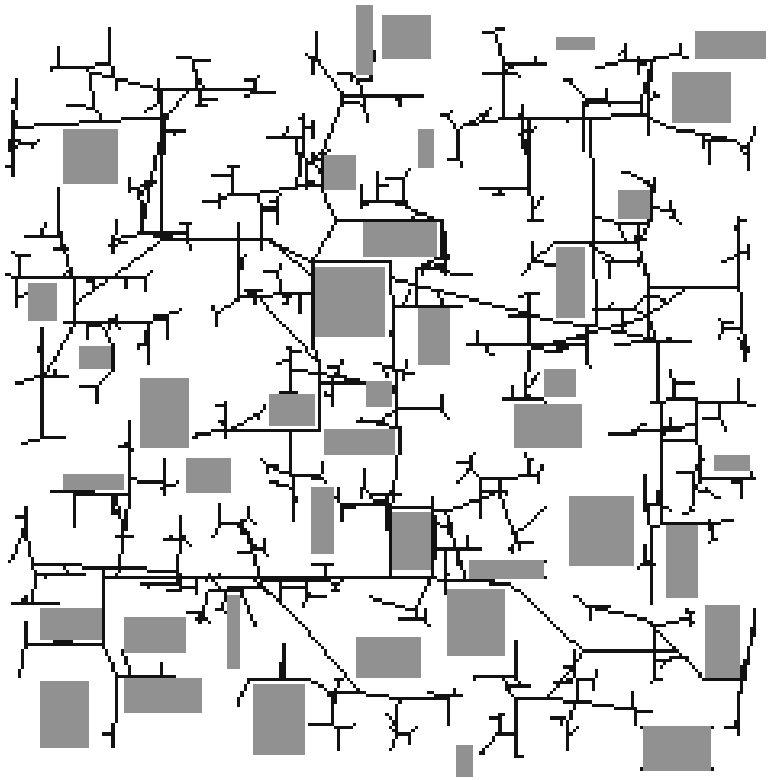


f_1 (MST cost)
f_2 (MST cost, center-of-gravity star cost, B, max sink delay)

Future Work

- Multi-layer clock routing for varying layer parasitics with obstacles on any layers
- Better topology rules considering obstacles and prescribed delays at sinks
- Integration with buffered clock tree design tool

Experiments: Example



Zero-skew routing for 555 sinks with 40 obstacles