Analysis and Justification of a Simple, Practical 2 1/2-D Capacitance Extraction Methodology *

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Abstract

This paper addresses post-routing capacitance extraction during performance-driven layout. We first show how basic drivers in process technology (planarization and minimum metal density requirements) actually simplify the extraction problem; we do this by proposing and validating five "foundations" through detailed experiments with representative $0.18\mu m$ process parameters and a 3-D field solver. We then present a simple yet accurate 2 1/2-D extraction methodology directly based on the foundations. This methodology has been productized and is being shipped with the Cadence Silicon Ensemble 5.0 product. We conclude that the 2 1/2-D approach has sufficient accuracy for current and near-term process generations.

1 Introduction

In deep-submicron VLSI, complex 3-dimensional interconnect structures pose a difficult challenge for parasitic capacitance extraction. Many extraction approaches exist, including 1-D, 2-D and 2 1/2-D analytic models [2, 4, 10, 5, 1] as well as 2-D and 3-D field solvers [11, 9, 7, 8]. The post-routing capacitance extraction during performance-driven layout design must be accurate, since correlation with "final" verification engines is needed for design convergence. It must also be fast, since even with net-filtering approaches, it may be performed dozens of times on full-chip layout, and thousands of times on critical signal nets, during iterative layout design. Simple 1- and 2-D extraction may not suffice in deep-submicron design: (i) wire aspect ratios (thickness divided by width) have reached 1.5 in $0.35\mu m$ logic processes, and will reach 2.5 in $0.18\mu m$ logic processes [13] so that lateral and fringe couplings become more significant, and (ii) increased packing densities, lower supply voltages, and use of dynamic logic all lead to lower noise margins, so that crossover and crossunder couplings must be modeled. At the same time, full 3-D numerical extraction is difficult to support during layout. For these reasons, the 2 1/2-D approach has been well-studied recently [5, 3, 1].

Our first contribution shows how basic drivers in process technology (planarization and minimum metal density requirements) actually simplify the capacitance extraction problem. We propose and validate five "foundations" through detailed experiments with representative $0.18\mu m$ process parameters and a 3-D field solver. Our second contribution is a simple yet accurate 2 1/2-D extraction methodology directly based on these foundations. It has recently been developed and validated in cooperation with major ASIC suppliers, and is being shipped with the first release of the Cadence Silicon Ensemble (SE) 5.0 product.

2 Foundations

2.1 Preliminaries

A multilayer VLSI process has metal interconnects, or wires, on layers $1, 2, \ldots, k$ (i.e., M1, M2, ..., Mk). Currently, there are $k = 6$ layers in leading-edge processes, but $k = 8$ or more will be seen by the turn of the century. We call the multilayer geometric structure of wires a *pattern*. We assume that wires in adjacent layers are orthogonal, which is often true in gate-array and standard-cell ASIC designs. We use geometric parameters of maximum-density local interconnects in emerging $0.18\mu m$ processes[1] (see Table 22 in [13]), and normalize all dimensions with respect to the minimum wire width in a given pattern. The following *normalized* dimensions are used: wire width = 1.0, wire thickness = 2.5, and dielectric height between adjacent layers = 3.0. Let s be the edge-to-edge spacing between a wire (the *victim*) and its same-layer neighboring wires (*neighbors*). We typically study the "extreme" cases of $s = 1.0$ and $s = \infty$, with the latter meaning that the neighbors are too far away to have significant coupling to the victim.

We use an industrial-strength multipole-accelerated 3-D field solver, Fastcap[2] [8], to obtain coupling capacitances between multiple conductors in the form of a capacitance matrix. Since we run Fastcap on normalized patterns in free space, we obtain *normalized capacitances* as output. For example, if the minimum wire width in a pattern is $0.36\mu m$, a normalized capacitance of $100pF$ implies actual capacitance of

$$100(pF) \cdot 0.36(\mu m/m) \cdot \epsilon_r = 0.1404fF$$

where we assume that the relative permittivity of SiO_2 is $\epsilon_r = 3.9$. We will report only *normalized* values for all dimensions and capacitances (in units of pF), as only the ratios between different capacitance values are significant.

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[1] Experimental results for $0.5\mu m$ processes (aspect ratio 1.0) and $0.35\mu m$ processes (aspect ratio 1.5) can be found in [6].

[2] Fastcap is a public-domain program available by anonymous ftp from rle-vlsi.mit.edu. It is an element of several commercial products, e.g., from Quantic and Ansoft.

0-89791-847-9/97/0006/$3.50 DAC 97 - 06/97 Anaheim, CA, USA

2.2 Coupling between wires on layer i and wires on layer $i-2$

Two experiments study coupling between wires on layers i and $i-2$, as well as effects of ground planes and same-layer neighboring wires. The pattern for the first experiment has one wire (*victim*) on layer i and one wire on layer $i-2$, but no wires on layer $i-1$ (see Figure 1). Let s_{center} be the horizontal distance between the *centers* of the two wires. We shift the wire on layer $i-2$ and observe the change of the ratio between $C_{i,i}/C_{i,i-2}$, where $C_{i,i}$ is the total capacitance for the victim, and $C_{i,i-2}$ the coupling between the two wires. We also study the two cases where layer $i-3$ is ground, and where there is no ground at all. Last, we consider two possible spacings ($s = 1.0, \infty$) for the two same-layer neighbors of the victim. All wires have length 20 and the ground is a 40×40 plane. Table 1 shows the following:

(i) The ground has a strong shielding effect on $C_{i,i-2}$. In the case of no neighbors and full overlap ($s_{center} = 0$), $C_{i,i-2}/C_{i,i} = 28.4\%$ when there is no ground versus 16.3% when there is a bottom ground plane.

(ii) Neighboring wires also have a significant shielding effect on $C_{i,i-2}$. With two neighbors at $s = 1.0$, $s_{center} = 0$ and a bottom ground present, $C_{i,i-2}/C_{i,i} = 1.8\%$ versus 16.3% when there are no neighbors.

(iii) The parallel-plate capacitance from overlap of the victim on layer i and the wire on layer $i-2$ is not the dominant component in the coupling. From full overlap ($s_{center} = 0$) to non-overlap ($s_{center} = 1$), relative changes in the coupling capacitance are less than 2%.

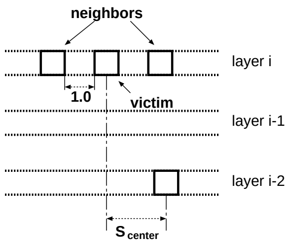

Figure 1: Cross-section of a pattern in the first experiment of Section 2.2.

s_{center}	$s = \infty$		$s = 1.0$	
	with ground	w/o ground	with ground	w/o ground
0.0	486.6/79.49	458.4/130.1	1428/24.77	1424/37.96
1.0	486.5/78.78	451.9/127.4	1428/24.41	1424/37.63
4.0	484.6/71.70	454.8/123.1	1428/21.03	1424/36.91
10.0	479.4/46.96	446.5/100.4	1427/12.30	1424/24.40

Table 1: $C_{i,i}/C_{i,i-2}$, where $C_{i,i}$ is total capacitance of the layer-i victim, and $C_{i,i-2}$ is its coupling to the wire on layer $i-2$.

In practice, there is always at least one ground (e.g., the substrate), and the likelihood of neighboring wires is high (see Footnote 3). Furthermore, it is unlikely that there are no wires on layer $i-1$. We study the effect of wires on layer $i-1$ using a pattern with one wire on layer i (the victim), one parallel and fully-overlapped wire on layer $i-2$ (similar to $s_{center} = 0$ in the first experiment), and a number of wires (*crossunders*) on layer $i-1$ (see Figure 2). We vary the number of crossunders and observe the change in both $C_{i,i}$ and the ratio $C_{i,i}/C_{i,i-2}$.

Again, four possible combinations are studied: (i) layer $i-3$ is a bottom plane, or there is no ground; and (ii) the victim has two same-layer neighbors at spacing $s = 1.0$ or $s = \infty$. All wires have length 20 and the ground is a 40×40 plane. Crossunders on layer $i-1$ are evenly distributed over the ground plane. The capacitance values are given in Table 2, where 2x - 12x indicates from 2 to 12 crossunders on layer $i-1$. Note that 12x corresponds to 30% of the area on layer $(i-1)$ being occupied.[3] We observe that, in addition to the strong shielding effect on $C_{i,i-2}$ due to the ground or same-layer neighbors, more crossunders on layer $i-1$ imply less significant $C_{i,i-2}$. When there are twelve crossunders and a bottom ground, $C_{i,i-2}/C_{i,i} = 0.4\%$ with no neighbors on layer i, and 0.2% with two neighbors on layer i. Given the minimum area occupancy of metal layers in deep-submicron processes, the coupling between a wire on layer i and a wire on layer $i-2$ is not significant. We conclude the following from these two experiments:

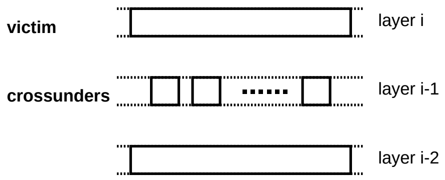

Figure 2: Cross-section for a pattern in the second experiment of Section 2.2.

	$s = \infty$		$s = 1.0$	
	with ground	w/o ground	with ground	w/o ground
2x	534.5/48.45	521.5/82.3	1433/16.64	1427/25.25
4x	581.3/21.99	578.5/31.6	1437/9.185	1450/11.54
8x	622.2/3.47	622.5/6.86	1440/3.45	1457/2.67
12x	635.9/2.47	636.7/4.21	1443/2.43	1458/1.95

Table 2: $C_{i,i}/C_{i,i-2}$ values for the second experiment of Section 2.2.

Foundation 1 *Ground, and neighboring wires on the same layer, have significant shielding effects. Thus, both must be considered for accurate modeling.*

Foundation 2 *Coupling between wires in layer $i+1$ and wires on layers $i-1$ is negligible when the metal density on layer i exceeds a certain threshold.*

These two foundations are further verified below. Foundation 2 implies that capacitance extraction can be simplified by treating layer $i-2$, and symmetrically layer $i+2$, as ground planes. We now verify this.

2.3 Coupling between wires on layers $i \pm 2$ and i

Three experiments show that layers $i \pm 2$ can be treated as ground planes for wires on layer i. In the first experiment, there is one *victim* wire of length 20 on layer i and one *crossunder* of length 20 on layer $i-1$. The *real* pattern (see Figure 3) in practice has a number of wires on layer $i-2$, with layer $i-3$ acting as a ground plane (or the substrate is a bottom ground plane). We assume that wires on layer $i-2$ are 40 units long.

[3]In deep-submicron processes ($\leq 0.35\mu m$) the minimum area occupancy of a metal layer is typically set by the foundry to 30% for uniformity of etch rate or CMP planarization. Foundries may specify certain shapes of dummy metal which are small enough so as to not hold much charge during manufacturing (e.g., 2.5 μm by 2.5 μm). The key observation is that maximum possible occupancy is 50%, even with the line-to-line spacing = 1.0. Thus, conductor structure on adjacent orthogonal wiring layers is fairly predictable.

We also solve a *model* pattern by treating layer $i-2$ as a 40×40 ground plane without looking beyond this layer (i.e., there is no ground plane on layer $i-3$). Our experiment varies the number (density) of wires on layer $i-2$ and compares $C_{i,i}$ and $C_{i,i-1}$ for different patterns. $C_{i,i}$ is again the total capacitance for the victim, and $C_{i,i-1}$ is the coupling between the victim and the crossunder. In Table 3, 2x - 16x indicates from 2 to 16 wires on layer $i-2$ for the real pattern; *GND* indicates the model pattern. Compared with the model pattern, $C_{i,i}$ in cases 8x - 16x differs by less than 0.7% when the victim has no neighbors ($s = \infty$), and by less than 0.4% when it has two neighbors at spacing $s = 1.0$; the corresponding values are 6.2% and 7.5% for $C_{i,i-1}$.

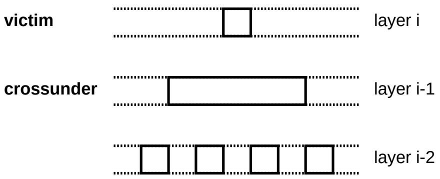

Figure 3: Cross-section of the real pattern in the first experiment of Section 2.3: the victim on layer i, one crossunder on layer $i-1$ and a number of wires on layer $i-2$. Layer $i-3$ is a ground plane, but is not shown in the figure.

layer $i-2$	$s = \infty$	$s = 1.0$
2x	513.7/112.9	1431/31.93
4x	519.5/112.0	1432/33.04
8x	527.4/100.5	1430/27.64
12x	529.5/99.17	1430/26.64
16x	530.7/98.00	1433/27.83
GND	531.0/95.46	1428/30.55

Table 3: $C_{i,i}/C_{i,i-1}$, where $C_{i,i}$ is the total capacitance of the victim, and $C_{i,i-1}$ the coupling between the victim and the crossunder.

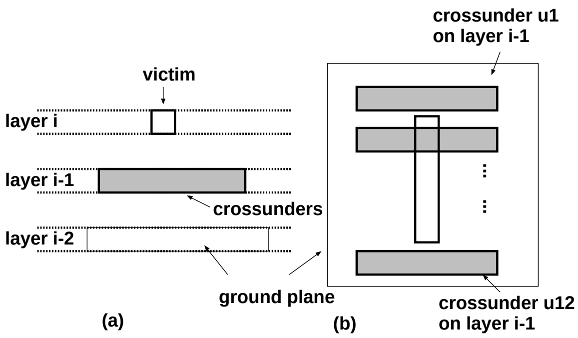

Figure 4: Layer $i-2$ is modeled as a ground plane: (a) the cross-section view; (b) the top view.

Due to the minimum area occupancy requirement, a more likely scenario has a number of crossunders on layer $i-1$ instead of a single crossunder. Our second experiment in this section assumes that there is one *victim* on layer i, two same-layer neighbors of the victim at spacing $s = 1.0$ or $s = \infty$, and twelve crossunders ($u1, \cdots, u12$) on layer $i-1$ (see Figure 4). All wires on layers i and $i-1$ have length 20. The *real* pattern has twelve wires uniformly distributed in a 40×40 plane on layer $i-2$ and a 40×40 ground on layer $i-3$; the wires on layer $i-2$ have length 40. There are two model patterns: the *model1* pattern treats layer $i-2$ as a 40×40 ground, and the *model2* pattern treats layer $i-2$ as free space. We compare the total capacitance $C_{i,i}$ for the victim wire and the coupling $C_{i,u1}, \cdots, C_{i,u12}$ between the victim wire and crossunders $u1, \cdots, u12$. Table 4 shows that

(i) Both model1 and model2 can produce similar values for total capacitance $C_{i,i}$ and couplings $C_{i,l1}$ and $C_{i,r1}$ between the victim and its same-layer neighbors, when compared with the real pattern.

(ii) Model1 is better than model2 when used to solve the coupling between the victim and crossunders. Compared with the real pattern, the largest deviations for $C_{i,u1}, \cdots, C_{i,u12}$ are 10.7% when $s = \infty$, and 14.0% when $s = 1.0$ for model1; corresponding values for model2 are 45% and 72%. Furthermore, for couplings $C_{i,u3}, \cdots, C_{i,u10}$ between the victim and crossunders not at the boundary (see Figure 4), the deviation is at most 4.2% for model1. Since most crossunders in real designs are not at the boundary, the error introduced by model1 is negligible.

(iii) Even when same-layer neighbors have their strongest shielding at minimum spacing $s = 1.0$, the coupling mainly due to crossunders accounts for $1-(621.2+626.0)/1447 = 13.8\%$ of the total capacitance $C_{i,i}$ (more significant percentages are observed for representative $0.50\mu m$ and $0.35\mu m$ geometric parameters). Therefore, coupling between the victim and crossunders must be considered in the capacitance extraction. We conclude that when there is no layer $i+1$ and beyond, layer $i-2$ can be viewed as a ground for computing total capacitances for wires on layer i, or coupling capacitances between wires on layer i and wires on layer $i-1$.

The third experiment of this section considers the impact of wires on layers $i+1$ and beyond. To have a geometric structure that still can be solved by Fastcap[4], we assume one victim on layer i with two same-layer *neighbors* at spacing $s = 1.0$ or ∞, six crossunders on layer $i-1$ and six crossovers on layer $i+1$. All wires on layer i have length 10, and all crossunders/crossovers have length 20. Crossunders/crossovers are uniformly distributed in 20×20 planes such that the area occupancy for layers $i \pm 1$ is 30%. In the *real* pattern, there are six wires distributed in a 20×20 plane on layer $i+2$ or $i-2$. These wires have length 20; layers $i \pm 2$ also have area occupancy of 30%. In the *model* pattern, layers $i \pm 2$ are 20×20 ground planes.

Table 5 reports total capacitance $C_{i,i}$ for the victim, same-layer couplings $C_{i,l1}$ and $C_{i,r1}$ between the victim and its neighbors, crossunder couplings $C_{i,u1}, \cdots, C_{i,u6}$ between the victim and crossunders $u1, \cdots, u6$, and crossover couplings $C_{i,o1}, \cdots, C_{i,o6}$ between the victim and crossovers $o1, \cdots, o6$. The difference between the model pattern and the real pattern is less than 0.5% for $C_{i,i}$, $C_{i,l1}$ and $C_{i,r1}$, and about 5% for crossunder or crossover coupling if the crossunder or crossover is not at the boundary in our pattern. We conclude:

Foundation 3 *During capacitance extraction for wires on layer i, layers $i \pm 2$ can be treated as ground planes with negligible error. There is no need to look beyond layers $i \pm 2$.*

[4] Shorter wires mean that the coupling due to the front and end sidewalls, as well as wire corners, is more significant. Our experiments use wires that are as long as possible, subject to Fastcap being run on a workstation with 400MB RAM.

	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,u7}$	$C_{i,u8}$	$C_{i,u9}$	$C_{i,u10}$	$C_{i,u11}$	$C_{i,u12}$
real	∞	629.5	-	-	16.4	19.89	36.89	50.95	59.62	61.09	60.59	61.47	51.39	32.92	16.78	12.28
model1		629.7	-	-	16.97	20.21	37.47	53.14	60.98	62.8	62.17	62.01	52.24	33.65	17.24	13.69
model2		630.8	-	-	18.56	21.24	37.45	56.19	63.3	65.61	65.58	62.85	54.74	35.73	20.21	17.94
real	1.0	1447	621.2	626	5.632	7.623	13.11	15.34	16.22	16.65	17.06	18.66	16.29	11.27	5.383	4.095
model1		1447	621	626.3	5.567	7.478	13.38	15.8	17.16	17.49	17.99	19.67	17.04	11.69	5.68	4.668
model2		1447	615.2	616.9	6.11	7.347	13.38	19.33	20.67	20.97	21.11	21.17	20.07	14.22	8.294	7.041

Table 4: Total capacitance $C_{i,i}$ of the victim on layer i and couplings between the victim and crossunders on layer $i-1$.

	s	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,u1}$	$C_{i,u2}$	$C_{i,u3}$	$C_{i,u4}$	$C_{i,u5}$	$C_{i,u6}$	$C_{i,o1}$	$C_{i,o2}$	$C_{i,o3}$	$C_{i,o4}$	$C_{i,o5}$	$C_{i,o6}$
real	∞	418.9	-	-	13.51	33.77	52.18	52.26	33.95	13.67	13.93	34.09	52.43	52.35	34.31	14.17
model		418.9	-	-	14.16	34.68	52.54	52.53	34.39	14.26	14.08	34.52	52.67	52.59	34.31	14.15
real	1.0	779.9	310.4	310.4	5.099	11.73	16.09	16.09	11.85	5.03	6.042	13.95	19.46	19.32	13.86	6.135
model		781.6	309.5	308.9	6.663	12.66	17.46	17.34	12.58	6.613	6.679	13.71	18.47	18.31	13.6	6.706

Table 5: Total capacitance $C_{i,i}$ of the victim on layer i, couplings $C_{i,l1}$ and $C_{i,r1}$ between the victim and its same-layer neighbors, and couplings between the victim and crossunders on layer $i-1$ or crossovers on layer $i+1$.

2.4 Coupling between wires on the same layer

To isolate the impact of crossunders and crossovers, we study the following two patterns. The *optimistic* pattern treats layers $i \pm 1$ as ground planes; this emphasizes the shielding effect due to crossunders and crossovers and in general leads to underestimation of couplings between wires on layer i. The *pessimistic* pattern treats layers $i \pm 2$ as ground planes without any wires on layers $i \pm 1$; this removes all shielding effects due to crossunders and crossovers and in general leads to overestimation of couplings between wires on layer i.

We first study the coupling between a victim wire and its non-immediate neighbors. We use a 40×40 ground plane and wires of length 20. Orthogonally with respect to the optimistic and the pessimistic patterns, we again have a *real* pattern and a *model* pattern. The real pattern has five wires on layer i, *l2*, *l1*, *victim*, *r1* and *r2* at spacing $s = 1.0$. The model pattern has only the immediate neighbors (*l1* and *r1*) of the victim. According to Table 6, differences in the total capacitance for the victim between the real pattern and the model pattern are less than 0.2%. The error associated with the model pattern for the coupling between the victim and its immediate neighbors is approximately 3%. Therefore, coupling analysis to wires in the same layer need only consider nearest neighbors.

neighbor widths	1	2	3	4
capacitance $C_{i,i}$	764.5	765.2	764.9	764.4

Table 8: Total capacitances $C_{i,i}$ for the victim in case of different neighbor widths.

We also study interactions between the victim's two neighbors as well as the effect of neighbor widths. We consider only the worst case interaction, given by the pessimistic pattern with wires (victim and two neighbors) on layer i and ground planes on layers $i \pm 2$. We use a 40×40 ground plane and wires of length 10. To observe the interaction between the victim's neighbors, we vary the spacings between the victim and its neighbors, and measure the change in total capacitance of the victim. Let C_{l-r} be the total capacitance of the victim when the left and right neighbors are distance l and r away ($l = \infty$ or $r = \infty$ indicates no left or right neighbor). Simulation and derived results are given in Table 7. The *derived* values are based on formula $C_{l-r} = (C_{l-l} + C_{r-r})/2$. Since differences between the simulated and derived values are often less than 1.0%, we see that couplings on opposite sides can be considered independently. To assess the effect of neighbor widths, we assume that the victim has a fixed width of 1.0, and that two neighbors (at spacing 1.0) have identical widths. We vary the widths of the neighbors and observe the change in total capacitance of the victim (see Table 8). Since the maximum variation is less than 0.2%, widths of neighbors can be ignored. We summarize the experiments of this section by:

Foundation 4 *Coupling analysis to wires in the same layer need only consider nearest neighbors independently, with the widths of same-layer neighbor wires having negligible effect on the coupling.*

2.5 Coupling between wires on layer i and wires on layers $i \pm 1$

To study the interaction between crossunder coupling and the crossover coupling, we first observe the impact of the crossover coupling on the crossunder coupling. We assume that layer i has twelve wires $i1, \cdots, i12$, i.e., area occupancy of 30%, and that layer $i-1$ has one wire (*crossunder*) and same-layer neighbors at spacings $s = 1.0, \infty$. We solve one pattern which treats layer $i+1$ as a ground plane (*full crossing)*, which models the greatest possible effect due to crossovers, and a second pattern which treats layer $i+2$ as a ground plane without any wires on layers $i+1$ (*no crossing*), which models no effect due to crossovers. Again, we use a 40×40 ground plane and wires of length 20.

We compute the crossunder coupling between wires on layer i and the central wire on layer $i-1$ (see Table 9). The difference between the two extreme cases is less than 6% (excluding cases at the boundary). Recall that the total crossunder and crossover coupling accounts for about one third of total capacitance for a victim; hence, the crossunder coupling can be computed independently without considering crossovers while introducing an error of at most 2% for the victim's total capacitance. Due to the symmetry between crossunders and crossovers, we have:

Foundation 5 *The joint interaction of layers $i-1$ and $i+1$ on layer i is negligible; therefore, corrections for orthogonal crossovers and crossunders can be performed independently.*

3 A 2 1/2-D Methodology

The above foundations justify a simplified yet accurate 2 1/2-D extraction methodology. In this section, we first present methods to generate capacitance coefficients by one-time use of 3-D simulation on predetermined patterns, and then discuss the computation of lumped capacitances for nets in real designs based on these capacitance coefficients.

pattern	real					model		
	$C_{i,i}$	$C_{i,l2}$	$C_{i,l1}$	$C_{i,r1}$	$C_{i,r2}$	$C_{i,i}$	$C_{i,l1}$	$C_{i,r1}$
optimistic	1451	32.04	602.2	602.1	31.67	1449	602.2	619.9
pessimistic	1436	54.9	616.6	616.5	54.86	1436	639.8	639.6

Table 6: Total capacitance $C_{i,i}$ of the victim wire on layer i and couplings $C_{i,l2}, C_{i,l1}, C_{i,r1}$ and $C_{i,r2}$ between the victim wire and its neighbors ($l2, l1, r1$ and $r2$).

spacing	1-1	1-2	1-3	1-4	1-∞	2-2	2-3	2-4	2-∞	3-3	3-4	3-∞	4-4	4-∞	∞-∞
simulated	764.5	639.2	600.0	582.5	559.7	511.5	471.0	452.8	430.3	429.7	411.0	387.7	393.3	368.1	341.7
derived	-	638.0	597.1	578.9	553.1	-	470.6	452.4	426.6	-	411.5	385.7	-	367.5	-

Table 7: Simulated and derived total capacitances of the victim in cases of different neighbor spacing.

3.1 Capacitance coefficient generation

We assume (i) the substrate is a ground plane for layer i only if $i = 1$ or $i = 2$; and (ii) each of layer $i+2$ and layer $i-2$, if it exists, is a ground plane (resp. the *top* and *bottom* ground planes) so that no couplings to layers beyond them need be considered. In addition, we assume all wires have length l.

To extract lateral, area and fringe capacitances, we use a pattern which, in addition to grounds, has the *victim* and its immediate *neighbors* on layer i, but no wires on layer $i \pm 1$. Let total capacitance for the victim be C_{self}, and let coupling to its neighbors be C_{l1} and C_{r1}. The *lateral capacitance coefficient*, which captures the per-length and per-side coupling between the victim and its neighbor, is given by

$$C_l = (C_{l1} + C_{r1})/(2 \cdot l) \quad (1)$$

The remainder $C_{self} - (C_{l1} + C_{r1})$ is assumed to be the area and fringe capacitances for the victim. We run the same simulation with another width w' for the victim, and obtain C'_{self}, C'_{l1} and C'_{r1}. Clearly,

$$\begin{aligned} C_{self} - (C_{l1} + C_{r1}) &= 2 \cdot l \cdot C_a + 2 \cdot (l + w) \cdot C_f, \quad (2) \\ C'_{self} - (C'_{l1} + C'_{r1}) &= 2 \cdot l \cdot C_a + 2 \cdot (l + w') \cdot C_f, \quad (3) \end{aligned}$$

where C_a is the *area capacitance coefficient* (i.e., per-length and per-side coupling between grounds and the top/bottom sides of the victim), and C_f is the *fringe capacitance coefficient* (i.e., per-length and per-side coupling between grounds and sidewalls of the victim). Both can be computed by solving Equations (2) and (3) simultaneously. Overall, tables are computed for C_l, C_a and C_f for different wire widths w and spacings s.

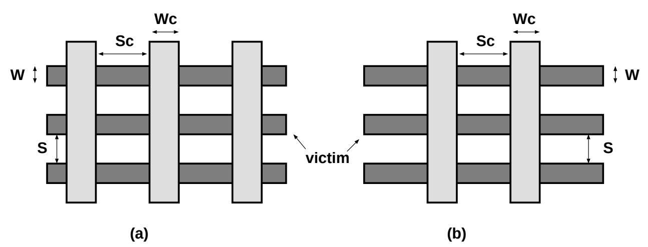

Figure 5: The geometric structure on layers i and $i+1$ for generating crossover correction capacitances.

According to Foundation 5, couplings due to crossover and crossunder can be generated independently. We solve the two patterns in Figure 5 to obtain the coupling between the victim and a crossover. In addition to grounds, the pattern in Figure 5(a) has three wires on layer i and three wires on layer $i+1$. Wires on layer i have width w and spacing s. Crossovers on layer $i+1$ have width w_c and spacing s_c. The only difference between Figures 5(a) and (b) is that the latter has just two wires on layer $i+1$. We first compute the total capacitance C_{self} for the central (victim) wire on layer i in Figure 5(a), and total capacitance C'_{self} for the victim in Figure 5(b), then define the (per-side) *crossover correction capacitance* C_{over} as

$$C_{over} = (C_{self} - C'_{self})/2. \quad (4)$$

The (per-side) *crossunder correction capacitance* C_{under} can be generated similarly. Since the crossover and crossunder coupling depends on w, s, w_c and s_c(see Figure 5), tables are computed for C_{over} and C_{under} for different values of w, s, w_c and s_c.

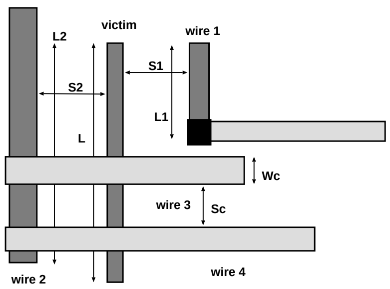

Figure 6: An example for 2 1/2-D capacitance analysis.

3.2 Algorithm for 2 1/2-D capacitance extraction

A typical situation that can occur in IC designs is shown in Figure 6. The *victim* wire on layer i is being analyzed. *Wire1* and *wire2* are same-layer neighbors and *wire3* and *wire4* are crossovers. We first obtain geometric parameters from the layout database, including width w for the victim, *effective* lengths[5] and spacings, (l_1, s_1) and (l_2, s_2), for neighbors wire1 and wire2, and the width and spacing (w_c, s_c) for every crossover and crossunder (only those for *wire3* are shown in the Figure). We then calculate the total capacitance for the victim according to the algorithm given in Table 10, where *look_up_range* is the minimum spacing between the victim and its neighbor

[5] The effective length of a victim's neighbor is the length of the parallel run between them.

spacing	crossover	$C_{i1,2}$	$C_{i2,2}$	$C_{i3,2}$	$C_{i4,2}$	$C_{i5,2}$	$C_{i6,2}$	$C_{i7,2}$	$C_{i8,2}$	$C_{i9,2}$	$C_{i10,2}$	$C_{i11,2}$	$C_{i12,2}$
1.0	full	6.31	4.798	8.827	11.2	11.77	11.45	11.14	11.91	11.99	11.55	9.545	7.137
	no	5.946	4.902	8.576	11.5	12.35	12.25	12.09	12.91	12.91	12.27	9.935	7.334
∞	full	10.55	9.758	20.69	31.18	35.66	36.87	36.7	37.35	36.81	34.81	28.44	17.32
	no	10.79	9.705	21.27	31.55	36.01	37.2	36.99	37.58	36.99	35.07	28.75	17.4

Table 9: Crossunder couplings between wires $i1, \cdots, i12$ on layer i and the crossunder on layer $i-1$ with its same-layer neighbors at spacing 1.0 and ∞, for both full and no crossover.

when the coupling between them is negligible. Linear interpolation is used to compute values between different widths in look-up tables, and linear interpolation on $1/spacing$ is used to compute values between different spacings. Furthermore, linear extrapolation is used for widths and spacings that exceed values in look-up tables. More sophisticated formulas presented in [5, 1] can be used here. But layouts in gate-array and standard-cell often exhibit a limited set of widths and spacings. Therefore, look-up tables with reasonable size can suffice, along with limited use of interpolation and extrapolation.

```
For any given victim wire segment of width w and length l
  Let the lumped capacitance for the victim be C_self = 0
  For each side of length l
    Find out all the same-layer neighbors within look_up_range
    Let their effective lengths be l_i and spacing s_i
    For each neighbor
      Lookup C_l, C_a and C_f by s_i and w
      C_self = C_self + (C_l + C_a + C_f) · l_i
    For any crossover of width w_c
      Get the next crossover and determine spacing s_c
      Lookup C_over by w, s_i, w_c, s_c
      C_self = C_self + C_over
    For any crossunder of width w_c
      Get the next crossunder and determine spacing s_c
      Lookup C_under by w, s_i, w_c, s_c
      C_self = C_self + C_under
  For each side of width w
    Find out all the same-layer neighbors within look_up_range
    Let their effective lengths be l_i and spacing s_i
    For each neighbor
      Lookup C_l and C_f by s_i and w
      C_self = C_self + (C_l + C_f) · l_i
```

Table 10: Algorithm for 2 1/2-D capacitance extraction.

3.3 Experience with the 2 1/2-D extraction methodology

Two nets were extracted from real designs and their lumped capacitances were computed based on the 2 1/2-D methodology. We also separated the two nets into a number of small sections and used a 3-D simulator to solve all the relevant geometries for these sections. Capacitances from different sections were then summed. Table 11 compares results from the two methods; errors were 0.54% for the smaller net and 3.33% for the larger one. Our method has separately been validated in cooperation with the Motorola RISC Division, Semicustom Operation by comparing extracted and measured capacitances.

4 Conclusions

We have validated five "foundations" that allow simplification of the capacitance extraction problem for multilayer interconnects. We have also described a simple yet accurate 2 1/2-D extraction methodology, now implemented in a commercial cell-based layout tool. We showed that this methodology gives results that are very close (within a few percent) to measured silicon and 3-D numerical simulation. Typical extraction and performance verification flows often ignore one or more factors such as process variations, thermal gradients, errors in device and cell characterization, foundry insertion of dummy metal, etc. Since these errors can swamp our several percent error versus 3-D simulation, we conclude that the proposed 2 1/2-D methodology is sufficient for layout optimization. Our ongoing research and development seeks a more holistic integration of synthesis and analysis activities within a framework for constraint-driven design.

	2 1/2-D analysis	3-D simulation	error
smaller net	6.53552	6.5713	-0.54%
larger net	3152.42	3261.17	-3.33%

Table 11: Comparison between 2 1/2-D analysis and 3-D simulation.

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