Multilevel Circuit Partitioning

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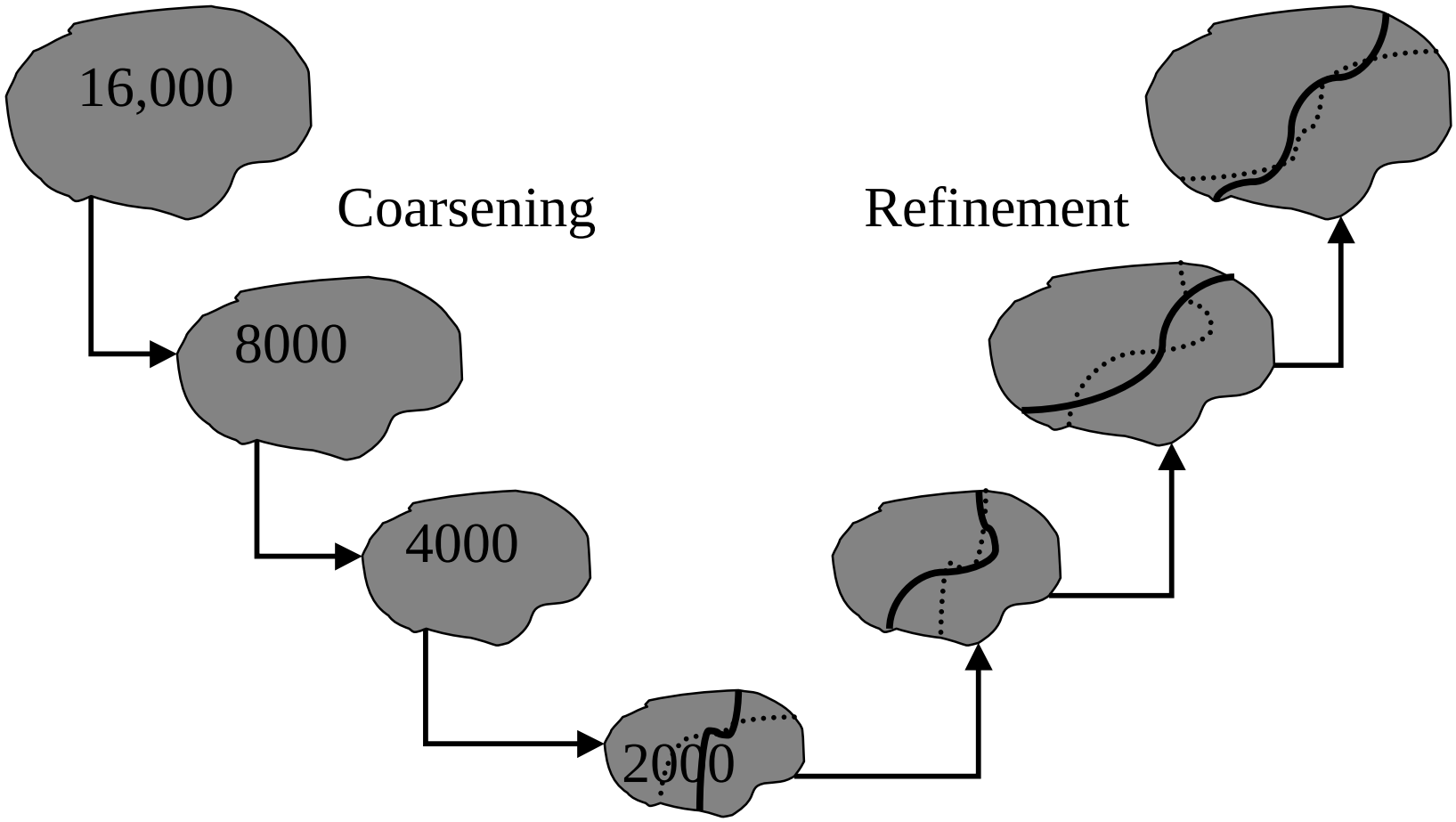
Talk Outline

- Multilevel partitioning paradigm
- Previous work
- Our innovations
- Experimental results
- The future of pure partitioning

The Multilevel Approach



You Must Have Multilevel

- Extremely efficient
- More chances to climb out of local minima
- Superior solution quality
- Flexible objectives
- Scales with circuit size

Prediction: multilevel approaches will become the industry standard

Previous Work

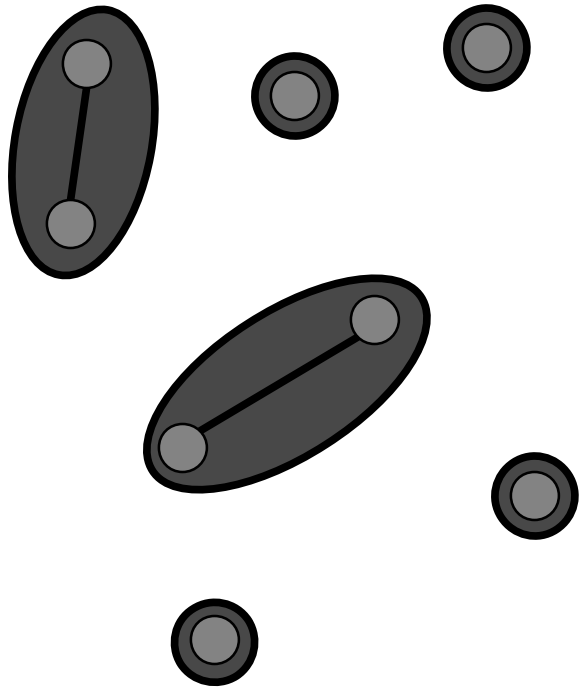
- Scientific Computing
  - Chaco (Hendrickson and Leland, 1993)
  - Metis (Karypis and Kumar, 1995)
- VLSI CAD
  - Cong and Smith, 1993
  - Hauck and Borriello, 1995
  - GMetis (Alpert and Kahng, 1996)
  - hMetis (Karypis and Kumar, 1997)

Our Contributions

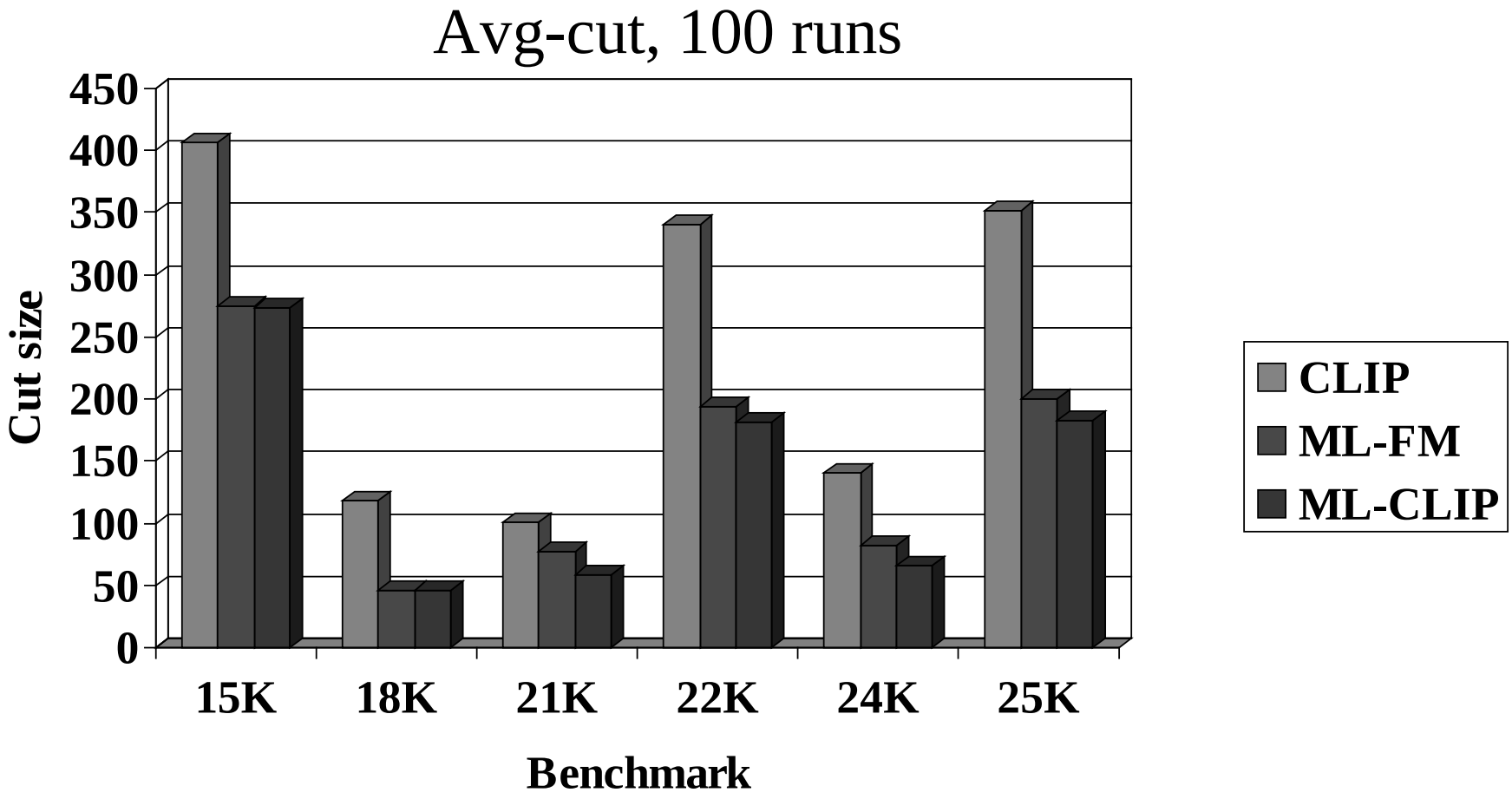
- Flexible matching-based coarsening
  - Creates more levels
  - Matching ratio M (1.0, 0.5, 0.33)
- CLIP-FM refinement engine
  - Interchangeable with FM
  - 18% improvement (Dutt/Deng)

Matching-based Coarsening

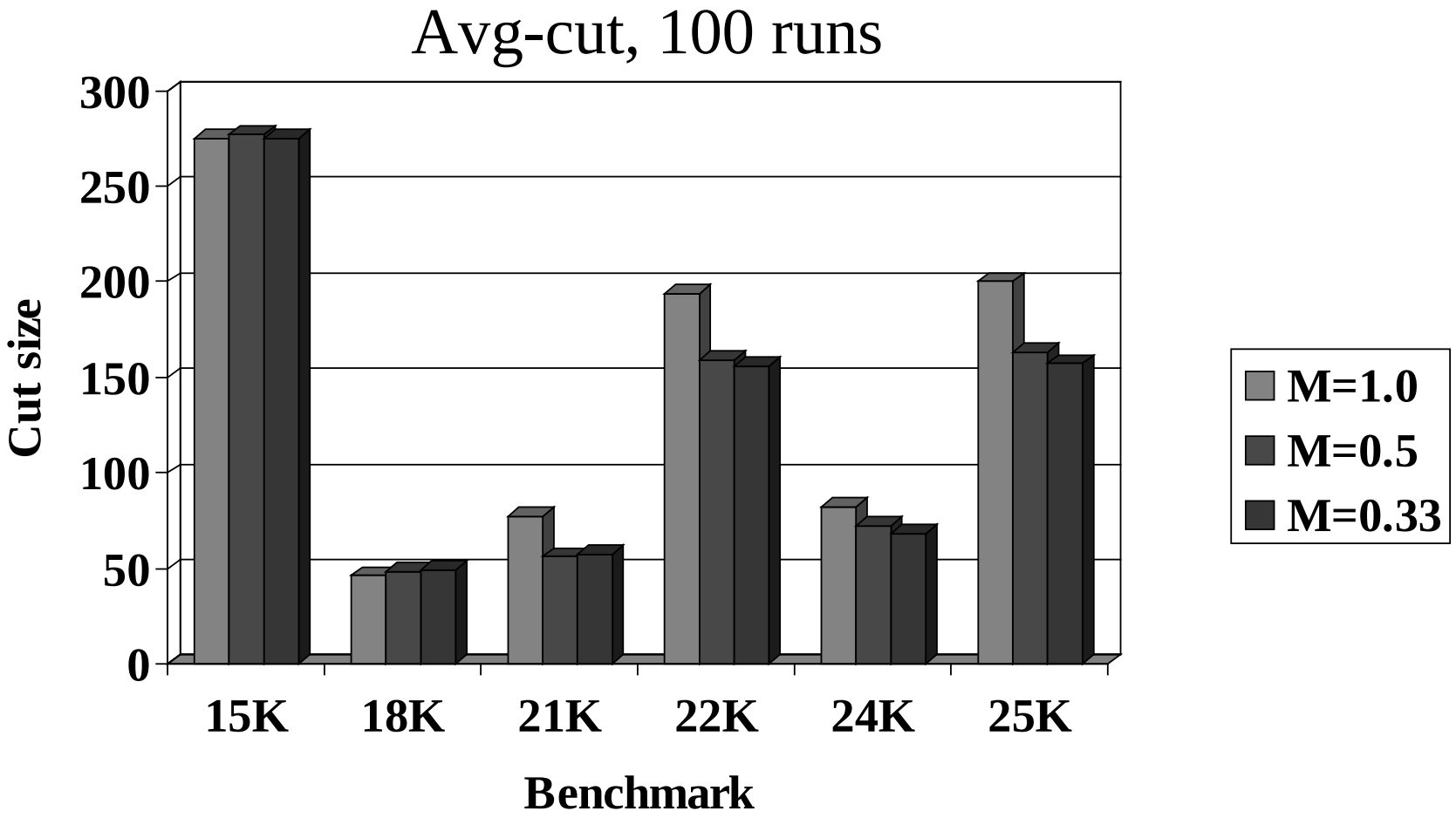
- Randomly sort vertices
- Try to match current vertex to best vertex
- Stop when number of matched vertices < M|V|



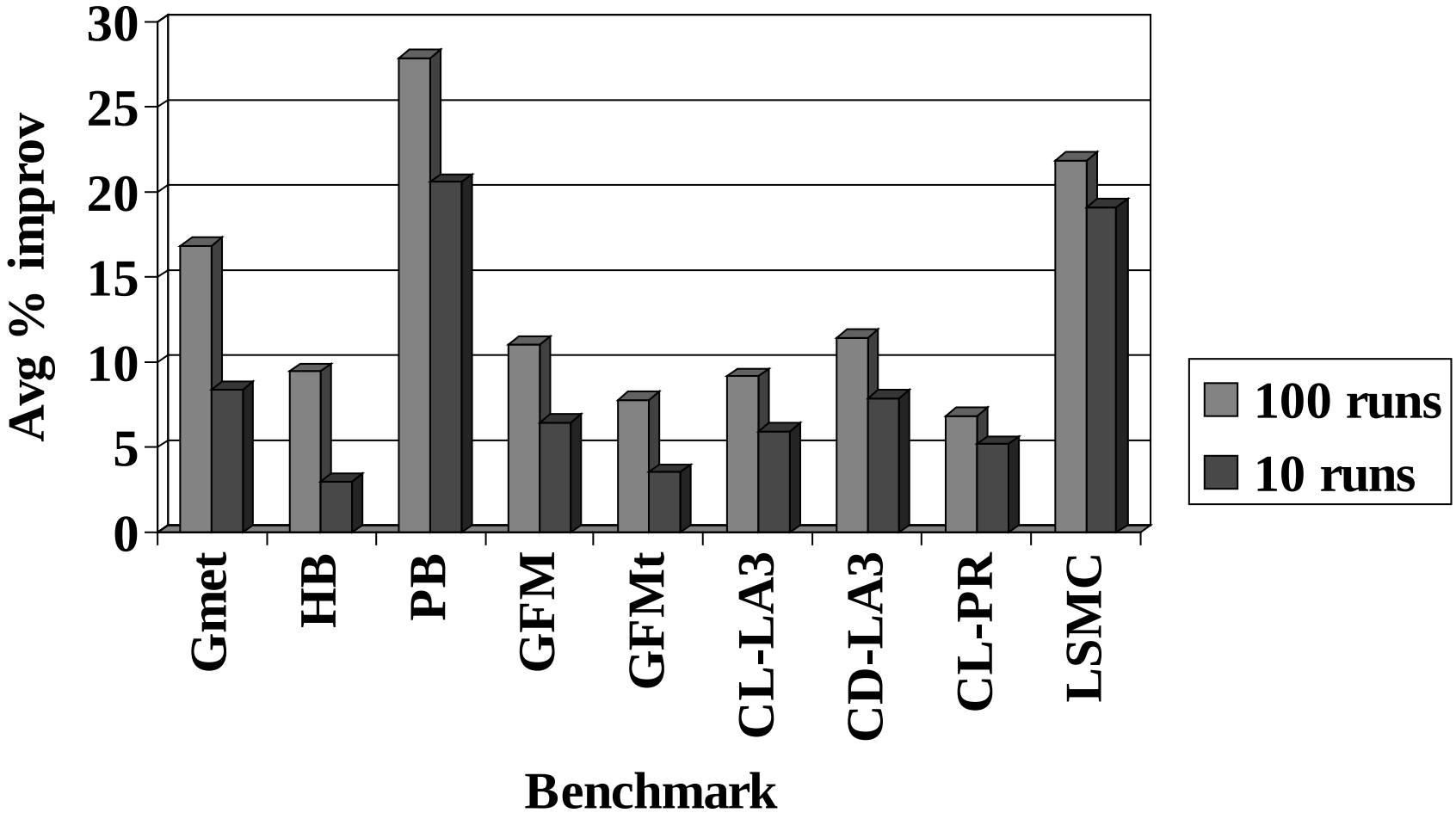
Experiments: ML vs CLIP



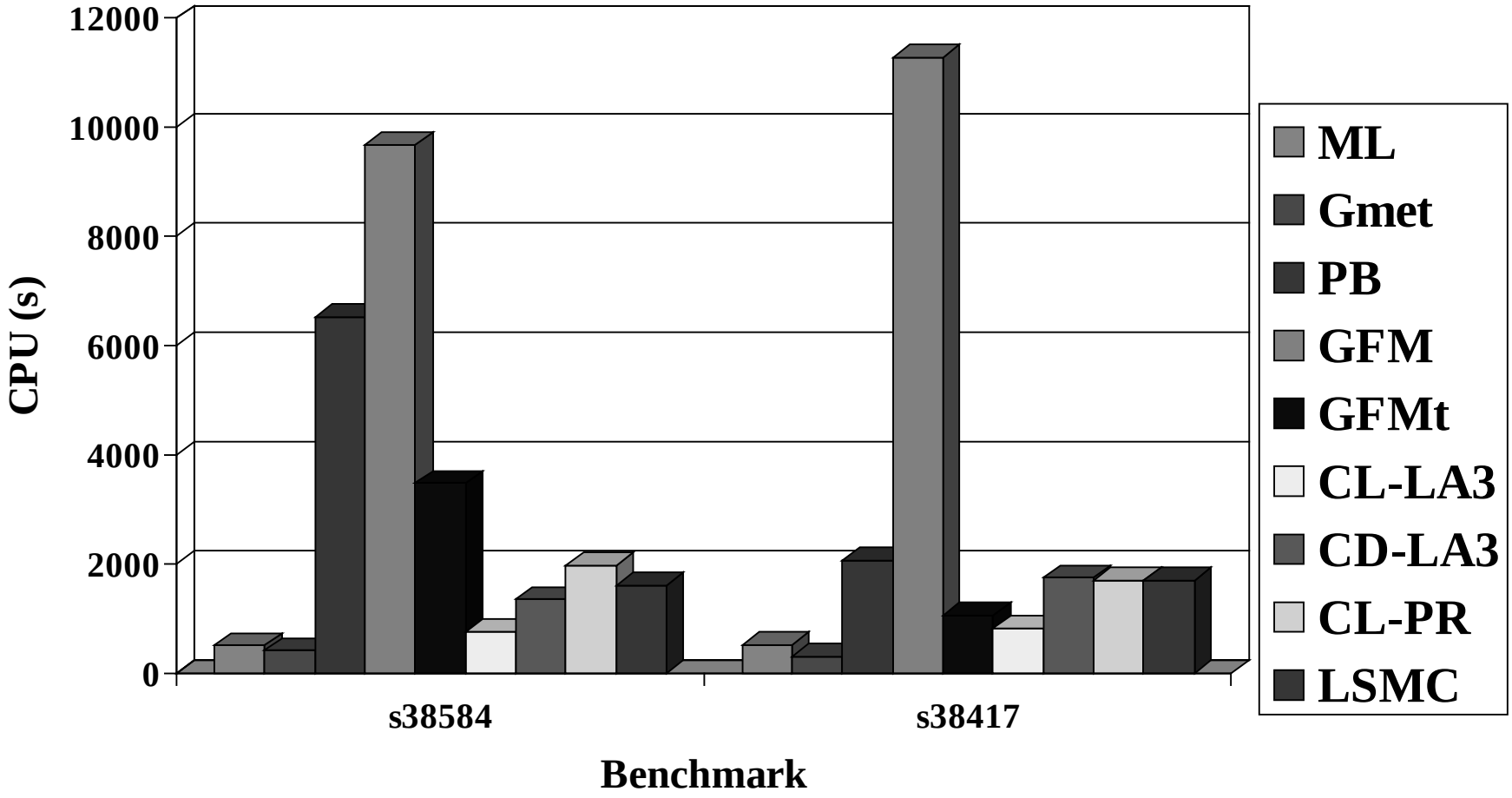
Experiments: Matching ratio M



ML-CLIP (0.5) vs Other Methods



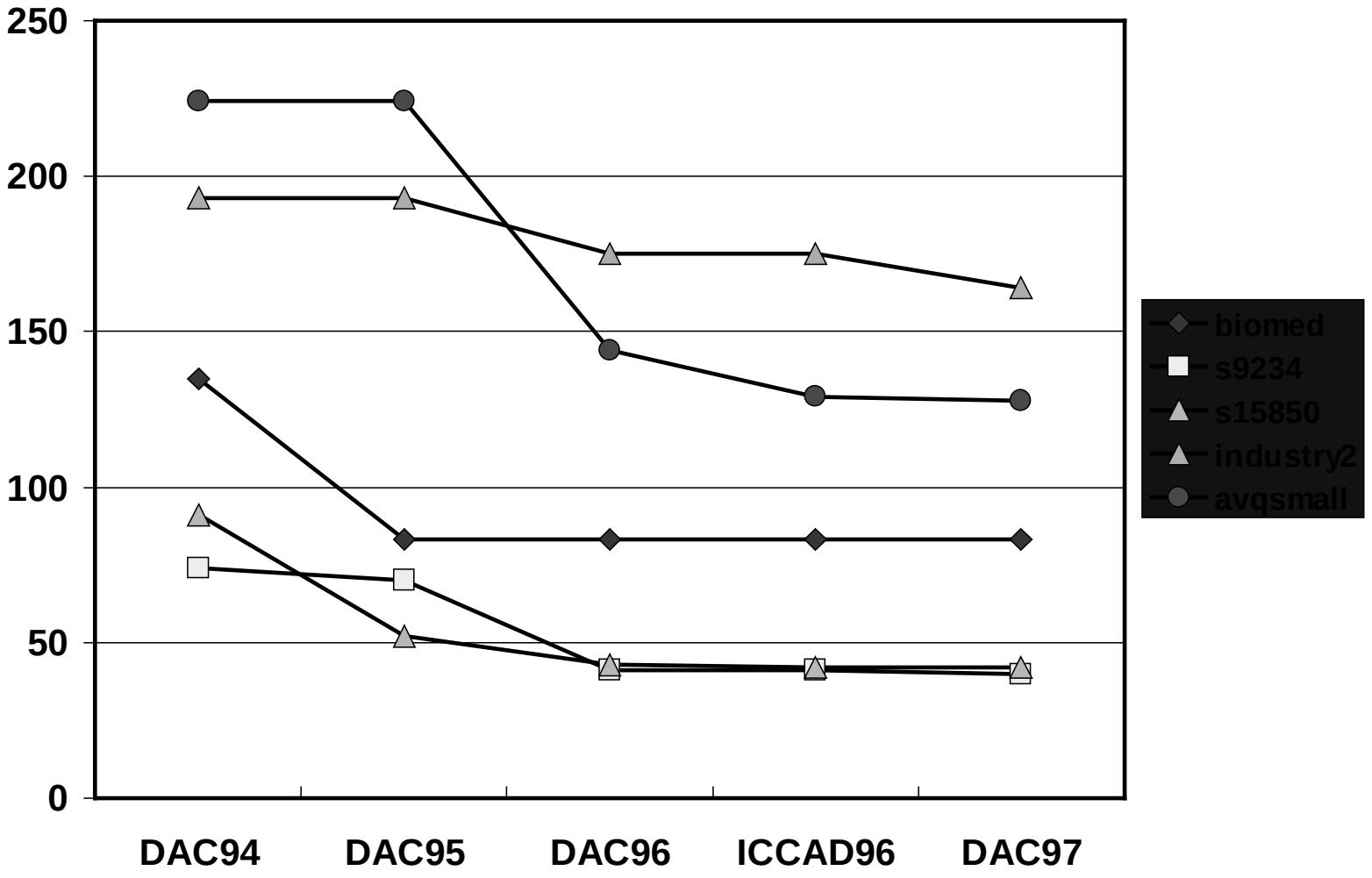
CPU Comparisons



Conclusions

- New matching scheme
- Use of CLIP inside partitioner
- Excellent solution quality
- Good CPU times
- Effective quadrisection-based placement
- Any multilevel approach will be effective

Is pure partitioning a solved problem?



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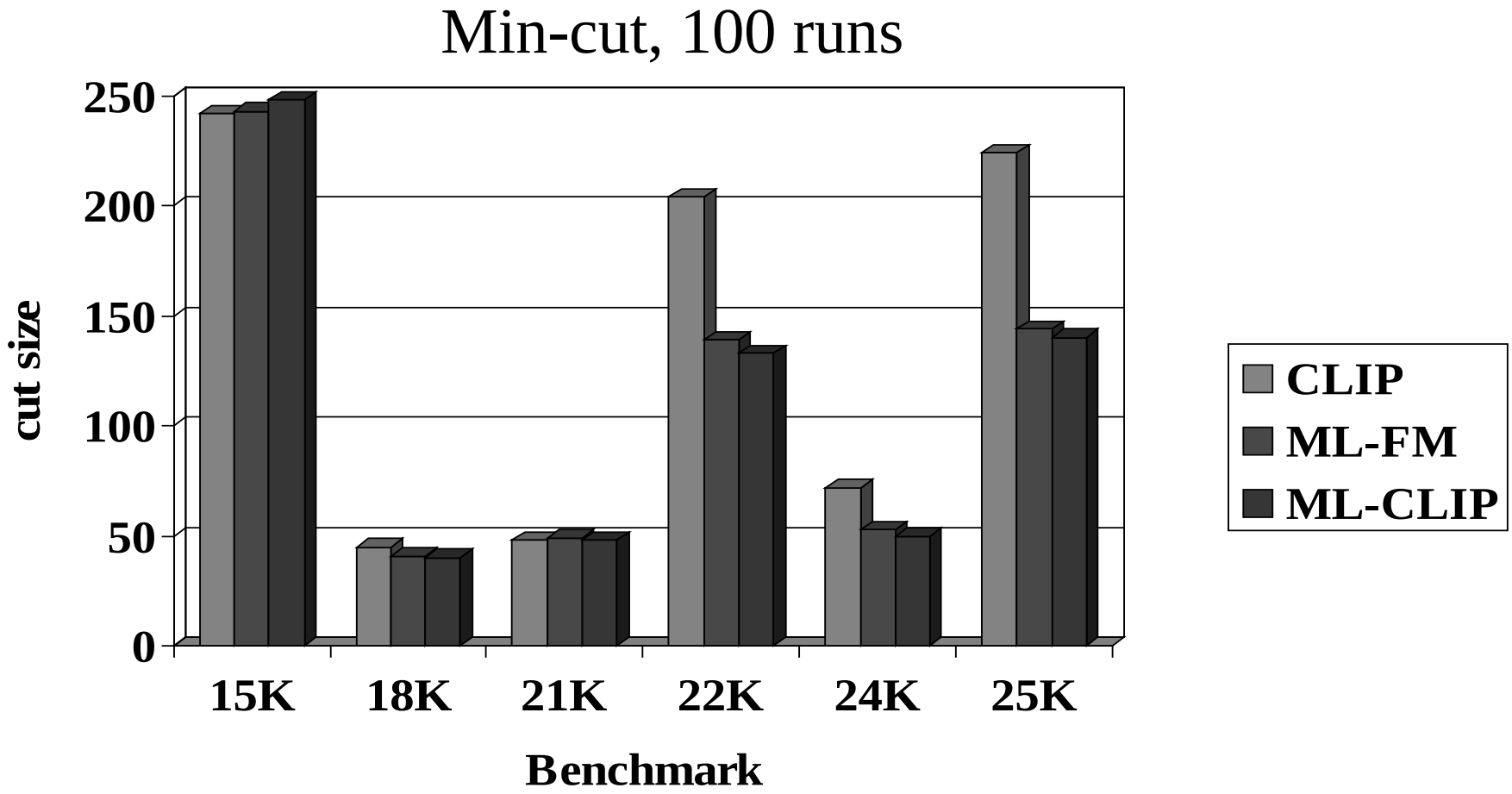
Experiments: ML vs CLIP