Delay Models for MCM Interconnects When Response is Non-monotone*

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Abstract

Elmore delay has been extensively used for interconnect delay estimation because its simplicity of evaluation makes it appropriate for layout design. However, since Elmore delay does not take into account the effect of inductance, the discrepancy between actual delay and Elmore delay becomes significant for long RLC transmission lines, such as for MCM and PCB interconnects. We describe a simple two-pole based analytic delay model that estimates arbitrary threshold delays for RLC lines when the response is non-monotone; our model is far more accurate than the Elmore model. We also describe an application of our model for controlling response undershoot/overshoot and for the reduction of interconnect delay through constraints on the moments.

1 Introduction

Recently, accurate estimation of interconnect threshold delays and rise times has become essential to the design of high-speed systems. Many interconnect delay models have been advocated; these are classified roughly into simulation based models and closed form analytical models. Simulation methods such as SPICE give the most accurate insight into arbitrary interconnect structures, but are computationally expensive. Faster methods based on moment matching techniques are proposed in [13, 14, 15, 17], but are still too expensive to be used during layout optimization. Thus, Elmore delay [2], a first order analytical approximation of delay under step input, has been the most widely used model for performance-driven layout synthesis.

Recently, a number of analytical delay formulas have been proposed for interconnect delay based on the first few moments of the response under step and ramp input [5, 4, 10, 11, 18]. The authors of [5] use Elmore delay as an upper bound for the 50% threshold delay for RC interconnection lines under arbitrary input waveforms. The work of [4] gives lower and upper bounds for the ramp input response; their (single-pole) delay model for 50% threshold voltage can be obtained by applying the Elmore definition to the ramp input response. Our own previous work has presented analytical delay models for monotone response under step and ramp inputs, based on first and second moments [10, 11]. Quite recently, [18] have used the first three moments to accurately compute two poles of the impulse response. Note that all of these approaches assume that the response is monotone (or overdamped) in deriving their respective delay models. However, for long lines with sufficient inductive impedance the response will be non-monotone.

For RLC lines, which are the necessary representation of interconnects whose inductive impedance cannot be neglected [8], Elmore and other first-order delay models cannot accurately estimate signal delay because they are independent of inductance. To illustrate the effect of inductive impedance on the response, we consider a 2-port model for an interconnect driven by a step input with finite source impedance. Figure 1 compares the RC and RLC line responses computed by SPICE3e: 90% threshold delay is 288 ps for the RLC model, but is 358 ps for the RC model. Elmore delay, which does not depend on line inductance, will yield the same delay estimate of 386 ps for both the RC and the RLC cases. This inaccuracy can be harmful for current performance-driven routing methods which try to optimize interconnect segment lengths and widths (as well as drivers and buffers).

A non-monotone (i.e., underdamped) voltage response oscillates before settling to a steady state value. Such a response occurs when the ratio of inductive impedance to resistance exceeds a certain threshold in an interconnect line. MCM substrate interconnects have smaller driver resistance, and inductive impedance greater than resistive impedance as a consequence of greater widths and lengths compared to their on-chip VLSI counterparts; the voltage response for such interconnects tends to be nonmonotone. Consequently, the effect of inductance is more evident in MCM interconnects. To address the deficiencies of the Elmore model, this paper gives a simple, yet reasonably accurate, *analytical* delay model for interconnect lines which are inductive (i.e., RLC transmission lines) and whose voltage response is not monotonically increasing. Our proposed model can estimate signal delay for non-monotone response at arbitrary threshold voltages. Recently, [10] proposed a similar set of analytical delay models, but these are restricted to the case of a monotone voltage response. Preliminary experimental results show that our delay estimates are within 27% of SPICE-computed delays (for most cases within 15%), while Elmore delay estimates can differ by as much as 100% from the SPICE-computed delays. We also briefly

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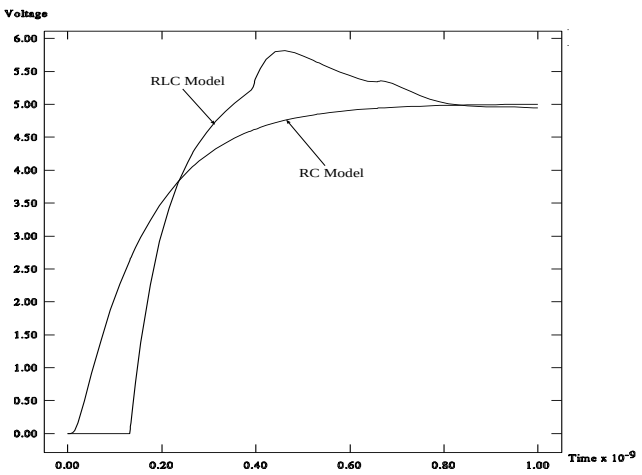

Figure 1: Comparison of HSPICE responses at the end of an interconnect line driven by a step input and terminated with a capacitive load, with the line represented using both RC and RLC 2-port models. The 90% threshold delay is 288 ps for the RLC model, and 358 ps for the RC model. The driver resistance is 10.0 Ω and the load capacitance at the end of the line is 2.0 pF. The line parameters are $r = 0.075\ \Omega/\mu m$, $l = 0.123\ pH/\mu m$, $c = 8.8\ fF/\mu m$; the length of the line is 400 μm.

discuss an approach to reduce the threshold delay by controlling the overshoot of the voltage response. This translates into a condition between the first and second moments of the interconnect transfer function, which are functions of driver and interconnect parameters.

The remainder of this paper is organized as follows. Section 2 describes delay computation using our new model. Section 3 explains minimization of delay by allowing small ringing. Section 4 gives experimental results, and Section 5 states our conclusions.

2 New Delay Model for Interconnects

For simplicity, we consider a single interconnect line in studying response and delay models. We develop our delay model as a function of first and second moments (or coefficients) of the transfer function; note that the same delay model can be applied to the corresponding moment values of arbitrary interconnect trees. The denominator of the transfer function of a single RLC interconnect line with source and load impedance (Figure 2) is obtained from ABCD parameters [1] as

$$\begin{aligned} H(s) &= \frac{1}{\left[(1+\frac{Z_S}{Z_T})\cosh(\theta h) + (\frac{Z_S}{Z_0}+\frac{Z_0}{Z_T})\sinh(\theta h)\right]} \\ &= \frac{1}{1+b_1 s+b_2 s^2+\ldots+b_k s^k+\ldots} \end{aligned} \quad (1)$$

where $\theta = \sqrt{(r+sl)sc}$ is the propagation constant and $Z_0 = \sqrt{\frac{R+sL}{sC}}$ is the characteristic impedance; $r = \frac{R}{h}, l = \frac{L}{h}, c = \frac{C}{h}$ are resistance, inductance, and capacitance per unit length and h is the length of the line. The variables b_k are called the coefficients of the transfer function and are directly related to the moments of the transfer function [10]. Expanding the transfer function into a Maclaurin series of s around $s = 0$ leads to an infinite series, and to compute the response the series is truncated to desired order. We model the source as a resistance R_S and the load as capacitance C_L. For a two-pole model the transfer function is approximated as

$$H(s) \approx \frac{1}{1+b_1 s+b_2 s^2}$$

with coefficients

$$\begin{aligned} b_1 &= R_S C + R_S C_L + \frac{RC}{2} + RC_L \\ b_2 &= \frac{R_S RC^2}{6} + \frac{R_S RCC_L}{2} + \frac{(RC)^2}{24} + \frac{R^2 CC_L}{6} \\ &\quad + \frac{LC}{2} + LC_L \end{aligned} \quad (2)$$

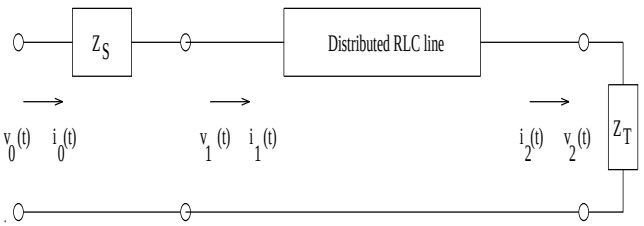

Figure 2: 2-port model of a distributed RLC line with source impedance Z_S and load impedance Z_T.

When the input at the source is modeled as a step waveform, the output response in the transform domain is $V_{out}(s) = \frac{V_0}{s}H(s)$. The corresponding time domain response using the two-pole model is

$$v(t) = V_0\left(1 - \frac{s_2}{s_2-s_1}e^{s_1 t} + \frac{s_1}{s_2-s_1}e^{s_2 t}\right) \quad (3)$$

where $s_{1,2} = \frac{-b_1 \pm \sqrt{b_1^2-4b_2}}{2b_2}$.

The condition for the response to be non-monotone is for the poles to be complex, i.e., $b_1^2 - 4b_2 \leq 0$ (as noted earlier, this corresponds to the inductive impedance exceeding a certain value). By writing the poles as $s_{1,2} = -\alpha \pm \jmath\beta$, the non-monotone time domain response becomes

$$v(t) = V_0\left[1 - \frac{\sqrt{\alpha^2+\beta^2}}{\beta}e^{-\alpha t} * sin(\beta t + \rho)\right] \quad (4)$$

where $\alpha = \frac{b_1}{2b_2}$; $\beta = \frac{\sqrt{4b_2-b_1^2}}{2b_2}$; $\rho = tan^{-1}(\frac{\beta}{\alpha})$.

Notice that the response first reaches the saturation voltage V_0 at time $t = \frac{\pi-\rho}{\beta}$; over the interval $t \in [0, \frac{\pi-\rho}{\beta}]$ the derivative of the response $v'(t)$ is positive, i.e., the response is a continuous non-decreasing function of t. We wish to compute the threshold delay when the response

first crosses some given threshold voltage, e.g., at which the logic state changes. Thus, we can assume that the threshold delay is bounded by the range $[0, \frac{\pi-\rho}{\beta}]$. (The approach we give for approximating response over a specified range is quite general, in the sense that it can be used to compute threshold delay for the response within any range of interest.) We can further reduce the upper bound of the range as follows. Rearranging (3) for a given threshold voltage v_{th} with corresponding delay time t_{th} (in other words, $v_{th} = \frac{v(t_{th})}{V_0}$), we have

$$e^{\alpha t_{th}} = \frac{\sqrt{\alpha^2+\beta^2} sin(\beta t_{th} + \rho)}{\beta(1 - v_{th})}$$

Since $e^{\alpha t_{th}} \geq 1$,

$$\begin{aligned} sin(\beta t_{th} + \rho) &\geq \frac{\beta(1 - v_{th})}{\sqrt{\alpha^2+\beta^2}} \\ t_{th} &\leq \frac{\pi - \rho}{\beta} - \frac{1}{\beta} sin^{-1}(\frac{\beta(1 - v_{th})}{\sqrt{\alpha^2+\beta^2}}) \end{aligned}$$

Using a new time variable τ that shifts the time t_{th} as $\tau = t_{th} + \rho/\beta$, we obtain the bound on τ

$$\rho/\beta \leq \tau \leq (\pi - \xi)/\beta$$

where $\xi = sin^{-1}(\frac{\beta(1-v_{th})}{\sqrt{\alpha^2+\beta^2}})$. Rewriting t by using τ and rearranging (4) yields

$$e^{-\alpha\tau} * sin(\beta\tau) + \frac{\beta}{\sqrt{\alpha^2+\beta^2}} exp(-\frac{\alpha\rho}{\beta})(v_{th} - 1) = 0 \quad (5)$$

The delay at a given threshold voltage v_{th} cannot be calculated directly from this equation, so we adopt the approach of approximating $e^{-\alpha\tau} * sin(\beta\tau)$ with a degree-two polynomial [7]. Specifically, we approximate $f(t_{th}) = exp(-\alpha t_{th}) sin(\beta t_{th})$ over the interval $E = [LB, UB]$ using a vector space representation, where

$$\begin{aligned} UB &\stackrel{\text{def}}{=} \text{upper bound of the approximation interval} \\ LB &\stackrel{\text{def}}{=} \text{lower bound of the approximation interval} \end{aligned}$$

The Gramm-Schmidt technique [7] yields the following approximation of $e^{-\alpha\tau} * sin(\beta\tau)$ over an interval [LB, UB] by a degree-two polynomial (see [12] for details).

$$a_1\tau^2 + a_2\tau + a_3 = 0 \quad (6)$$

where

$$\begin{aligned} a_1 &= \frac{8}{7(UB-LB)^2}(2c_1 - c_2 - 2c_3 - c_4 + 2c_5) \\ a_2 &= \frac{1}{35(UB-LB)^2}[UB(-108c_1 + 26c_2 + 80c_3 + 54c_4 \\ &\quad -52c_5) + LB(-52c_1 + 54c_2 + 80c_3 + 26c_4 - 108c_5)] \\ a_3 &= \frac{1}{35(UB-LB)^2}[UB^2(31c_1 + 9c_2 - 3c_3 - 5c_4 + 3c_5) \\ &\quad +UBLB(46c_1 - 44c_2 - 74c_3 - 44c_4 + 46c_5) \\ &\quad +LB^2(3c_1 - 5c_2 - 3c_3 + 9c_4 + 31c_5)] \\ &\quad +\frac{\beta}{\sqrt{\alpha^2+\beta^2}} exp(-\frac{\alpha\rho}{\beta})(v_{th} - 1) \\ c_1 &= exp(-\alpha LB) sin(\beta LB) \\ c_2 &= exp\left(-\frac{\alpha(UB+3LB)}{4}\right) sin\left(\frac{\beta(UB+3LB)}{4}\right) \\ c_3 &= exp\left(-\frac{\alpha(UB+LB)}{2}\right) sin\left(\frac{\beta(UB+LB)}{2}\right) \\ c_4 &= exp\left(-\frac{\alpha(3UB+LB)}{4}\right) sin\left(\frac{\beta(3UB+LB)}{4}\right) \\ c_5 &= exp(-\alpha UB) sin(\beta UB) \end{aligned}$$

Solving (6) with respect to τ and subtracting ρ/β from τ yields the threshold delay time

$$t_{th} = \frac{-a_2 - \sqrt{a_2^2 - 4a_1a_3'}}{2a_1} - \rho/\beta \quad (7)$$

Note that the two-pole approximation assumes that the response at the load end of the line begins from $t = 0$. However, for interconnects where time of flight, $T_f = \sqrt{LC}$, is non-negligible, the response remains zero until $t = T_f$. Hence, we estimate a given threshold delay as the maximum of time of flight and the delay estimate from (7), i.e., $max[T_f, t_{th}]$. We can estimate the risetime between two threshold voltages as the difference of the respective threshold delay estimates.

Finally, because the range $\tau \in [\frac{\rho}{\beta}, \frac{(\pi-\rho-\xi)}{\beta}]$ may be too large for the Gramm-Schmidt procedure to effectively approximate the response with a single degree-two polynomial. Hence, we divide this range in two to improve the approximation of the response function $e^{-\alpha\tau} * sin(\beta\tau)$. Since $sin(\beta\tau)$ is increasing in the range $[0, \frac{\pi}{2\beta}]$, we divide the original range into the two ranges $[LB1, UB1] = [\frac{\rho}{\beta}, \frac{\pi}{2\beta}]$ and $[LB2, UB2] = [\frac{\pi}{2\beta}, \frac{(\pi-\xi)}{\beta}]$. We choose the proper range by comparing the threshold voltage v_{th} to the response value at time $t = \frac{\pi}{2\beta}$, i.e., $v(\frac{\pi}{2\beta}) = 1 - \frac{\sqrt{\alpha^2+\beta^2}}{\beta} exp(-\frac{\alpha}{\beta}(\rho - \frac{\pi}{2}))$. This procedure can be extended to other (e.g., ramp) input waveforms.

3 Constraint on Moments for Control of Undershoot/Overshoot

In this section, we illustrate how our simple threshold delay model can yield simple analytic constraints for interconnect synthesis. Specifically, we address the question of finding interconnect and driver parameters for optimum delay with controlled ringing. Consider a simple RLC line driven by a gate, with Z_S being the driver impedance and C_L being the load impedance at the end of the line. The characteristic impedance of the line is given by $Z_0 = \sqrt{\frac{R+sL}{sC}}$. Ideally, the driver and

line parameters are adjusted such that Z_S matches Z_0 and the voltage response at the end of the line is critically damped. However, if the driver impedance Z_S is just smaller than the characteristic impedance of the line, the voltage response will have a small amount of ringing: this can be advantageous in that the threshold delay will decrease [19]. The problem with ringing is that it can cause false switching if the voltage response drops back below the threshold; hence, the advantages of ringing can be exploited only if the maximum oscillation (overshoot or undershoot) is bounded such that false switching does not occur. We now develop an analytical equation that achieves this control in terms of coefficients of the transfer function. Additional context for our discussion may be found in [10].

The voltage response for ringing is given by

$$v_{out}(t) = V_0 \left[1 - \frac{\sqrt{\alpha^2 + \beta^2}}{\beta} e^{-\alpha t} sin(\beta t + \rho) \right]$$

where $\rho = tan^{-1}(\frac{\beta}{\alpha})$. To find the peaks of overshoot and undershoot in the response, we set the derivative $v'_{out}(t)$ to zero, yielding $\beta t = n\pi$ with $n = 1, 3, 5, ...$ for overshoots and $n = 2, 4, 6, ...$ for undershoots. The first undershoot occurs at time $T_1 = 2\pi/\beta$, and the value of the undershoot is

$$\delta v = V_0 e^{-\alpha T_1} \sqrt{1 + (\frac{\alpha}{\beta})^2} sin(\beta T_1 + \rho) = V_0 e^{-\alpha T_1}.$$

The constraint for a given percentage undershoot v_{us} can be obtained as

$$\frac{\alpha}{\beta} = \frac{1}{2\pi} |ln(v_{us})|$$

For example, with 5% undershoot, we have $v_{us} = 0.05 V_0$ and $\frac{\alpha}{\beta} = 0.48$. We can express α and β in terms of coefficients of the transfer function, i.e., $\frac{\alpha}{\beta} = \frac{b_1}{\sqrt{4b_2 - b_1^2}}$. Therefore,

$$b_1^2 = \left[\frac{4(\frac{\alpha}{\beta})^2}{(\frac{\alpha}{\beta})^2 - 1} \right] b_2$$

With 5% undershoot the above equation reduces to $b_1^2 = 0.74 b_2$ and a 90% threshold delay estimate for this case can be obtained (see [10]) as

$$T_{0.9} = 1.66 \frac{2b_2}{\sqrt{4b_2 - b_1^2}} = 2.13 b_1$$

Similarly, for 5% overshoot, the relation between the coefficients is $b_1^2 = 1.91 b_2$ and a corresponding delay estimate is $T_{0.9} = 1.20 b_1$. As expected, the delay increases for a strong undershoot requirement, and in general the delay increases if ringing in the response is suppressed [19]. The above constraint between α and β to reduce the undershoot in the response could be applied with the delay model in Equation (7) to perform delay-driven routing tree synthesis.

Length	Threshold	Delay (ps)		
μm	v_{th}	SPICE	Elmore	New
3000	10%	28	3	25
	20%	36	6	36
	30%	45	9	45
	40%	55	13	54
	50%	63	17	61
	60%	68	23	69
	70%	74	30	76
	80%	81	40	83
	90%	89	57	90
10000	10%	75	4	66
	20%	82	8	70
	30%	92	13	88
	40%	101	19	103
	50%	112	26	118
	60%	124	34	132
	70%	137	45	145
	80%	151	60	158
	90%	167	86	171
50000	10%	338	14	329
	20%	354	31	329
	30%	365	49	329
	40%	374	70	329
	50%	383	95	362
	60%	393	126	406
	70%	404	166	448
	80%	421	221	490
	90%	450	317	532

Table 1: Threshold delay estimates at various thresholds for non-monotone response under HSPICE, Elmore and our New models. Source resistance is 10 Ω and load capacitance is 2 pF.

4 Experimental Results

We evaluate the above models by simulating various RLC interconnect lines with different source/load impedances and different input rise times. We consider typical interconnect parameters encountered in MCM interconnects [3]. For all cases, the interconnect resistance, inductance and capacitance per length are $r = 3.0 \times 10^{-4} \Omega/\mu m$, $l = 0.433\ pH/\mu m$ and $c = 0.1\ fF/\mu m$, respectively and the length of the interconnect line ranges from 3000 to 50000μm. We also vary the load capacitance and the driver resistance from 2 to 3pF and from 10 to 70Ω, respectively. We compute delays at thresholds ranging from 10% to 90% from the response at the load using the HSPICE simulator (see Tables 1 - 4 for results with four of the configurations). For cases when the response is non-monotone the difference between delays from HSPICE and delays from our model is always less than 27% despite this large range of instances. The Elmore approximation always underestimates delays when the voltage thresholds are small, and can either overestimate or underestimate when the voltage thresholds are large. Overall, Elmore delay differs from HSPICE delay by up to 100%. When the response is monotone (i.e., with real poles), the maximum difference between our new model delay and HSPICE delay is 23%.

Length	Threshold	Delay (ps)		
μm	v_{th}	**SPICE**	**Elmore**	**New**
3000	10%	35	11	32
	20%	51	23	51
	30%	66	36	67
	40%	80	52	82
	5%	95	71	95
	60%	111	93	113
	70%	130	123	133
	80%	153	164	157
	90%	186	234	189
10000	10%	81	14	66
	20%	98	29	89
	30%	116	47	114
	40%	136	67	138
	50%	159	90	162
	60%	184	120	187
	70%	208	157	213
	80%	228	210	241
	90%	254	300	272
50000	10%	351	34	329
	20%	370	72	329
	30%	386	115	329
	40%	404	165	386
	50%	433	224	451
	60%	466	296	516
	70%	497	388	583
	80%	543	519	652
	90%	601	743	726

Table 2: Threshold delay estimates at various thresholds for non-monotone response under HSPICE, Elmore and our New models. Source resistance is 30 Ω and load capacitance is 3 pF.

5 Conclusions

We have developed a simple two-pole based analytical delay model which can estimate delay times corresponding to arbitrary threshold voltages when the interconnect response is non-monotone. Because our model takes into account the effect of inductance, we can estimate delay times for *RLC* lines far more accurately than with the Elmore delay model. We have also discussed a delay minimization approach that uses controlled small ringing in the response waveform. Ongoing work extends the analysis of threshold delays under nonmonotone response to more general input waveforms.

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Length	Threshold	Delay (ps)		
μm	v_{th}	**SPICE**	**Elmore**	**New**
3000	10%	32	12	29
	20%	46	26	45
	30%	60	42	61
	40%	75	60	77
	50%	92	81	94
	60%	112	107	115
	70%	138	141	141
	80%	173	188	176
	90%	234	269	234
10000	10%	78	17	66
	20%	92	35	83
	30%	108	56	108
	40%	125	80	129
	50%	145	109	153
	60%	169	144	180
	70%	198	190	210
	80%	226	253	246
	90%	269	363	293
50000	10%	347	44	329
	20%	365	93	329
	30%	379	149	329
	40%	394	213	378
	50%	413	289	447
	60%	452	383	520
	70%	482	503	601
	80%	538	672	693
	90%	615	961	805

Table 3: Threshold delay estimates at various thresholds for non-monotone response under HSPICE, Elmore and our New models. For the case of $h = 3000\mu m$ the poles are real (monotone response). Source resistance is 50 Ω and load capacitance is 2 pF.

Length	Threshold	Delay (ps)		
μm	v_{th}	**SPICE**	**Elmore**	**New**
3000	10%	38	18	36
	20%	58	37	58
	30%	78	60	79
	40%	101	86	102
	50%	126	116	128
	60%	158	154	160
	70%	198	202	200
	80%	255	270	256
	90%	352	386	351
10000	10%	84	22	66
	20%	105	47	95
	30%	128	75	132
	40%	155	108	166
	50%	185	146	197
	60%	217	193	227
	70%	253	253	269
	80%	302	339	324
	90%	377	485	397
50000	10%	356	51	329
	20%	377	108	329
	30%	397	172	350
	40%	427	246	425
	50%	466	334	502
	60%	508	442	585
	70%	562	581	678
	80%	642	777	786
	90%	762	1111	918

Table 4: Threshold delay estimates at various thresholds for non-monotone response under HSPICE, Elmore and our New models. For the case of $h = 3000\mu m$ the poles are real (monotone response). Source resistance is 50 Ω and load capacitance is 3 pF.