AN ANALYTICAL DELAY MODEL FOR RLC INTERCONNECTS

Andrew B. Kahng and Sudhakar Muddu**
UCLA Computer Science Department, Los Angeles, CA 90095-1596 USA
abk@cs.ucla.edu, sudhakar@cs.ucla.edu

ABSTRACT

We develop an analytical delay model based on first and second moments to incorporate inductance effects into the delay estimate for interconnection lines. Delay estimates using our analytical model are within 15% of SPICE-computed delay across a wide range of interconnect parameter values. We also extend our delay model for estimation of source-sink delays in arbitrary interconnect trees. For the small tree topology considered, we observe improvements of at least 18% in the accuracy of delay estimates when compared to the Elmore model (which is independent of inductance), even though our estimates are as easy to compute as Elmore delay. The speedup of delay estimation via our analytical model is several orders of magnitude when compared to a simulation methodology such as SPICE.

1. INTRODUCTION

Accurate calculation of propagation delay in VLSI interconnects is critical to the design of high speed systems. Current techniques are based on either *simulation* or (closed-form) *analytical formulas*. Simulation tools such as SPICE give the most accurate insight into arbitrary interconnect structures, but are computationally expensive. Transient simulation of lossy interconnects based on convolution techniques is presented in [8, 12]. Faster techniques based on moment computations are proposed in [11, 16, 17]. Since these methods are too expensive to be used during iterative layout optimization, the Elmore delay [2] approximation (which represents the first moment of the transfer function) is now widely used in the performance-driven design of clock distribution and Steiner global routing topologies. However, Elmore delay cannot accurately estimate the delay for RLC interconnect lines, i.e., the representation for interconnects whose inductive impedance cannot be neglected [4, 6]. Typically, the Elmore delay formula gives good estimates if interconnect lines are RC or overdamped, but gives overestimates for RLC or underdamped interconnects. This inaccuracy can be harmful for current performance-driven routing methods which try to optimize interconnect segment lengths and widths (as well as drivers and buffers) based on estimated delays.

This paper gives a new and accurate *analytical* delay estimate for distributed RLC interconnects which considers the effect of inductance. Previous moment-based analysis of RLC lines (e.g., [9, 8]) can derive a delay estimate only after simulating the response, rather than from an analytical formula. To validate our analysis and delay formula, we model VLSI interconnect lines having various combinations of source and load parameters, and obtain delay estimates from SPICE, Elmore delay and the proposed analytical delay model. The delay estimate using SPICE is extracted from a computed response at the specified node, whereas the other two models are closed-form expressions. Over our range of test cases, Elmore delay estimates can be quite far from the SPICE-computed delays, while our analytical delay model estimates are within 15% of SPICE delays. We also extend our delay model to estimate source-sink delays in arbitrary interconnect trees. For the small tree topology considered, our delay estimates are again within 18% of SPICE-computed delays, while Elmore delay estimates vary by as much as 35% from SPICE-computed delays. Since our analytical model has the same time complexity as the Elmore model, we believe that it can be useful in present-day performance-driven routing methodologies.

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2. PREVIOUS ANALYTICAL DELAY MODELS

The transfer function of an RLC interconnect line with source and load impedance (Figure 1) can be obtained using the ABCD parameters [1] as

$$H(s) = \frac{1}{(1 + \frac{Z_S}{Z_T})\cosh(\theta h) + (\frac{Z_S}{Z_0} + \frac{Z_0}{Z_T})\sinh(\theta h)} \qquad (1)$$

where $\theta = \sqrt{(r + sl)sc}$ is the propagation constant and $Z_0 = \sqrt{\frac{R+sL}{sC}}$ is the characteristic impedance; $r = \frac{R}{h}, l = \frac{L}{h}, c = \frac{C}{h}$ are resistance, inductance, and capacitance per unit length and h is the length of the line. To compute the RLC line response from the transfer function, the method of Padé approximation has been used by, e.g., [9, 10]. The output transfer function is expanded into a Maclaurin series of s around $s = 0$, and the series is truncated to desired order. In general, analytical computation of the exact voltage response is very tedious and is usually in the form of an infinite series.

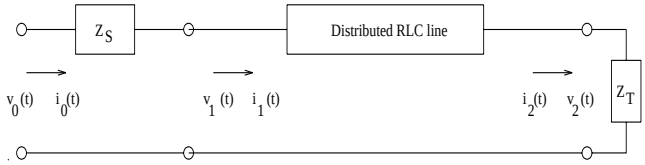

Figure 1. 2-port model of a distributed RLC line with source impedance Z_S and load impedance Z_T.

Efficient delay estimates for RC lines are typically derived by considering a single interconnect line with resistive source and capacitive load impedances; delay formulas for an interconnect tree entail recursive application of the formula for a single line. The analytical Elmore delay [2] estimate, Sakurai's heuristic delay formula [14, 15] and the single pole delay estimates of [3] have been widely used.

- Elmore delay is defined to be the first moment of the system impulse response, i.e., the coefficient of s or the first moment in the system transfer function $H(s)$. Applying this definition to $H(s)$ in Equation (1) and considering a source resistance R_S and a capacitive load C_T, the Elmore delay for a distributed RC or RLC line model is

$$T_{ED} = R_S(C + C_T) + R(\frac{C}{2} + C_T) \qquad (2)$$

  By considering only one pole in the transfer function, i.e, approximating the denominator polynomial to only first moment, the single-pole response can be obtained as in [3]. The single pole of the transfer function is equal to the inverse of the Elmore delay T_{ED}. Hence, the delay at arbitrary thresholds of the single-pole response can be directly related to Elmore delay (Elmore delay corresponds to the 63.2% threshold delay of the single-pole response).

For example, delay at 90% threshold voltage is $2.3 * T_{ED}$, i.e.,

$$T_{0.9} = 1.15RC + 2.3\,(R_S(C + C_T) + RC_T) \qquad (3)$$

Below, we use this expression to compute 90% threshold delay according to the Elmore model.

- Sakurai [14] also gives response and delay calculations for the distributed RC line. He calculates the time-domain response from the transfer function using the Heaviside expansion over poles of the transfer function. Then, he approximates the response using a single pole and observes the variation of delay with respect to source and load parameters; a 90% threshold delay estimate is *heuristically* obtained as $T_{0.9}(h) = 1.02RC + 2.3\,(R_S(C + C_T) + RC_T)$, quite similar to the Elmore delay equation (3).

Since these single pole delay estimates cannot accurately estimate delay for RLC interconnects, Zhou et al. [17] proposed a two-pole approximation for the transfer function to compute the *response* at the load for RLC interconnection trees. However, this technique does not provide any analytical expression for delay and is too time-consuming to be used in iterative layout optimization. Recently, [7] proposed to improve the Elmore delay model by using higher-order moments; this work gives a heuristic delay model equal to the sum of the first moment (M_1) and its standard deviation ($\sqrt{|M_1^2 - M_2|}$).[1]

3. A NEW ANALYTICAL DELAY MODEL

We now develop a simple closed-form delay estimate, based on first and second moments, which to our knowledge is the first analytical delay model that handles arbitrary threshold voltages and inductance effects for a distributed line. We model an arbitrary interconnect line as follows: (i) the source is modeled as a resistive and inductive impedance ($Z_S = R_S + sL_s$), and (ii) the load at the end of the interconnect line is modeled as a capacitive impedance ($Z_T = \frac{1}{sC_T}$). Thus, the transfer function for the interconnect line of Figure 1 is given by Equation (1). We truncate this transfer function by expanding the hyperbolic functions around $s = 0$; expansion around $s = \infty$ is not necessary since we consider only the first few coefficients of the transfer function. I.e., expanding *cosh* and *sinh* as infinite series and collecting terms up to the coefficient of s^2 in the denominator, we obtain the truncated transfer function

$$H(s) \approx \frac{1}{1 + sb_1 + s^2 b_2}$$

with coefficients $b_1 = R_S C + R_I C_T + \frac{RC}{2} + RC_T$ and $b_2 = \frac{R_S RC^2}{6} + \frac{R_S RCC_T}{2} + \frac{(RC)^2}{24} + \frac{R^2 CC_T}{6} + L_S C + L_S C_T + \frac{LC}{2} + LC_T$. Note that the first and second moments of the transfer function can be obtained from the coefficients b_1 and b_2, i.e., $M_1 = b_1$ and $M_2 = b_1^2 - b_2$. (We use the coefficient notation b_1, b_2 and the moment notation M_1, M_2 interchangeably according to the simplicity of the expression.) Depending on the sign of $b_1^2 - 4b_2$, the poles of the transfer function can be either real or complex. We separately derive our delay model from the two-pole response for each of these cases.

Real Poles:

The two-pole methodology [6, 17] yields the following response for the case of real poles:

$$v(t) = V_0(1 - \frac{s_2}{s_2 - s_1} e^{s_1 t} + \frac{s_1}{s_2 - s_1} e^{s_2 t})$$

[1] In the early drafts of our paper [6] we also considered exactly the same model; however, we found that it is not as accurate as our present model for various source and load parameters (see [6] for details).

R_S	L_S	C_T	SPICE	Elmore	New Model
Ω	pH	pF	ps	ps	ps
50	2.46	0.176	22.33	22.93	22.27
100	2.46	0.176	45.30	45.20	45.70
500	2.46	0.176	224.50	223.50	228.95
1000	2.46	0.176	446.20	446.4	457.46
25	2.46	1.76	107.10	108.40	108.65
50	2.46	1.76	210.40	210.80	214.74
100	2.46	1.76	415.20	415.40	425.10
500	2.46	1.76	2052.60	2053.0	2103.68
1000	2.46	1.76	4099.50	4100.0	4101.30

Table 1. 90% threshold delay estimates for combinations of source and load parameters for which the poles of the response are real (i.e., overdamped response). The interconnect line parameters are $r = 0.015\ \Omega/\mu m$, $l = 0.246\ pH/\mu m$ and $c = 0.176\ fF/\mu m$ and the length of the interconnect is $100\ \mu m$.

where $s_{1,2} = \frac{2}{-M_1 \pm \sqrt{4M_2 - 3M_1^2}}$. The condition for the poles to be real is $(4M_2 - 3M_1^2) \geq 0$. Since $s_2 - s_1 = -\frac{\sqrt{4M_2 - 3M_1^2}}{M_1^2 - M_2}$ is negative, the coefficients $\frac{s_2}{s_2 - s_1}$ and $\frac{s_1}{s_2 - s_1}$ are positive. Also, since the magnitude $|s_2|$ is greater than $|s_1|$, the second term in the response decreases rapidly compared to the first term. Hence, the two-pole response can be lower-bounded as

$$v(t) \approx V_0(1 - \frac{s_2}{s_2 - s_1} e^{s_1 t})$$

Since the voltage is lower-bounded, the delay obtained is an upper bound on the actual delay. The delay τ_r (the subscript indicates the case of real poles) at threshold voltage v_{th} is

$$\tau_r = \frac{K_r}{|s_1|} = K_r \frac{M_1 + \sqrt{4M_2 - 3M_1^2}}{2}$$

where K_r is a function of the coefficients b_1 and b_2, i.e., $K_r = \ln(\frac{1}{2(1 - v_{th})})[1 + \frac{b_1}{\sqrt{b_1^2 - 4b_2}}]$). For the wide range of source, load and interconnect parameter values considered in our simulations (see Table 1), we find that K_r for $v_{th} = 0.90$ is actually almost a constant, i.e., $K_r = 2.36$ gives a very strong fit between SPICE delay values[2] and $\frac{1}{|s_1|}$ [6]. Thus, we use

$$\tau_r = 2.36 * \frac{(M_1 + \sqrt{4M_2 - 3M_1^2})}{2}; \qquad (4)$$

the resulting delay estimates are compared against those of various other methods in Table 1. Our analytical delay model gives estimates close to those obtained from SPICE, but Elmore delay also gives good estimates for this case of overdamped response.

Complex Poles

The condition for complex poles is $(4M_2 - 3M_1^2) = (b_1^2 - 4b_2) \leq 0$. The time-domain response for complex poles [5] is

$$v(t) = V_0(1 - \frac{\sqrt{\alpha^2 + \beta^2}}{\beta} e^{-\alpha t} * \sin(\beta t + \rho))$$

where $\alpha = \frac{M_1}{2(M_1^2 - M_2)}$, $\beta = \frac{\sqrt{3M_1^2 - 4M_2}}{2(M_1^2 - M_2)}$ and $\rho = \tan^{-1}(\frac{\beta}{\alpha})$. Using the above equation and threshold voltage v_{th}, we get

$$e^{-\alpha t} * \sin(\beta * t + \rho) = \frac{1 - v_{th}}{\sqrt{1 + (\frac{\alpha}{\beta})^2}}\ . \qquad (5)$$

[2] SPICE simulation results are obtained using SPICE3 and the built-in LTRA (lossy transmission line) model, which is based on convolution techniques [12].

R_S Ω	L_S pH	C_T pF	SPICE ps	Elmore ps	New Model ps
10	0.0246	0.0176	1.22	0.90	1.30
15	0.0246	0.0176	1.33	1.31	1.38
20	0.0246	0.0176	1.47	1.71	1.51
25	0.0246	0.0176	1.60	2.12	1.64
10	0.0246	0.176	4.50	5.12	4.25
15	0.0246	0.176	5.85	7.32	5.31
20	0.0246	0.176	7.90	9.55	8.60
10	2.46	0.0176	1.31	0.90	1.40
15	2.46	0.0176	1.40	1.31	1.49
20	2.46	0.0176	1.55	1.71	1.59
25	2.46	0.0176	1.63	2.12	1.69
10	2.46	0.176	4.65	5.10	4.30
15	2.46	0.176	5.85	7.33	5.30
20	2.46	0.176	7.98	9.55	8.70
10	24.6	0.0176	1.80	0.90	1.96
15	24.6	0.0176	1.89	1.31	2.06
20	24.6	0.0176	2.00	1.71	2.15
25	24.6	0.0176	2.19	2.11	2.21
10	24.6	0.176	5.65	5.10	5.44
15	24.6	0.176	6.50	7.33	5.95
20	24.6	0.176	7.66	9.55	6.97
25	24.6	0.176	9.47	11.78	9.26

Table 2. 90% threshold delay estimates for combinations of source and load parameters for which the poles of the response are complex (i.e., underdamped response). The interconnect line parameters are $r = 0.015$ $\Omega/\mu m$, $l = 0.246$ $pH/\mu m$ and $c = 0.176$ $fF/\mu m$ and the length of the interconnect is 100 μm.

The delay at a given threshold voltage can be computed by solving for time in Equation (5) recursively. One way to solve the recursive Equation (5) is to approximate the time variable in the exponential term by Elmore delay, i.e., substitute T_{ED} for time t. Expanding *sine* as a Taylor series and considering only the first term yields

$$\tau_c = \frac{K_c}{\beta} = K_c * \frac{2(M_1^2 - M_2)}{\sqrt{3M_1^2 - 4M_2}}$$

where $K_c = \frac{(1-v_{th})e^{\alpha * T_{ED}}}{\sqrt{1+(\frac{\alpha}{\beta})^2}} - \rho$. Even though K_c is a function of b_1 and b_2, for a wide range of interconnect, source and load parameters it too is almost a constant, i.e., $K_c = 1.66$ gives a good fit between SPICE delay values and $\frac{1}{\beta}$ [6]. In other words, our 90% threshold delay estimate for complex poles is

$$\tau_c = 1.66 \cdot \frac{2(M_1^2 - M_2}{\sqrt{3M_1^2 - 4M_2}} \,. \qquad (6)$$

Table 2 shows delay values for various combinations of source, load and interconnect parameters assuming this value of K_c. The delay estimates using our analytical model are within 15% of SPICE-computed delay estimates, while Elmore delay estimates vary by as much as 33% from SPICE-computed delays. Hence, for the case of complex poles (i.e., underdamped response), the Elmore model is no longer acceptably accurate.

As detailed in [6], we have also considered the special case in which poles are equal, i.e., a double pole configuration. The delay at 90% threshold for this case can be obtained as $\tau_{0.9} = K_d \frac{b_1}{2}$, which gives a recursive equation for K_d, i.e., $K_d = \ln(10(1 + K_d))$ from which $K_d \approx 3.9$. Thus, in the case of a double pole we estimate the 90% threshold delay as

$$\tau_{0.9} = K_d \cdot \frac{b_1}{2} = 1.95 b_1 \qquad (7)$$

which is independent of the inductance value and different from the Elmore delay expression.

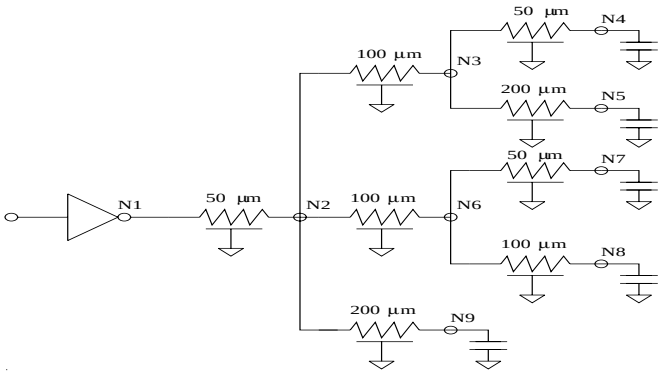

Figure 2. A simple interconnection tree consisting of distributed RLC lines.

4. INTERCONNECTION TREES

We conclude with an extension of our analytical model to estimate delays in arbitrary interconnect trees. An RLC network is called an RLC tree if it does not contain a closed path of resistors and inductors, i.e., all resistors and inductors are floating with respect to ground and all capacitors are connected to ground. Consider an RLC interconnect tree with root (or source) S and set of sinks (or leafs) $L = \{L_1, L_2, \ldots, L_n\}$. The unique path from root S to sink node i is denoted by $p(i)$ and is referred to as the *main path*. The edges/nodes not on the main path are referred as the *off-path* edges/nodes. We model each edge on the main path of the tree using a lumped RLC segment, e.g., an **L**, **T**, or **Π** model. We replace the off-path subtree rooted at node j with the total subtree capacitance at node j. (Figure 3 shows an example of a main path where each branch in the tree is replaced by RLC segments, and the off-path subtrees are replaced by their respective subtree capacitances.) At any node j, the total capacitance is given by

$$\begin{aligned} C'_j &= C_j && \text{if no off-path subtree at node } j \\ &= C_j + C_{T(j)} && \text{if node } K \text{ has off-path subtree } T(j) \end{aligned}$$

where C_j is the capacitance at the node and $C_{T(j)}$ is the off-path subtree capacitance at node j. The k^{th} coefficient b_k of the transfer function for the general RLC circuit of Figure 3 can be expressed using the following recursive equation [5]:

$$b_k^M = R_{M-1} \sum_{j=1}^{M-1} C'_j \cdot b_{k-1}^j + L_{M-1} \sum_{j=1}^{M-1} C'_j \cdot b_{k-2}^j + b_k^{M-1} \qquad (8)$$

where b_K^M refers to the coefficient of s^k in the transfer function

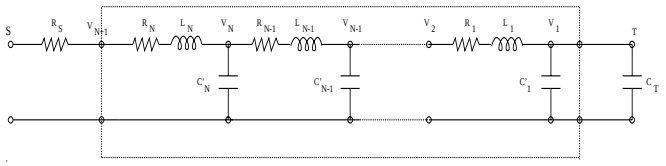

Figure 3. Representation of the main path in the tree, where each distributed line is modeled using RLC segments.

between node M and node 1. Note that $b_0^j = 1$, $b_{-1}^j = 0$ for all j and $b_k^1 = 0$ for all k. Using the above recursive equation the expressions for the first and second coefficients of the transfer function at the root can be derived as

$$b_1^{N+1} \quad = \quad R_N \sum_{j=1}^{N} C'_j + b_1^N = \sum_{i=1}^{N} R_i \sum_{j=1}^{i} C'_j$$

$$b_2^{N+1} = \sum_{j=2}^{N} C_j' \sum_{l=j}^{N} R_l \sum_{i=1}^{j-1} C_j' \sum_{d=i}^{j-1} R_d + \sum_{j=1}^{N} C_j' \sum_{l=j}^{N} L_l \quad (9)$$

For any given source and sink pair the coefficients b_1 and b_2 can be computed in linear time by traversing the main path and using the above recursive equation. Using the analytical delay model developed in the previous section, we can obtain an analytical delay estimate for RLC interconnect trees using the first and second coefficients. Thus, the 90% threshold delay at a given sink i, depending on the value of $(4M_2 - 3M_1^2)$, is

$$T_{ND}(i) = \begin{cases} K_r \cdot \frac{(M_1 + \sqrt{4M_2 - 3M_1^2})}{2} & \text{for Real poles} \\ K_c \cdot \frac{2(M_1^2 - M_2)}{\sqrt{3M_1^2 - 4M_2}} & \text{for Complex poles} \\ K_d \cdot \frac{M_1}{2} & \text{for Double poles} \end{cases} \quad (10)$$

where the first and second moments are expressed as $M_1 = b_1$ and $M_2 = b_1^2 - b_2$. The coefficients of the transfer function are obtained from Equation (9). By contrast, 90% threshold delay according to the Elmore model is simply $T_{ED}(i) = 2.3 * M_1$.

We evaluate our analytical model by considering the simple interconnection tree shown in Figure 2. We consider the sink node $N4$ for delay estimation. Each edge on the main path between the root and node $N4$ is replaced by a two-**L** segment model.[3] We then apply the above recursive coefficient computation for the resultant RLC circuit of the main path. The 90% threshold delays according to both the Elmore model and our new analytical model (Equation (10)) are then computed. We also compute the delay at the given sink node using SPICE3e, where each edge of the tree is modeled using the LTRA (Lossy Transmission Line) model (with SPICE, we first compute the response at the sink node and then find the delay for 90% threshold voltage). Table 3 compares delay estimates over a range of interconnect parameters, driver resistance values, and sink load capacitance values: Elmore delay varies by as much as 35% from the SPICE-computed delay, but our new model is within 18% of the SPICE delay for all examples. Note that our delay estimates also require three orders of magnitude less computation than SPICE, since they have the same time complexity as the Elmore delay estimate.

5. CONCLUSIONS

Fast delay estimation methods, as opposed to simulation techniques, are needed for incremental performance-driven layout synthesis. Elmore delay based estimation methods, although efficient, cannot accurately estimate the delay for RLC interconnect lines. We have obtained an analytical delay model, based on first and second moments of RLC interconnection lines, which considers the effect of inductance. The resulting delay estimates are significantly more accurate than Elmore delay estimates We also extend our delay model to estimate source-sink delays in arbitrary interconnect trees. For the small tree topology considered, we observe improvement of at least 18% in the accuracy of our delay estimates, compared to the Elmore model. Since our model has the same time complexity as the Elmore model, we believe it can be valuable in modern iterative layout synthesis methodologies. Ongoing work applies our analytical model to delay-driven routing tree construction, zero-skew routing, and delay estimation in nets spanning multiple routing layers (i.e., with modeling of vias).

Line Para. ($/\mu m$)	C_L (pF)	Delay (ps) SPICE	Elmore	New Model
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 0.246\ pH$	0.02	5.7	6.6	5.0
$R = 0.0015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	0.2	37	26	31
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	0.2	39	29	32
$R = 0.0015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	2.0	179	238	205
$R = 0.0015\ \Omega$ $C = 0.176\ fF$ $L = 0.246\ pH$	2.0	231	238	232
$R = 0.015\ \Omega$ $C = 0.176\ fF$ $L = 2.46\ pH$	2.0	199	270	230

Table 3. 90% threshold delay values for a wide range of interconnect parameters at Node 4 of the tree in Figure 5. The driver resistance is $R_S = 10\Omega$. We compare SPICE LTRA, and the Elmore model, against our analytical delay model.

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[3] Our model is not limited to traditional segment models, and indeed we believe the accuracy of our results would improve if we use non-uniform segment models [5] designed to perfectly match the low-order moments of the distributed RLC line.