Efficient Gate Delay Modeling for Large Interconnect Loads *

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Abstract

With fast switching speeds and large interconnect trees (MCMs), the resistance and inductance of interconnect has a dominant impact on logic gate delay. In this paper, we propose a new Π model for distributed *RC* and *RLC* interconnects to estimate the driving point admittance at the output of a CMOS gate. Using this model we are able to compute the gate delay efficiently, within 25% of SPICE-computed delays. Our parameters depend only on total interconnect tree resistance and capacitance at the output of the gate. Previous "effective load capacitance" methods [7, 9], applicable only for distributed *RC* interconnects, are based on Π model parameters obtained via a recursive admittance moment computation. Our model should be useful for iterative optimization of performance-driven routing or for estimation of gate delay and rise times in high-level synthesis.

Keywords: gate delay, reduced-order models, driving point admittance, effective capacitance, interconnect modeling

1 Introduction

As the feature size of integrated circuits decreases, gate delays decrease and interconnect delays increase. The overall logic-stage delay consists of a gate delay component plus an interconnect delay component. Previously, the gate delay component could be estimated by modeling the entire interconnect tree at the gate output as a simple lumped capacitance. Now, with increased interconnect resistance and larger interconnect trees, the lumped capacitance approximation results in pessimistic delay and rise time calculations. Accurate estimation of gate delay and rise time closely depends on the model for the driving point admittance of a load interconnect tree at the output of a gate.

Furthermore, with interconnect delays dominating overall path delays for current integrated circuits, algorithms for synthesis and layout optimization must consider interconnect effects. It has been observed that existing accurate delay estimates are not efficient enough to be used in iterative gate and interconnect sizing during the typical synthesis/layout/in-place optimization loop. Incremental delay analysis is also needed during performance-driven routing.

We propose a simple, efficient model for driving point admittance which can be used in an iterative regime to accurately predict gate delays. The simplest approximation of the driving point admittance of the load interconnect tree is the total capacitance of the tree (C_{tot}), which is a (pessimistic) first-order approximation [7, 8].[1] For submicron technologies and MCM interconnects, the total interconnect resistance is large and comparable to the driver output resistance; it cannot be neglected in the gate delay calculations. The actual delay is much smaller than that derived from the lumped capacitance model, because the interconnect resistance acts as a shield to reduce the load capacitance seen by the gate driver. Another simple method – which approximates the load tree using a simple lumped *RC* segment model with resistance and capacitance equal to the total interconnect resistance (R_{tot}) and total interconnect capacitance (C_{tot}) – yields an optimistic delay estimate because the total interconnect resistance is lumped together and shields the total capacitance. The lumped capacitance and the lumped *RC* models are among standard options in present day synthesis and layout tools, e.g., [11].

O'Brien and Savarino [4] have proposed a one-segment Π model (see Figure 1) to approximate the load interconnect at the gate, matching the first three moments of the driving point admittance of the gate. The moments of the driving point admittance are computed recursively [4, 5]. The response waveform obtained using the Π model is reasonably close to the actual response for most examples. Recently, [7, 9] have argued that empirical ("k-factor") formulas for delay and output rise time of gates should depend only on the input slew rate and load capacitance. To make the Π model compatible with k-factor delay formulas, they compute an "effective load capacitance" iteratively using the Π model parameters derived from the recursive admittance moment computation. The authors of [7, 9] further extend the effective capacitance computation to accurately predict the response waveform tail, via a two-piece gate output waveform approximation. The methodology is quite accurate, but requires significant computation time even when only the first three moments are calculated for each gate load. I.e., although the moment computation is linear, calculating the moments for each gate load can be expensive for large designs. Thus, we now propose a new Π model for estimating the driving point admittance at the output of a CMOS gate. Whereas previous methods [7, 9] are for distributed *RC* interconnects, we propose gate load models for both *RC* and *RLC* interconnects. Our Π model parameters depend only on the total (lumped) interconnect tree parameters at the output of the gate, and match the first three moments of the driving point admittance of the load interconnect tree. For various interconnect topologies the gate delay and the rise time are within 25% of SPICE-computed delays, whereas lumped capacitance based delay estimates are off by as much as 150%.

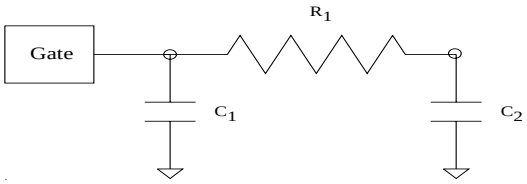

Figure 1: One-segment Π model for matching the first three moments of the driving point admittance of a load interconnect tree.

2 Computation of Driving Point Admittance

There have been many studies [2, 3, 6] of the moments and coefficients[2] of the transfer function. As noted above, O'Brien and Savarino [4] give a set of rules for recursively computing the first three moments of the driving point admittance for discrete elements and for distributed *RC* interconnects. Sriram and Kang [10] compute the admittance at the root of the tree by modeling each interconnect as multiple *RC*/*RLC* segments, then recursively compute the admittance using the expression for a single *RLY* section. They first express the admittance at each node as a rational function, and then convert to a polynomial series of required accuracy. In this section we briefly review the computation of

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[1] C_{tot} includes the load capacitance at the leaves. Coupling effects may be taken into consideration by including their effect in the total capacitance.

[2] The coefficients of the transfer function refer to terms in the inverse of the transfer function polynomial.

admittance coefficients and also show an interesting relationship between the coefficients of the numerator and denominator polynomials of the admittance expression.

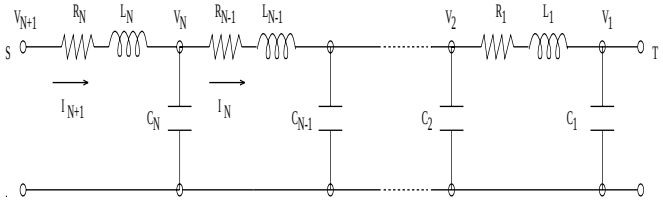

Figure 2: N-segment RLC circuit.

Consider a general circuit consisting of N RLC segments as shown in Figure 2. Such a circuit can be used to model any distributed RLC interconnect line. From KCL, the current at node $N+1$ can be written using the recursive equation

$$I_{N+1}(s) = sC_N V_N(s) + I_N(s) = \sum_{j=1}^{N} sC_j V_j(s) \quad (1)$$

Without loss of generality, we can express the current and node voltages as a series in s, i.e.,

$$\frac{I_j(s)}{V_1(s)} = a_0^j + a_1^j s + a_2^j s^2 + a_3^j s^3 + \dots$$
$$\frac{V_j(s)}{V_1(s)} = b_0 + b_1^j s + b_2^j s^2 + b_3^j s^3 + \dots$$

Replacing the node voltages and currents in Equation (1) and collecting terms for coefficients of s^k ($k \geq 1$), we get

$$a_k^{N+1} = C_N b_{k-1}^N + a_k^N = \sum_{j=1}^{N} C_j b_{k-1}^j \quad (2)$$

For RLC circuits and RLC interconnects, the coefficient $a_0^j = 0$. The transfer function between the source node S and the node T can be expressed as

$$H(s) = \frac{V_1(s)}{V_{N+1}(s)} = \frac{1}{b_0 + b_1^{N+1} s + b_2^{N+1} s^2 + b_3^{N+1} s^3 + \dots}$$

The transfer function coefficients can also be obtained by expressing the voltage at node $N+1$ recursively in terms of voltage at node N [1]. Therefore, the coefficient of s^k in the transfer function polynomial is

$$b_k^{N+1} = R_N \sum_{j=1}^{N} C_j \cdot b_{k-1}^j + L_N \sum_{j=1}^{N} C_j \cdot b_{k-2}^j + b_k^N = \sum_{j=1}^{N} C_j b_{k-1}^j \sum_{i=j}^{N} R_i + \sum_{j=1}^{N} C_j b_{k-2}^j \sum_{i=j}^{N} L_i \quad (3)$$

The numerator and denominator polynomials of the driving point admittance can be obtained by expressing the voltage $V_{N+1}(s)$ in terms of the transfer function, i.e.,

$$Y(s) = \frac{I_{N+1}(s)}{V_{N+1}(s)} = \frac{I_{N+1}(s)}{V_1(s)} \cdot H(s) = \frac{a_1^{N+1} s + a_2^{N+1} s^2 + a_3^{N+1} s^3 + \dots}{b_0 + b_1^{N+1} s + b_2^{N+1} s^2 + b_3^{N+1} s^3 + \dots}$$

We now express the driving point admittance as an infinite series

$$Y(s) = \sum_{i=1}^{\infty} A_i s^i$$

where A_i represents the i^{th} moment of the admittance function. The driving point admittance moments can also be expressed in terms of the coefficients a_k and b_k from Equations (2) and (3):

$$A_i = \frac{-1}{b_0} \sum_{j=1}^{i} b_j^{N+1} A_{i-j} + \frac{a_i^{N+1}}{b_0} \quad (4)$$

3 An RC Model for the Driving Point Admittance

In this section, we develop a one-segment RC Π model, with *predetermined* parameter values that depend only on the total resistance and total capacitance, to model the driving point admittance of a distributed RC interconnect tree. Recall that previous methods compute Π model parameters using the first three moments of the driving point admittance of the load interconnect at the gate output. Our advantage over previous methods lies in the trivial expense of finding the parameters of our model. The driving point admittance of the Π equivalent circuit in Figure 1 is

$$Y_{eq}(s) = sC_1 + \frac{sC_2}{1 + sR_1C_2} = s(C_1 + C_2) - s^2 R_1 C_2^2 + s^3 R_1^2 C_2^3 + \dots \quad (5)$$

Let the driving point admittance at the gate output be represented by

$$Y(s) = \sum_{i=1}^{\infty} A_i s^i = sA_1 + s^2 A_2 + s^3 A_3 + \dots$$

The parameters of the equivalent circuit can be obtained by comparing the first three moments of the admittance with the corresponding coefficients in Equation (5), i.e.,

$$R_1 = \frac{-A_3^2}{A_2^3} \quad C_1 = A_1 - \frac{A_2^2}{A_3} \quad C_2 = \frac{A_2^2}{A_3} \quad (6)$$

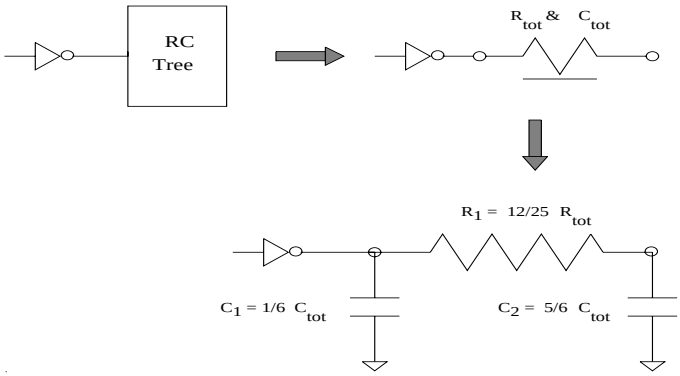

Figure 3: An open-ended RC line to capture an RC interconnect tree, and the RC Π model.

Our new model is an "open-ended RC Π model" derived as follows. Rather than recursively compute the driving point admittance moments at the gate, we approximate the entire interconnect tree by an equivalent open-ended RC line whose resistance and capacitance are equal to the total interconnect resistance and capacitance, as shown in Figure 3. By using an open-ended RC line to approximate the entire tree, the

distributed nature of the load interconnect is still considered in the calculation of model parameters (i.e., the resistance of the open-ended line shields part of the load capacitance from the gate driver), yet we gain efficiency by easily deriving the moments of the resultant driving point admittance.

The admittance of an open-ended *RC* line can be obtained from the 2-port parameters as [2]

$$\begin{aligned} Y(s) &= \frac{\tanh(\theta)}{Z_0} \\ &= sC_{tot} - s^2\frac{R_{tot}C_{tot}^2}{3} + s^3\frac{2R_{tot}^2C_{tot}^3}{15} + \dots \end{aligned} \quad (7)$$

where the propagation constant $\theta = \sqrt{R_{tot}sC_{tot}}$, and the characteristic impedance $Z_0 = \sqrt{\frac{R_{tot}}{sC_{tot}}}$. Therefore, the first three moments of the driving point admittance using the open-ended line approximation are

$$A_1 = C_{tot}, \quad A_2 = -\frac{R_{tot}C_{tot}^2}{3}, \quad A_3 = \frac{2R_{tot}^2C_{tot}^3}{15}$$

Substituting the above driving point admittance moments in Equation (6) yields Π model circuit parameters[3]

$$R_1 = \frac{12R_{tot}}{25}, \quad C_1 = \frac{C_{tot}}{6}, \quad \text{and} \quad C_2 = \frac{5C_{tot}}{6}$$

The new Π model has parameters that are functions of only total interconnect resistance and capacitance, and yet it still closely approximates the first three moments of the driving point admittance of the load.

4 An *RLC* Model for the Driving Point Admittance

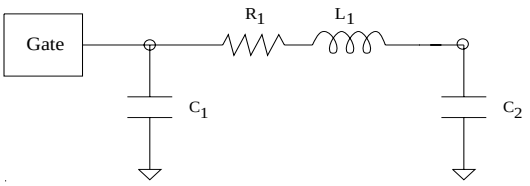

Figure 4: A *RLC* Π model for matching the first three moments of the driving point admittance of an *RLC* interconnect tree.

In this section, we develop a one-segment *RLC* Π model (Figure 4) to model the driving point admittance of a distributed *RLC* interconnect tree. To our knowledge, no *RLC* interconnect load model has been given previously. The driving point admittance of the *RLC* Π model in Figure 4 is

$$\begin{aligned} Y_{eq}(s) &= sC_1 + \frac{sC_2}{1+sC_2(R_1+sL_1)} \\ &= s(C_1+C_2) - s^2R_1C_2^2 + s^3\left(R_1^2C_2^3 - L_1C_2^2\right) + \dots \end{aligned} \quad (8)$$

Similar to the driving point admittance approximation for the *RC* interconnect tree, we approximate the entire *RLC* interconnect tree with an equivalent open-ended *RLC* line whose resistance, inductance and capacitance are equal to the total interconnect resistance, inductance and capacitance as shown in Figure 5. The admittance of an open-ended *RLC* line can be obtained as

$$\begin{aligned} Y(s) &= \frac{\tanh(\theta)}{Z_0} \\ &= \frac{sC_{tot} + \frac{s^2R_{tot}C_{tot}^2}{6} + s^3(\frac{R_{tot}^2C_{tot}^3}{120} + \frac{L_{tot}C_{tot}^2}{6}) + \dots}{1 + \frac{sR_{tot}C_{tot}}{2} + s^2(\frac{R_{tot}^2C_{tot}^2}{24} + \frac{L_{tot}C_{tot}}{2}) + \dots} \\ &= sC_{tot} - \frac{s^2R_{tot}C_{tot}^2}{3} + s^3(\frac{2R_{tot}^2C_{tot}^3}{15} - \frac{L_{tot}C_{tot}^2}{3}) + \dots \end{aligned} \quad (9)$$

where the propagation constant $\theta = \sqrt{(R_{tot}+sL_{tot})sC_{tot}}$, and the characteristic impedance $Z_0 = \sqrt{\frac{(R_{tot}+sL_{tot})}{sC_{tot}}}$.

As before, the open-ended *RLC* line model can be further approximated to a reduced-order Π model without losing much accuracy in the delay estimates. Matching the resistive terms of Equation (8) and (9) alone will yield the same parameters as derived for the *RC* Π model. The inductance parameter of the Π model can be obtained by matching the inductive term in the third moment of the driving point admittance and using the previously derived *RC* Π model resistance and capacitance values. Therefore, the *RLC* Π model parameters for the driving point admittance of an *RLC* interconnect tree are

$$R_1 = \frac{12R_{tot}}{25} \quad L_1 = \frac{12L_{tot}}{25} \quad C_1 = \frac{C_{tot}}{6} \quad C_2 = \frac{5C_{tot}}{6}$$

where L_{tot} is the total inductance of the interconnect tree.

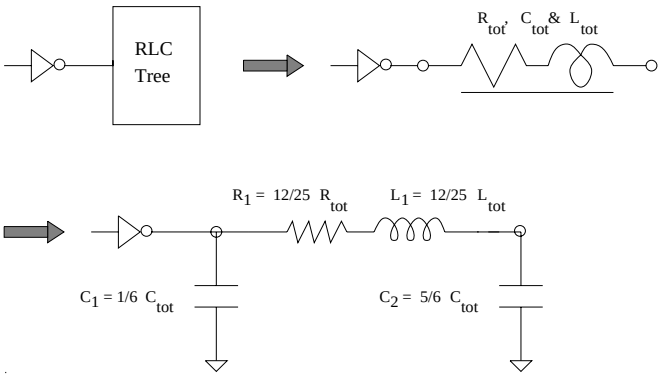

Figure 5: An open-ended *RLC* line to capture an *RLC* interconnect tree, and the *RLC* Π model.

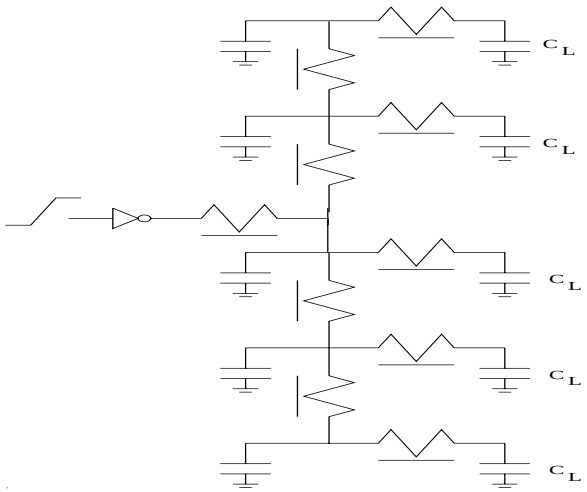

Figure 6: An inverter (2-input NAND with identical inputs) driving an *RC* interconnect tree with 10 interconnects and 5 loads. All the interconnects are identical with parameters $R = 0.25\,\Omega/\mu m$, and $C = 0.015\,fF/\mu m$, and all load and discrete capacitors = $50\,fF$. The length and width of the transistors in the driver are $1\mu m$ and $16\mu m$.

[3] We also studied another approximate model with $R_1 = R_{tot}$ in the Π circuit [2], the motivation being that the resistance of the equivalent circuit should be the same as the total resistance of the load interconnect tree. However, delay estimates were always less accurate than with the model we give here.

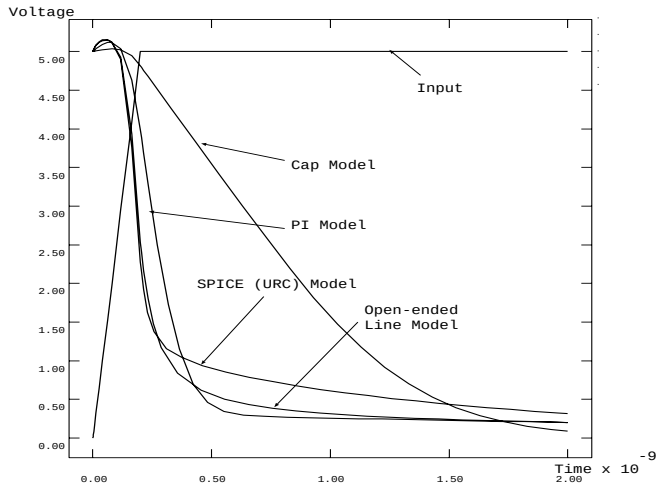

Figure 7: Response waveform at gate output with load interconnect tree shown in Figure 3 for Example 1. The proposed open-ended *RC* line model and the Π model very closely estimates the actual response (URC model) than does the total capacitance model.

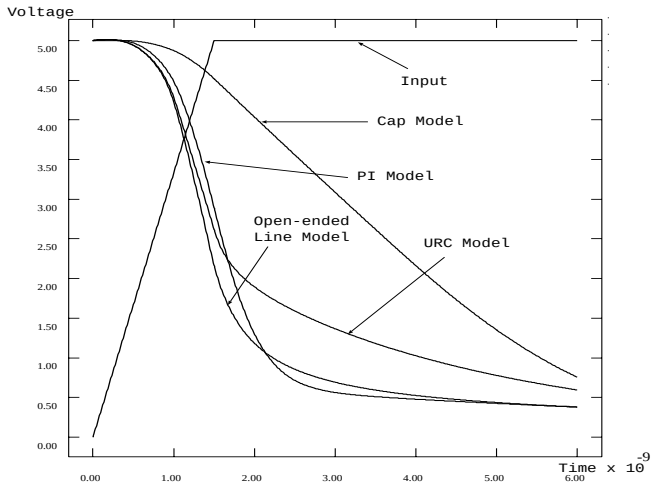

Figure 8: Response waveform for Example 2, i.e., load interconnect tree of Figure 3 with longer interconnect lengths. Both the open-ended line model and the Π model more closely estimate the actual response than does the total capacitance model.

	N-channel	P-channel		N-channel	P-channel
TOX	2.0E-08	2.0E-08	GAMMA	0.4481	0.4970
PHI	0.60	0.60	NSUB	1.8E+16	2.2E+16
XJ	0.15	0.15	NFS	2.4E+12	4.6E+12
TPG	1.0	1.0	VMAX	1.5E+05	1.8E+05
VTO	0.7333	-0.9679	ETA	1.5E-01	1.8E-01
DELTA	9.5E-01	4.3E-01	KAPPA	9.5E-02	3.2E+00
LD	1.0E-09	1.0E-09	CGDO	2.6E-12	2.6E-12
KP	1.3E-04	4.3E-05	CGSO	2.6E-12	2.6E-12
UO	762.1	254.0	CGBO	3.0E-10	3.5E-10
THETA	5.3E-02	1.7E-01	CJ	1.2E-04	5.3E-04
RSH	2.365	2.553	MJ	0.4398	0.5074
CJSW	4.7E-10	7.9E-11	MJSW	0.1240	0.0772
PB	0.80	0.85			

Table 1: SPICE Level 3 model parameters. The channel length and width of the devices for most examples are $1\mu m$ and $4\mu m$.

5 Experimental Results

In this section we simulate various *RC*/*RLC* interconnect topologies to show the accuracy of both the open-ended line model and the reduced-order Π model. The SPICE model parameters for the gate driver, a 2-input NAND gate with both input signals the same, are shown in Table 1. We varied length and width for the transistors, as well as rise time for the input signal.

The authors of [7] noted that for small, balanced interconnect trees, the total capacitance model yields fairly accurate gate delay estimates. For trees with resistive and long nets (e.g., MCMs) the Π model of [7] (applying the recursive admittance computation and then using the iterative effective capacitance formula) yields estimates very close to the actual delays. We now show that our "open-ended *RC* Π model" also gives fairly accurate delay estimates, with the same time complexity as for the traditional lumped capacitance model. We verify our models by plotting the output response for the same interconnect trees studied in [7], as well as for a topology having larger fanout.

Example 1: Consider the load interconnect topology shown in Figure 6. We assume the length of each interconnect to be $4mm$, and all load and discrete capacitors are $50\,fF$. We used the 2-input NAND gate with the identical inputs as the driver; the length and width of the transistors in the driver are $1\mu m$ and $16\mu m$. We obtained the exact response at the gate output using SPICE3e and the URC (Uniform distributed *RC*) model for each *RC* interconnect. We then obtained the response for the total capacitance model, and for both the "open-ended" line model and our Π model, using SPICE3e[4]; see Figure 7. In [7] the same interconnect topology with smaller and less resistive nets was analyzed, and it was observed that for such balanced interconnect trees the total capacitance model gives fairly accurate results. However, Figure 7 shows that for large interconnect lines, the total capacitance model fails to follow the SPICE response curve while the proposed Π model still estimates the SPICE response accurately. Note that the response at the gate output for the model in [4] is identical to the SPICE response. Thus, we do not separately list the delay values or plot the response for the Π model in [4].

Example 2: We consider the same load interconnect topology used in Example 1, but the length of each interconnect is increased to $8mm$ and all load and discrete capacitor values are decreased to $10\,fF$. We also changed the length and width of the transistors in the driver to $1\mu m$ and $4\mu m$ to increase the driver resistance. The response at the gate output in Figure 7 shows that both the "open-ended" line model and our Π model still closely approximate the SPICE URC response for long interconnect lines. Notice that our Π model tracks the effect of interconnect shielding. Figure 7 shows that the waveform tail of both the "open-ended" line model and our Π model deviate from the actual response. The error in our model (with respect to the URC model) stems from the open-ended *RC* approximation, but we again note that this is a tradeoff with complexity. A comparison of threshold delays between various models is given in Table 2.

Example 3: A different load interconnect tree topology is shown in Figure 9. The authors of [7] noted that for such long (chain-like) interconnect topologies, the lumped capacitance model could not yield accurate gate delay estimates, while their effective capacitance model obtains an accurate response. Indeed, the effective capacitance model of [7] produces a response waveform that is closer to the actual response, except at the tail end of the waveform. Our Π model also gives a fairly

[4] Even though we have used SPICE for computing delay estimates with our Π model, we could also use, e.g., the Elmore delay model to compute the delay estimates during layout optimization.

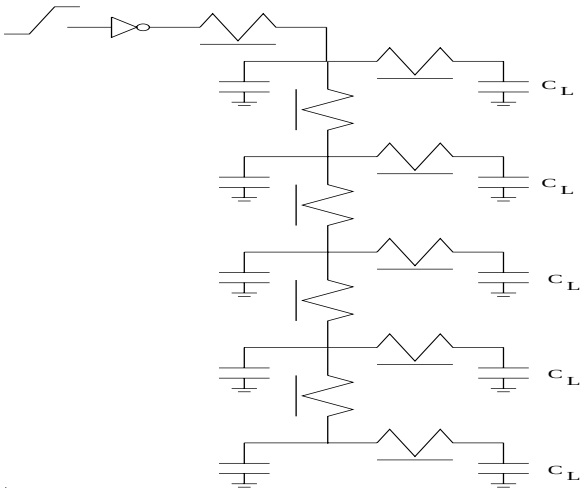

Figure 9: An inverter driving a different load interconnect topology. All the interconnects are identical with parameters $R = 0.25\,\Omega/\mu m, C = 0.015\,fF/\mu m$, length = $8mm$. All load and discrete capacitors are $10\ fF$. The length and width of the transistors in the driver are $1\mu m$ and $4\mu m$.

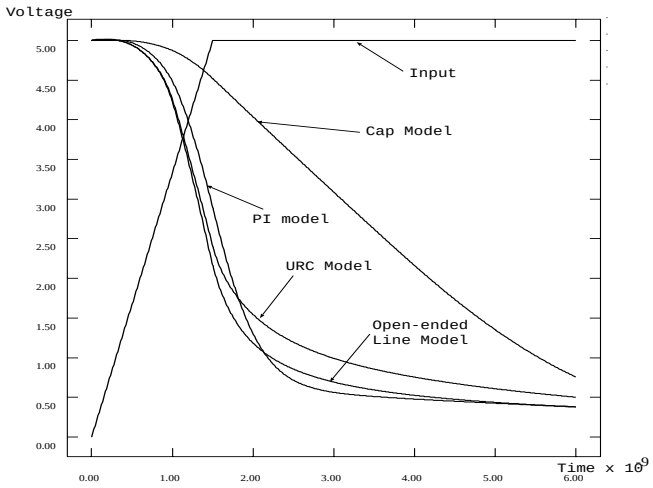

Figure 10: The response waveform at the inverter output for the interconnect tree in Figure 5, corresponding to for Example 3.

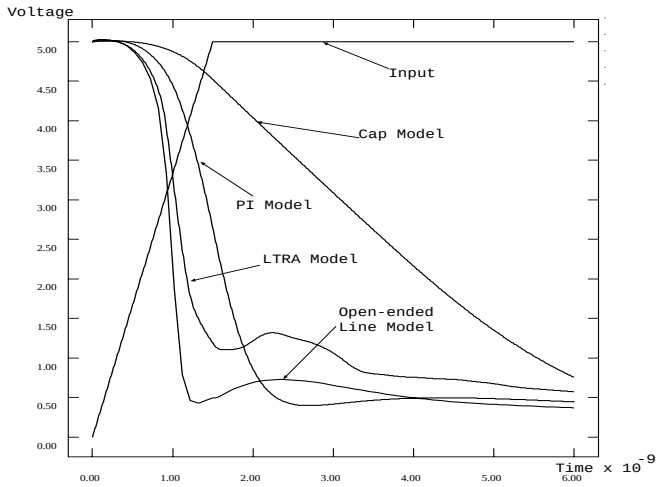

Figure 11: The response waveform for Example 4 at the inverter output of the interconnect tree in Figure 9, considering also the inductance of the lines. The inductance of each line is $L = 0.246\,nH/\mu m$, with all other parameters as before.

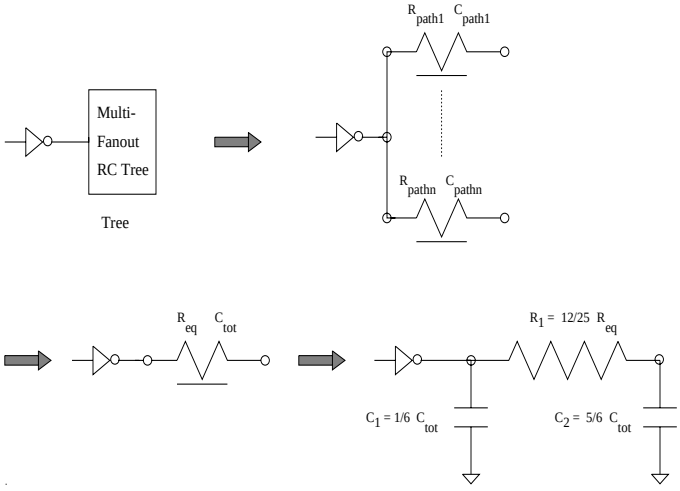

Figure 12: An open-ended *RC* line to capture interconnect trees with multi-fanout at the gate output, and the equiavlent *RC* Π model.

accurate waveform estimation, as shown in Figure 10, with much less computation time.

Example 4: We now consider the same load interconnect topology shown in Figure 9, where each line has inductance equal to $L = 0.246$ $nH/\mu m$ and all other parameters are as before. The actual response at the gate output is computed by using the SPICE LTRA (Lossy TRAnsmission Line Model) for each interconnect in the tree. The responses for the lumped capacitance model, open-ended *RLC* line model, and *RLC* Π model are plotted in Figure 11. The figure shows that both the "open-ended" line model and our Π model approximate the actual response very closely, even for distributed *RLC* interconnects.

Interconnection Trees with Multi-Fanout at Gate Output

Thus far, we have considered only single-fanout interconnect trees. When the interconnect topology has fanout greater than one at the gate output, using total resistance of the interconnect topology in the Π model yields optimistic delay estimates. Since the actual interconnect resistance acting as a shield is much less than the total interconnect resistance. To model multi-fanout interconnect trees (at the gate output) we have considered two solutions. The first solution replaces the total interconnect resistance in the open-ended *RC*/*RLC* line model with an *equivalent* resistance of the total interconnect tree using series/parallel resistance formulas. However, the capacitance is still equal to the total sum of all interconnect capacitances and discrete capacitances. As the computation complexity for calculating the equivalent tree resistance could be quite high, we also found the following approximate method. We replace each parallel path (or subtree) at the output with an open-ended *RC*/*RLC* line, whose resistance (inductance) is equal to the total resistance (inductance) R_{path} (L_{path}) of that subtree. The resulting parallel open-ended *RC*/*RLC* lines at the gate output can be further reduced to a single open-ended line with resistance equivalent to all parallel path resistances, i.e.,

$$R_{eq} = R_{path1}||R_{path2}||\ldots||R_{pathn}$$

The Π model parameters can again be derived using R_{eq} and C_{tot} as the resistance and capacitance of the open-ended line. As shown in Figure 12, only the resistance of the Π model changes, i.e., $R_1 = \frac{12R_{eq}}{25}$.

	50% Threshold delays (ns)				80% Threshold delays (ns)			
	SPICE URC model	Lumped Cap. model	Open-ended Line model	Π model	SPICE URC model	Lumped Cap. model	Open-ended Line model	Π model
Ex1	0.20	0.81	0.21	0.27	0.39	1.20	0.33	0.38
Ex2	1.54	3.63	1.43	1.59	4.05	5.54	2.23	2.20
Ex3	1.47	3.63	1.43	1.59	2.95	5.54	2.23	2.20
Ex4*	1.18	3.64	0.98	1.48	1.80	5.54	1.09	1.94
Ex5	2.35	2.95	2.55	2.55	3.95	4.35	4.09	4.09

Table 2: A comparison of threshold delays for the five example load interconnect trees using SPICE3e URC (Uniform distributed *RC*) model, lumped capacitance model, open-ended line model, and our new Π model. *In Example 4, the actual response is computed using SPICE LTRA model.

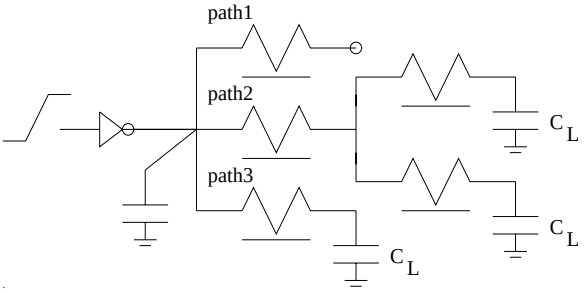

Figure 13: An interconnection topology with fanout equal to three. All the interconnects are identical with parameters $R = 0.25\ \Omega/\mu m$, and $C = 0.015\ fF/\mu m$, and all load and discrete capacitors $= 10\ fF$. The length of all interconnects is 8 *mm*.

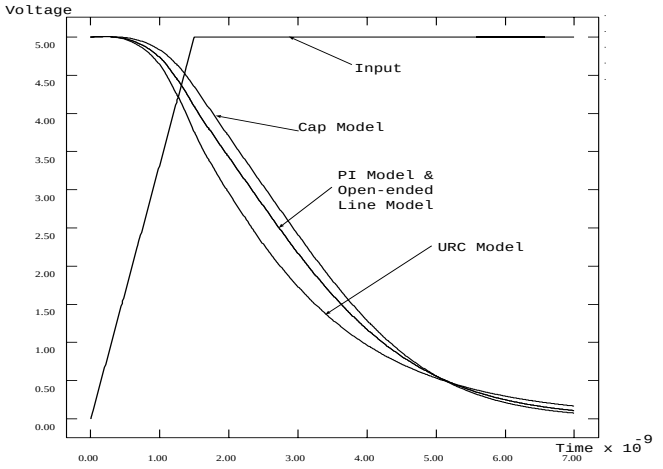

Figure 14: The response waveform at the inverter output for the interconnect tree with fanout equal to three in Figure 13, corresponding to Example 5.

Example 5: To illustrate the multi-fanout effect at the gate output, we consider the interconnect tree topology shown in Figure 13. The length and width of the transistors in the driver are $1\mu m$ and $4\mu m$. The response waveform for this example is shown in Figure 14; again, the "open-ended *RC* Π model" yields a fairly accurate response.

All of the above examples show that the "open-ended *RC* Π model" can capture delay with reasonable accuracy. However, the overall wave shape is not captured beyond the 80% threshold limit. The output fall time can be estimated by interpolating the slope region between the 90% and the 50% or 80% threshold point. The "open-ended *RC* Π model" can thus be used to estimate the gate delay and rise time, with estimates clearly better than the lumped capacitance model. A comparison of threshold delays between various models is given in Table 2. For the example interconnect trees studied, the gate delays and the rise times computed using our new model are within 25% of SPICE-computed values. On the other hand, the simple lumped capacitance based delay estimates are off by as much as 150%.

6 Conclusions

We have presented a new, efficient and accurate technique for modeling *RC* and *RLC* load interconnect trees at the output of a gate. Our Π model parameters depend only on total interconnect tree resistance, inductance and capacitance values. For the various interconnect topologies studied the gate delay and the rise time are within 25% of SPICE-computed values. Our model can be used in place of the recursive Π model used in the "effective load capacitance" formula [7] to reduce the modeling time complexity. We are currently extending our open-ended line model to separately consider the effects of interconnect capacitances and discrete/load capacitances.

REFERENCES

[1] A. B. Kahng and S. Muddu, "Two-pole Analysis of Interconnection Trees", *Proc. IEEE MCMC Conf.*, January 1995, pp. 105-110.

[2] A. B. Kahng and S. Muddu, "Efficient Analyses and Models of VLSI and MCM Interconnects", *UCLA CS Dept. TR-950033*, August 1995.

[3] S. P. McCormick, "Modeling and Simulation of VLSI Interconnections with Moments", *PhD Thesis*, MIT, June 1989.

[4] P. R. O'Brien and T. L. Savarino, "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation", *Proc. IEEE ICCAD*, 1989, pp. 512-515.

[5] P. R. O'Brien and T. L. Savarino, "Efficient On-Chip Delay Estimation for Leaky Models of Multiple-Source Nets", *Proc. IEEE Custom Integrated Circuits Conf.*, 1990, pp. 9.6.1-9.6.4.

[6] L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis", *IEEE Trans. on CAD*, April 1990, pp. 352-366.

[7] J. Qian, S. Pullela, and L. Pillage, "Modeling the "Effective Capacitance" for the *RC* Interconnect of CMOS gates", *IEEE Trans. on CAD*, December 1994, pp. 1526-1535.

[8] J. Rubinstein, P. Penfield and M. A. Horowitz, "Signal Delay in RC Tree Networks", *IEEE Trans. on CAD*, July 1983, pp. 202-211.

[9] C. Ratzlaff, S. Pullela, and L. Pillage, "Modeling the *RC* Interconnect effects in a Hierarchical Timing Analyzer", *Proc. IEEE Custom Integrated Circuits Conference*, May 1992, pp. 15.6.1-15.6.4.

[10] M. Sriram and S. M. Kang, "Fast Approximation of the Transient Response of Lossy Transmission Line Trees", *Proc. 30th ACM/IEEE Design Automation Conf.*, June 1993, pp. 691-696.

[11] Synopsys, "Design Compiler Family Reference Manual", version 3.3a, March 1995.