# A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping

Invited Paper

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## ABSTRACT

In recent years, several open-source projects have shown potential to serve a future technology commons for EDA and design prototyping. This paper examines how open-source and proprietary EDA technologies will inevitably take on complementary roles within a future technology commons. Proprietary EDA technologies offer numerous benefits that will endure, including (i) exceptional technology and engineering; (ii) ever-increasing importance in design-based equivalent scaling and the overall semiconductor value chain; and (iii) well-established commercial and partner relationships. On the other hand, proprietary EDA technologies face challenges that will also endure, including (i) inability to pursue directions such as massive leverage of cloud compute, extreme reduction of turnaround times, or "free tools"; and (ii) difficulty in evolving and addressing new applications and markets. By contrast, open-source EDA technologies offer benefits that include (i) the capability to serve as a friction-free, democratized platform for education and future workforce development (i.e., as a platform for EDA research, and as a means of teaching / training both designers and EDA developers with public code); and (ii) addressing the needs of underserved, non-enterprise account markets (e.g., older nodes, research flows, cost-sensitive IoT, new devices and integrations, system-design-technology pathfinding). This said, open-source will always face challenges such as sustainability, governance, and how to achieve critical mass and critical quality. The paper will conclude with key directions and synergies for open-source and proprietary EDA within an EDA Commons for education and prototyping.

## CCS CONCEPTS

• **Hardware → Electronic design automation**.

## KEYWORDS

Open-source, EDA, Hardware prototyping, VLSI design

**ACM Reference Format:**
Andrew B. Kahng. 2022. A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping: Invited Paper. In *ICCAD'22: IEEE/ACM 2022 International Conference On Computer Aided Design, October 30–November 03, 2022, San Diego, CA.* ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3508352.3561378


*ICCAD'22, October 30–November 03, 2022, San Diego, CA*

ACM ISBN 978-1-4503-9217-4/22/10…$15.00
https://doi.org/10.1145/3508352.3561378

## 1 INTRODUCTION AND BACKGROUND

For well over a decade, the semiconductor industry has witnessed a growing crisis of design. Design costs for a leading-edge system-on-chip are now in the range of $100M to $1B, with design teams routinely having thousands of engineers. Innovators are increasingly unable to evaluate their ideas in terms of silicon realization metrics (PPAC, SWaP) due to barriers of cost, expertise and risk. This is compounded by today's unprecedented diversity of architecture, device, process and integration technology options that must be holistically comprehended for product success.

Cost of design was called out as an existential threat to semiconductor scaling in the 2001 and subsequent editions of the ITRS roadmap [9]. Creation of the DARPA IDEA (Intelligent Design of Electronic Assets) and POSH (Public Open-Source Hardware) programs, part of the 2017 Electronics Resurgence Initiative (ERI), was "driven by this question: Can we dramatically lower the time and complexity required to design modern SoCs, and unleash a new era of circuit and system specialization?" [31]. The ERI itself made its "Page 3 Investments" with reference to scaling barriers already envisioned by Moore in 1965 [21].

In the context of scaling, the role of EDA technology, which enables *design-based equivalent scaling*, cannot be ignored. Whether by reducing design schedule, or by improving power, performance, area and cost (PPAC) outcomes, EDA contributes heavily to the "one week is one percent" trajectory of value scaling that is Moore's Law.[1] Importantly, turnaround time reduction brings a virtuous cycle: more design iterations enable more comprehensive design space exploration and better QoR within a prescribed design schedule [14]. *Open-source EDA* can complement proprietary EDA [4] by bringing added benefits such as customizability, scalability, accessibility, and democratization of design [17].

Tumeo [23] describes the *Open Hardware Technology Commons* (OHTC), as an "open and extensible portfolio of composable and interoperable hardware, software, design automation, and architecture design tools" that enables rapid prototyping of specialized systems in an era of domain specialization (see Figure 1). The OHTC is envisioned as a capability that bridges the ("lab-to-fab") "valley of death" and thereby unlocks barriers to hardware system innovation. The *EDA Commons* discussed in this paper is integral to the OHTC, providing (nation-scale, secure, cloud-based) design infrastructure that spans circuit design/architectures, EDA tools, and design libraries to serve researchers, educators, small and mid-size enterprises (SMEs), and other stakeholders.[2]

[1] At 3nm, more than half of the benefit seen in the new foundry technology is achieved through design-technology co-optimization (DTCO), and this portion is expected to continue increasing [22].

[2] In [23], the OHTC is described as an on-ramp to the *National Semiconductor Technology Center*, a U.S. NIST-funded component of the CHIPS and Science Act of 2022 [30]. However, the present discussion deals *generically* with potential roles of proprietary

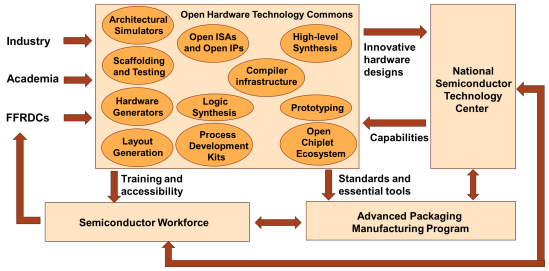


**Figure 1: Nature and role of an Open Hardware Technology Commons [23]. (FFRDC = Federally Funded R&D Center.)**

**Definitions.** The discussion below uses the following terminology.

- *Open-source EDA* refers to EDA tools that satisfy the definition of *open source*, i.e., code that is released publicly under a recognized open-source license.[3] As described in [2], open-source code is freely usable, freely modifiable, and shareable; an open-source license generally permits free redistribution, creation of derived works, and use by anyone for any purpose, in a technology-neutral manner. *Permissive* open-source licenses include BSD, MIT and Apache2.0. *Share-alike* licenses such as GPL-2 or GPL-3 are "copyleft" in nature: derivative works must be distributed under the same or equivalent license terms, which is often an immediate showstopper for adoption in industry.
- *Proprietary EDA* refers to the design automation tools offered by suppliers (e.g., Synopsys, Cadence and Siemens EDA) in the electronic system design industry [33]. Throughout the industry, it is standard for end-user license agreements to include provisions for (i) non-disclosure of (confidential) documentation, command languages and reports; (ii) no benchmarking; (iii) no reverse-engineering; and (iv) duty to comply with export control regulations. These provisions, along with (v) no usage for commercial purposes, apply to all usage by university students, teachers and researchers under the respective suppliers' academic/university programs.
- *Commons* refers to "resources belonging to or affecting the whole of a community."[4] The concept of a "commons" is often used in the context of *the tragedy of the commons*, a "social and political problem in which each individual is incentivized to act in a way that will ultimately be harmful to all individuals". The tragedy of the commons "leads to overconsumption, under investment, and ultimately depletion of a common pool resource."[5] This is relevant when root-causing the depletion of a given technology base or available workforce – e.g., for EDA.

**This Paper.** This paper discusses how open-source and proprietary EDA technologies complement each other, and are both required, in an *EDA Commons* that broadly aims to accelerate hardware system innovation. Section 2 reviews the desired roles and capability of an EDA Commons. Section 3 reviews respective strengths and roles of open-source and proprietary EDA tooling in an EDA Commons. Section 4 gives examples for which open-source EDA has distinct advantages over proprietary EDA in the EDA Commons context. Section 5 gives concluding thoughts.

## 2 EDA COMMONS: ROLE AND CAPABILITY

Over the past year or so, discussions of an EDA Commons have been motivated by the need to remove roadblocks to VLSI design training and innovation. The discussions have converged on several thematic elements.

- An EDA Commons should be a nation-scale shared infrastructure whose setup and maintenance costs are amortized across multiple purposes and stakeholders that span research, education and workforce development, government agencies, and needs of small and medium enterprises (SMEs).
- It should be secure and cloud-based to enable scalability and turnkey access, multi-party collaboration, and control and safeguarding of IP.
- It should offer access to leading-edge EDA tools, PDKs (foundry nodes) and IPs to accelerate hardware design and system innovation – particularly by academic groups and SMEs who seek to accelerate the "lab-to-fab" transition.
- It should offer sharable curriculum and modular, scalable training to broadly engage a next generation – thus opening up the front end of the VLSI design engineering and innovation pipeline – and to upskill the existing workforce.

An EDA Commons also serves higher-level, nation-scale goals such as (i) restoring low-cost (i.e., democratized) access to silicon prototyping that is needed to prove out innovative ideas; (ii) increasing the population of trained VLSI designers who are "tall and broad", with tapeout experience and ability to reason about full system problems so that they can innovate across the technology-hardware-software stack; and (iii) reversing decades-long migrations (e.g., semiconductor manufacturing capacity and supply chains) and declines (e.g., electrical engineering majors and students enrolled in VLSI courses).[6]

At the same time, it will be difficult for an EDA Commons to provide "all things to all people": licenses, compute, system maintenance, design and methodology services, helpdesk, labs and courseware, licensed IP, shuttle access, and more. Identification and root-causing of the problems that need to be solved, resourcing of viable solutions, a long-term sustaining model, and hitting meaningful target metrics on schedule will be crucial to any realization of an EDA Commons.

## 3 ROLES OF OPEN-SOURCE AND PROPRIETARY EDA

Table 1 contrasts the respective strengths of open-source and proprietary EDA technologies, and shows how the two complement each other. The table lists technology, support and sustainability as criteria where proprietary EDA dominates open-source EDA. On the other hand, open-source EDA has clear advantages when it

and open-source EDA in an EDA Commons. To the extent possible, the discussion remains orthogonal to any specifics of "CHIPS Act" components [37] [39] [32] or analogous initiatives worldwide [35] [38]: in all of these contexts, an EDA Commons would serve similar purposes and be similarly framed.

[3]Thus, code released without a license, or released with ad hoc conditions such as "for research purposes only", "for use by academic institutions only", or "if you wish to use this code commercially, contact the technology transfer office of University X" is *not* open source.

[4]https://www.google.com/search?q=commons+definition. Accessed September 3, 2022.

[5]Investopedia, https://www.investopedia.com/terms/t/tragedy-of-the-commons.asp. Accessed September 1, 2022.

[6]How far low-cost tapeout (as in the past days of MOSIS, and present-day ITRI, EuroPractice, CMC, etc.), cloud access to leading-edge EDA and design enablement, and shared courseware will move the needle is an open question. There is some risk of "cargo cult", as factors such as STEM foundations, societal norms for training and work culture, the cachet of hardware versus software career tracks, and even the availability of long-term research funding will all affect outcomes.

comes to extensibility (clone and edit the code), accessibility (free and permissive open source), and scalability (zero per-copy cost).[7] Each has its own type of "ecosystem" that brings unique strengths, and each can enable critical workforce development in unique ways. Some additional commentary on open source vs. proprietary contrasts is as follows.

**Table 1: Strengths of open-source EDA and proprietary EDA with respect to various criteria.**

| Criterion | Open-Source | Proprietary |
|---|---|---|
| Technology | | + |
| Support | | + |
| Sustainability | | + |
| Extensibility | + | |
| Accessibility | + | |
| Scalability | + | |
| Workforce Dev | + | + |
| Ecosystem | + | + |

**Technology.** Proprietary EDA technology – the result of tens of billions of dollars in R&D investment – is central to an EDA Commons. For advanced prototyping of circuits and systems, particularly in the analog/RF domain and for performance signoffs, only foundry-qualified proprietary tools can correctly synthesize and/or analyze designs in advanced nodes. Proprietary EDA tools are also well-tested by decades of use, thousands of customers, and tens of thousands of tapeouts.[8]

Proprietary EDA has also seen "hyperoptimization" of essentially the same tool architectures for over 20 years [16]. This enables tools to extract the best possible quality of results from a given foundry technology and design enablement – which matches the needs of EDA Commons users (e.g., SMEs and researchers) who seek to push the envelope of system realization in advanced foundry nodes.[9] By contrast, open-source EDA is less mature, and has focused on orthogonal objectives such as (i) extreme automation (e.g., 24-hour, no-human-in-the-loop generation of manufacturable layout, aka Silicon Compilers 2.0), (ii) enablement and application of machine learning, and (iii) development of *cloud-scalable* tool architectures and heuristic optimization strategies.

**Support.** Commercial EDA vendors have strong in-house support mechanisms that include user portals, hotlines, application engineers, training classes, and more. However, these have been optimized for large customers, with other types of users (e.g., government labs and small startups) being somewhat underserved [18]. In an EDA Commons, scaling proprietary EDA support mechanisms to much larger and more diverse user populations of teachers, students, government labs and SMEs may require new frameworks and/or outsourcing solutions. Open-source EDA tools enjoy an ethos of community and the ability for users to openly share tool issues, insights and fixes. This may make open-source EDA better suited and more scalable to some of the outreach, education and training functions in an EDA Commons.

**Ecosystem.** Proprietary EDA vendors participate in foundry-specific ecosystems and IP ecosystems, typically alongside IP providers, customers and consortia. This enables the delivery of design enablement and node-to-node scaling via co-development and design-technology co-optimization. Open-source EDA today has a different ecosystem that spans open hardware designers, contributors that include both developers and users, VLSI design educators, and diversity and outreach proponents. Growth of this ecosystem gains momentum from the stream of open-sourced IPs (RISC-V), open-sourced foundry PDKs (GlobalFoundries 180MCU and SkyWater 90FDSOI), and initiatives such as the PICO or Google-SkyWater tapeout sponsorships. It seems inevitable that as open-source EDA improves, it will gain user-driven foundry support (kits, qualification, PDK access) and even interfaces to proprietary EDA, such that the two ecosystems grow closer together and better serve EDA Commons goals.

**Workforce Development.** Both proprietary EDA and open-source EDA engage actively with VLSI design educators, trainers, and researchers [5] [25] [16]. Open-source EDA metrics such as number of VLSI tapeout classes and design boot camps, and number of research papers based on open-source tooling, have increased markedly over the past two years.

Workforce development must not overlook the critical need for an *EDA R&D workforce*. Nonlinear, quantum-leap innovations in semiconductor-based design cannot happen without corresponding innovations in EDA: a next generation of EDA R&D engineers is required. Moreover, if VLSI design workforce development and innovation are successfully accelerated as a result of EDA Commons and OHTC-like efforts, there will be more users and applications of EDA technology; these will require a larger EDA workforce.[10]

Finally, Figure 2 places EDA Commons needs along the continuum between open-source EDA and proprietary EDA. The figure suggests that, e.g., "job-readiness" at a design house may be best served by training on proprietary EDA tools, while pathfinding research for chiplet-based systems may require adaptation of open-source EDA tools. In general, openness, interoperability, public calibrations, and futures [11] match well to open source. The next section expands upon several specific needs that are better served by open-source EDA.

## 4 UNIQUE BENEFITS OF OPEN-SOURCE EDA

Potential benefits of open-source EDA – spanning research, teaching, workforce development, and underserved and future design needs – have been reviewed in, e.g., [12] [13] [16]. This section gives three examples of differentiated benefits provided by open-source EDA in the context of an EDA Commons: (i) simplified access for education and workforce development; (ii) design infrastructure for future needs; and (iii) unblocking of teaching and research related to machine learning for IC design and EDA.

[7] A recent European Commission staff working document [36] notes that "Open source tools are essential for introducing new companies and more developers into the field" – and that the EC "has proposed to invest in a European open source EDA tooling ecosystem".

[8] In his position statement at the DAC-2022 "What is the Future for Open-Source EDA?" panel [40], Dr. Charles Alpert of Cadence proposed a "10,000 tape-outs rule": "an EDA tool cannot be a fully robust and complete product until it has participated in 10,000 tape-outs".

[9] At the same time, years of incremental hyperoptimization have also led to (i) complexity, with 10000+ command-option combinations available in a modern place-and-route tool, and (ii) perpetuation of 1980s-vintage tool architectures, data structures and algorithms. The high cost of R&D additionally results in (iii) tool development that responds only to established market demands.

[10] While a trainee for circuit design R&D will need to work with proprietary EDA tools, a trainee for EDA R&D will need to work with open-source tools in order to understand software engineering, tool architecture, algorithms, performance optimization, etc. by the time they enter the workforce. At the DAC-2022 panel [40], Dr. Charles Alpert commented that this training could save two years of the learning curve inside an EDA R&D organization.

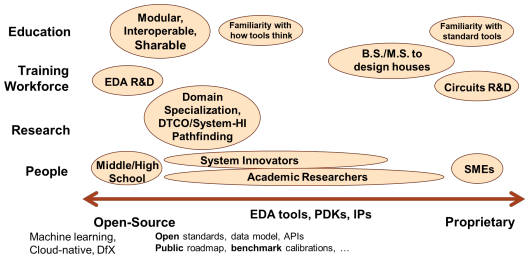


**Figure 2: Needs of education, training of designers and R&D engineers, stakeholders and next-generation workforce pipeline cohorts – placed along the continuum between open-source EDA and proprietary EDA.**

## 4.1 Free is Increasingly Far from Near-Free

For academic education and research, open-source EDA has only recently made it onto the radar screen.[11] This is largely because proprietary EDA suppliers, via their university programs, have for many years offered near-completely subsidized licenses for educational and research purposes. (E.g., ~$3000 for 300 seats of a vendor's entire EDA portfolio is *near-free* from a license cost standpoint.) And, as noted above, there is no reason for an analog circuits researcher to use anything but proprietary EDA.

The use of proprietary EDA in academia brings overheads that include system administration, server maintenance, budgeting for multiple university program subscriptions (teaching vs. individual research labs and academic units), verifying that users' physical locations comply with WAN or export constraints, reporting to EDA vendors, etc. These overheads present significant barriers for smaller labs and programs. Cloud-hosted licenses in a secure EDA Commons can democratize access to EDA tooling.

A separate consideration is that EDA technology, PDKs, and certain IPs (e.g., from Arm) all bring export control constraints that are now quite complex and fluid (see, e.g., [41]). Proprietary EDA EULAs call out export control compliance along with other limitations: only non-commercial use, no reverse-engineering, no benchmarking, no distribution of documentation or reports, confidentiality provisions, liability for damages, and more. While all of these limitations are perfectly reasonable for companies to impose, they create an *accessibility gap* relative to open-source EDA. In an EDA Commons, access to VLSI design education and initial design experiences will be simpler and more immediate via open-source EDA tooling, as cartooned in Figure 3. Open-source EDA may be preferable as an onramp and for outreach.

## 4.2 Design Infrastructure for Future Needs

Proprietary EDA generally does not provide design infrastructure to address speculative technologies and future design needs. A long-running example of this is EDA for chiplet-based and 3D integration, where capabilities have progressed in very small increments due to lack of incentives for proprietary tools to add new "experimental" capabilities. This is natural: commercial suppliers will not invest in tool development for novel technologies until addressable markets become clear. The consequence of this chicken-egg impasse is that design of proof-of-concept systems using speculative technologies

[11] This has been catalyzed not only by open hardware initiatives [29] [3], but also by pandemic-related distance learning, visa and export control issues.

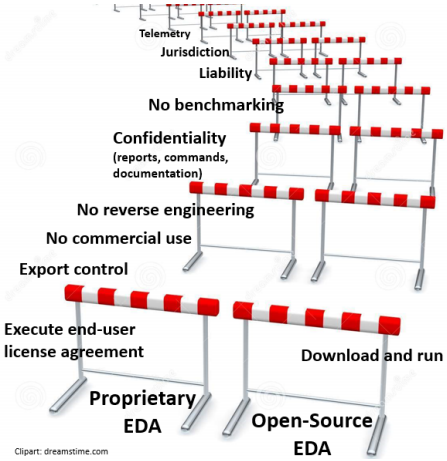


**Figure 3: Hurdles to getting started with proprietary and open-source tools.**

– a mandatory step in the lab-to-fab pathway – is impossible. As a result, valuable innovations may never cross the "valley of death" to reach mass production. Similarly, system-aware *pathfinding* – the early identification of promising (material, device, patterning, integration) technology options and their orchestrated impact on design, architecture and applications – is also impossible. This spoils the value that is ultimately extracted from any base manufacturing and supply chain capability.

To avoid these suboptimal outcomes, an EDA Commons must provide *agile* design infrastructure that can be rapidly modified to support and explore novel technologies and integrations. Proprietary EDA tools are unlikely to serve this need, since they are oriented to established design needs and are not modifiable by users. To accelerate the cycle of innovation, hardware designers and technologists also require new means to rapidly generate probative [8], exploratory design enablements (i.e., proxy PDKs [6] [24], cell libraries, and collaterals such as memory generators).

## 4.3 Unblocking Data and Machine Learning for IC Design and EDA

*Machine learning* (ML) that exploits design experience and data is well-understood as a potential scaling booster for EDA [14]. Recent works such as [19] [20] have spurred interest in ML for EDA. However, users today cannot easily explore ML using proprietary EDA tools: (i) there is a lack of standard reporting formats and tool metrics; (ii) each tool has its own, unique set of parameters by which users change the tool's behaviors and tradeoffs; and (iii) the tremendous fragmentation of names and formats across tool chains and vendors creates a "Tower of Babel" that hampers sharing of ML models and know-how. Tool command sets and reports are copyrighted and confidential, which further blocks ML deployment.

To overcome the "Tower of Babel" and other obstacles, a *METRICS1.0* infrastructure for the EDA and IC design industries was proposed in the late 1990s. METRICS1.0 afforded design organizations with the ability to measure all design activity, mine all data, predict tool outcomes, find sweet spots or field of use for tools, and perform design-specific tuning of tools [7, 15]. A current incarnation, METRICS2.1 [10], is a joint initiative of the OpenROAD project

[27] [1] and the IEEE CEDA Design Automation Technical Committee (DATC) [42]; it provides an open-source standard metrics naming convention, metrics dictionary, and reference JSON-based implementation in the OpenROAD and OpenROAD-flow-scripts platforms [28]. Thousands of RTL-to-GDS metrics datasets along with all configuration files needed for complete reproducibility are public in the DATC's GitHub [26]. This data helps introduce students and researchers to machine learning applications involving IC design. By contrast, publicizing analogous data developed using proprietary EDA tools is forbidden by current end-user license agreements.[12]

## 5 CONCLUSIONS

Future system design innovations will depend on EDA innovations – and a world with more designers and novel semiconductor-based products will require more EDA developers. An *EDA Commons* is envisioned as a multi-faceted, nation-scale infrastructure that will broadly accelerate semiconductor-based research and innovation, entrepreneurship, and education and workforce development. With its focus on design automation technology and design infrastructure, the EDA Commons complements efforts that focus on manufacturing, heterogeneous integration, packaging, system prototyping and other capabilities. For reasons given above, it will necessarily contain a mix of proprietary and open-source EDA technologies.

*Proprietary EDA* brings exceptional design automation technology, methodology and support along with well-established commercial and ecosystem relationships. However, proprietary EDA vendors cannot easily pursue self-disruptive directions such as massive leverage of cloud compute or extreme reductions of turnaround times, and it is also difficult for vendors to speculatively serve new applications before markets are well-defined. Moreover, the industry's (triopoly or duopoly) structure brings a tendency toward closed systems with proprietary interfaces.

*Open-source EDA* complements proprietary EDA by providing a broadly accessible, scalable onramp for education and workforce development. It can serve as a platform for EDA research, and as a means of training both designers and EDA developers with public code. Crucially, while proprietary EDA can be used to train future designers, open-source EDA *must* be used to train future EDA developers. Flexibility and customizability enables open-source EDA to address emerging needs such as system-design-technology pathfinding with speculative technologies. Open source enables standards such as naming and reporting that serves data collection and machine learning; beyond this, it democratizes access to chip design. At the same time, open-source EDA must solve challenges of transition to a sustainable business model [18] [34], governance, and "critical mass and critical quality".

As a "resource belonging to or affecting the whole of a community", an EDA Commons – should it come into existence – deserves attention and support from across the community.

- *Who should it serve?*
- *What must it deliver, and what must it discover – on what timeline?*
- *How will it move the needle, according to what success metrics?*
- *How should it be scoped, funded, governed, staffed, and sustained?*
- *How will it escape the tragedy of "overconsumption, under investment, and ultimately depletion"?*
- *How should open-source and proprietary EDA mix in service of the Commons' goals?*

Realizing an EDA Commons may soon become a real challenge for the EDA and design community. Will we treat it as the opportunity of a lifetime?

[12]It is worth emphasizing that open-source tools can enable true open standards (e.g., naming standards for tool and flow metrics and reporting data) that afford freedom to innovate and interoperate within an ecosystem. This is in contrast to "de facto standards" that can suddenly become closed or litigated, and that waste bandwidth by requiring defensive measures such as [43]. New, open standards to support IC and system design may be needed in a future EDA Commons, and these can flow from open-source EDA.

## 6 ACKNOWLEDGMENTS

Research at UCSD is supported in part by DARPA HR0011-18-2-0032 and by NSF CCF-2112665.

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