Power Delivery Pathfinding for Emerging Die-to-Wafer Integration Technology

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***Abstract*—In advanced technology nodes, emerging die-to-wafer (D2W) integration technology is a promising "More Than Moore" lever for continued scaling of system capability and value. In D2W 3D IC implementation, the power delivery network (PDN) is crucial to meeting design specifications. However, determining the optimal PDN design is nontrivial. On the one hand, to meet the IR drop requirement, denser power mesh is desired. On the other hand, to meet the timing requirement for a high-utilization design, more routing resource should be available for signal routing. Moreover, additional competition between signal routing and power routing is caused by inter-tier vertical interconnects in 3D IC. In this paper, we propose a power delivery *pathfinding* methodology for emerging die-to-wafer integration, which seeks to identify an optimal or near-optimal PDN for a given design and PDN specification. Our pathfinding methodology exploits models for routability and worst IR drop, which helps reduce iterations between PDN design and circuit design in 3D IC implementation. We present validations with real design examples and a 28nm foundry technology.**

I. Introduction

The semiconductor industry has enjoyed tremendous growth and innovation in large part due to the self-fulfilling prophecy of Moore's Law. With foundry 7nm products reaching high-volume production, only a few feasible technology nodes remain to potentially deliver PPAC (power, performance, area, cost) benefits from transistor, cell architecture and leteral scaling. The past decade has seen three-dimensional integrated circuit (3D IC) stacking technologies emerge as the main hope for future scaling of integration, area footprint and design performance / power envelope. However, conventional *packaging-driven* 3D IC integration technologies with through-silicon vias (TSVs) are limited by TSV size and pitch, which constrains achievable vertical integration density [1].

Multiple *foundry-driven* 3D integration technologies have recently emerged as viable solutions with significant PPAC benefits; these include high-precision face-to-face (F2F) wafer-on-wafer (WoW) and die-to-wafer (D2W) stacking [6][19]. WoW technology is more tailored towards power / performance / area improvement, whereas D2W aims to provide more cost-effective integration while also providing system-level power / performance improvements, e.g., for memory-on-logic, single-chip solutions, etc. WoW faces two key limitations compared to D2W technology: (1) same area constraint for top and bottom dies, which limits partitioning scenarios, and (2) lack of commercial EDA support. On the other hand, in D2W technology existing 2D IPs are partitioned across multiple dies (e.g., a large bottom die and various-sized smaller top dies). Hence, there is no need for special 3D EDA support in the D2W regime. This flexibility, coupled with relatively high integration density, has made D2W technology a practical solution to cope with 2D scaling challenges.

Power delivery network (PDN) is an integral aspect of physical design that directly affects reliability and functionality of product designs. With increasing power density and complexities from multiple voltage domains in modern designs, determining a high-quality PDN is challenging even in 2D ICs. The challenges are exacerbated in 3D ICs with additional resistance between the power supply and transistors in different tiers. Further, inter-tier *vertical interconnects* (VIs) must support both signal and power / ground routing, which limits feasible integration. Also, as VIs become smaller to support higher integration densities, they become more resistive, with adverse effects on PDN quality [21][22]. To achieve robust functionality, 3D IC designs must mitigate and balance these PDN-related challenges. This demands an efficient, accurate design space exploration (aka *pathfinding*) methodology that – given various technology- and design-dependent parameters – can quickly provide quality of result (QoR) tradeoffs of various PDN solutions.

In this work, we present an efficient pathfinding methodology for PDN design of emerging D2W-based designs. We build an IR drop model to predict the worst IR (WIR) drop of a given PDN configuration. To comprehend the effect of a given PDN solution on overall design QoR, we also develop a routability model which predicts the routability of a design given a PDN configuration. Putting these elements together, our pathfinding methodology first filters out PDN configurations based on a given design's prescribed IR drop limits; then, the routability model is used to identify the IR drop-feasible PDN configuration(s) that offer best routability. We thus obtain a high-quality, satisfying PDN solution that is "optimal" in the sense of both predicted IR drop and estimated routability within our modeled PDN design space. The PDN solution offers direct benefits to design QoR and ease of implementation. Our main contributions are as follows.

- We study the impact of VI density on design routability and build a VI-aware routability model.
- We propose an interface to properly combine IR drop analysis of PDN configurations and corresponding impact on routability.

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- On a 28nm design, our model identifies a PDN in the top-3 out of 256 possibilities.
- To the best of our knowledge, we are the first to propose such a pathfinding methodology to identify optimal PDN configurations for D2W-based designs.

II. Related Work

Several design methodologies using existing commercial 2D CAD tools have been proposed for physical implementation of gate-level 3D ICs [3][10][12][14][11]. The Shrunk2D (S2D) flow [12][14] performs gate-level 3D IC implementation, while the subsequent Cascade2D flow implements both gate-level and block-level monolithic 3D IC [3]. (Cascade2D focuses on monolithic 3D (face-to-back, or F2B) and does not support F2F bonding technology.) Recently, a commercial-quality F2F-bonded 3D IC implementation flow Compact-2D (C2D) has been proposed [11]. These 3D works leave open the issue of power delivery and routability interactions.

Power delivery in gate-level 3D ICs is considered in [13], which proposes a PDN-centered tier-partitioning technique that comprehends the IR drop vs. thermal tradeoff in monolithic 3D IC. [17] analyzes full-chip impact of PDN designs in monolithic 3D ICs. Optimized 3D PDN design configurations (in six categories) are compared across power, performance, IR drop and wirelength metrics in different technology nodes. However, design-specific PDN choices at the "Pareto frontier" of IR drop vs. routability are not addressed, as this would require exploration of PDN structures with degrees of freedom on each metal layer. [4] develops a system-level PDN model, along with static as well as dynamic frequency and time domain analyses. 2D and 3D ICs with extracted equivalent RLC parasitics are compared using a single baseline PDN structure. The focus is on dynamic rail analysis with frequency-related environmental differences (e.g., decap insertion) rather than PDN optimization.

"PROBE" [8] gives a methodology to rank BEOL stack options according to an intrinsic routing capacity; we use a routability characterization technique from [8]. Additional works have studied the issue of vertical cuts (interconnect demands) in gate-level 3D IC implementation - e.g., attempting to maximize the benefits of 3D ICs by increasing the number of monolithic inter-tier vias (MIVs) or face-to-face VIs [11][12]. [16] notes that as the number of vertical cuts increases, inter-die coupling capacitance increases, significantly affecting power and signal integrity in F2F bonded ICs.

The need for PDN pathfinding in 3D IC arises because power/ground delivery is far from "free": in the D2W regime, there are TSV and routability impacts, as well as a need for the PDN solution to support delivery of power/ground and signal through inter-tier VIs. The number of VIs is a significant determinant of power and signal integrity, in light of routing congestion and IR drop. This is in contrast to PDNs in 2D ICs, which are generally less sensitive to signal routing congestion on upper metal layers.[1] While previous studies of 3D IC implementation have illuminated many aspects of partitioning, place-and-route and power delivery, typically only a very limited PDN solution space is considered. We attempt to close this gap by explicitly considering both IR drop and routability.

[1]If the total number of VIs is high relative to the total number of nets (i.e., #VIs-to-#nets ratio), this means that the number of 3D nets across the VIs located on the top metal layer is also relatively high. Therefore, it is also essential to consider the impact of VIs (induced by a given design partition across tiers) when designing a PDN.

III. Methodology

A dense PDN can increase wirelength due to routing congestion and detours, and also affect feasibility of VI placement in the top layer of 3D ICs. To achieve a power delivery pathfinding flow that explores possible PDNs for a given design and WIR drop requirement, we develop WIR drop and routability models to filter and rank possible PDN designs.

A. Power Delivery Pathfinding Flow

We define the *power delivery pathfinding* problem as follows.

Power Delivery Pathfinding Problem. Given a placed circuit design with known cell and VI locations, provide a PDN design that meets the IR drop limit with best routability.
Inputs: Placed design, VI locations and BEOL stack.
Output: PDN with best routability meeting the IR drop limit.
Constraints: WIR drop and technology (design rules).

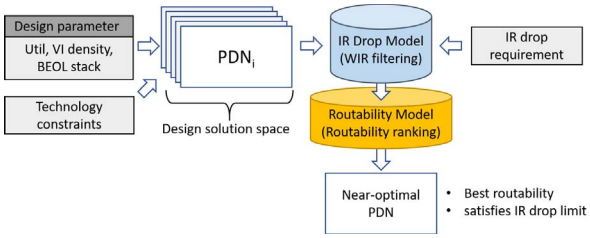

Fig. 1. Model-based PDN pathfinding flow which gives the optimal PDN design considering both IR drop requirement and routability requirement.

Figure 1 illustrates our power delivery pathfinding flow. The PDN design solution is enumerated by technology constraints (width, space and pitch) of each power metal stripe. For the enumerated PDN designs, we apply the IR drop model to predict their respective WIR values, and find PDN designs which satisfy the WIR requirement. We then use our routability model to rank PDN designs based on their routability. Besides the PDN variables including metal width, spacing and pitch, we also consider utilization and VI density of the design in the routability model, so as to comprehend the competition for routing resources between PDN and signal routing. Based on the IR drop and routability models, our flow returns a PDN design which satisfies the WIR constraint, and has the best routability. This PDN solution will provide the highest probability of a clean 3D IC implementation.

B. PDN Design Knobs

To explore the PDN design space, we use the PDN design knobs in Table I. Circuit design-independent knobs include width, space and pitch size of metal stripe as shown in Figure 2. Combinations of these knobs must satisfy the design rule constraints of the given technology. For a given 3D IC design, we use the number of cell instances, row utilization and VI density as circuit design-dependent knobs.

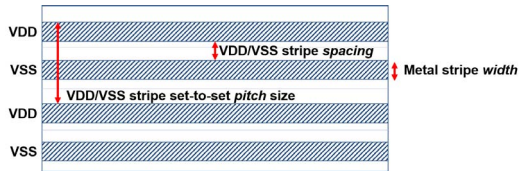

Fig. 2. Illustration of circuit design-independent PDN design knobs.

TABLE I
PDN DESIGN KNOBS.

Circuit design-independent knobs	
Metal stripe *width* (*w*)	Width of PDN stripe for each layer
VDD/VSS stripe set-to-set *pitch* size (*p*)	Set-to-set distance of VDD/VSS PDN stripe for each layer
VDD/VSS stripe *spacing* (*s*)	Spacing between VDD/VSS PDN stripe for each layer
Circuit design-dependent knobs	
#Instances	Instances in one tier of 3D IC
Utilization	Row utilization of circuit
VI density	The ratio of #VIs to #nets

C. WIR & Routability Modeling

We use nonlinear learning-based algorithms such as multivariable linear regression, and multivariate adaptive regression splines (MARS) [7] to build regression models for both WIR and routability.

WIR Modeling. We build a model to predict the WIR drop for a given PDN design. We use the circuit design-independent knobs as inputs of the WIR model. As mentioned in Section III-A, WIR model is built to prune the PDN design solution space by the WIR requirement. Figure 3(a) illustrates the WIR modeling flow. We perform static IR analysis with ANSYS RedHawk [25] to collect WIR data for various PDN designs. We then model WIR with the aforementioned modeling techniques. Finally we use hybrid surrogate modeling [9] to build a combined model for WIR assessment.

Routability Modeling. We build a model to predict the routability for a given circuit design with pre-routed PDN. Similar in spirit to PROBE [8], we measure the routability of a PDN design by the maximum cell swap count, K $threshold$ (K_{th})[2] before exceeding a pre-defined design rule violation (DRV) threshold. To train the model of PDN routability, uniform cell placement is needed for gradually increasing routing difficulty as K value increases. Figure 4(a) illustrates the mesh-like placement in PROBE. We use 3-input AOI cell for mesh-like placement, and the inputs and output of each cell are connected.

A higher K_{th} value implies that the given PDN design has better routability, i.e., more routing capacity. To understand the impact of VIs on routability of a given PDN in the 3D IC context, we extend the mesh-like placement with connections from cell pin to VI pin on the top metal layer as shown in Figure 4(b). We fix the location of VI pins during random swapping of neighboring cells. The number of VIs is determined by VI density as the input parameter, and VI density is defined as #VIs/#nets. The VIs are placed on the top metal and VIs do not overlap the PDN.[3] Each VI is connected to the net of the nearest cell output pin. Figure 3(b) illustrates the routability modeling flow. We perform PROBE-like routability analysis [8] with Innovus [24] to collect K_{th} data for various PDN designs. We then model K_{th} value with the aforementioned modeling techniques. By combining several models (multivariable linear regression and MARS), we achieve a hybrid surrogate model to assess the routability of PDN design. Model validations are discussed in Section IV-D.

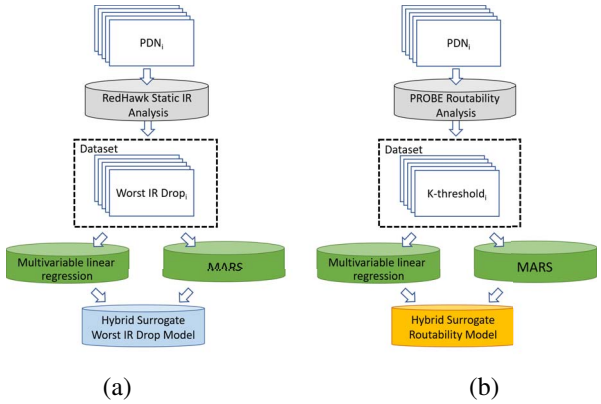

Fig. 3. (a) WIR modeling flow. (b) Routability modeling flow.

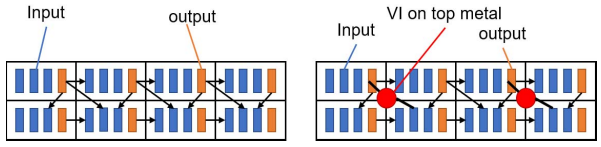

Fig. 4. Illustration of (a) mesh-like placement as in [8], and (b) our 3D mesh-like placement with VIs.

We use both circuit design-independent knobs and circuit design-dependent knobs as inputs to our routability model. We use the routability model to sort all PDN designs that satisfy the WIR requirement in order to find the optimal PDN.

It is important to rank the relative routability by the K_{th} value over the absolute value of K_{th} predicted through regression. Thus, not only the linearity expressed by the Pearson correlation coefficient [15] but also the ranking comparison by each K_{th} is required. We use the Spearman's rank correlation coefficient [18] to compare the routability ranking of PDNs with predicted K_{th} values with the ranking of PDNs with real K_{th} values obtained experimentally from PROBE-like analyses. In general, there is a strong correlation when the coefficient between the two ranking groups is ≥ 0.9.

IV. EXPERIMENTS

In this section, we describe our experimental setup and results. We perform experiments with an 8-track 28nm FDSOI foundry enablement and row utilization determined by the number of available cell rows. For example, 8 rows of cells and 3 rows of white space implies a row utilization of 0.727.[4] For PROBE-like routability study, we perform place-and-route

[2]The K value indicates number of neighbor-swaps normalized to the total number of instances for a given placement, and K_{th} is the minimum K value when routing fails. Following [8], we define routing failure as #DRVs > 150. We refer readers to [8] for more details.

[3]Note that to implement routing by a commercial 2D P&R tool during the experiment, the VIs in the routability model are placed as I/O pins.

[4]For ease of use, the values of the following utilizations are rounded to the first decimal place.

using *Cadence Innovus Implementation System v18.10* [24]. For IR drop study, we perform static IR analysis using *ANSYS RedHawk v15.1.1* [25]. Table II shows the reference design we use for our experiments. For each model, we use 67% of the overall dataset for training and the remaining 33% of the dataset for testing. We use a MARS implementation in Python3 from the Py-earth package [20]. The following discussion reviews our (i) scalability study; (ii) sensitivity study; (iii) IR drop model; (iv) routability model; and (v) verification on real designs.

TABLE II
REFERENCE DESIGN OF PDN.

PDN design				
Metal layer	**Direction**	***width*** (μm)	***spacing*** (μm)	***pitch*** (μm)
M2	H	Standard cell power rails		
M3	V	0.4	10	20
M4	H	0.4	0.8	12
B1 (M7)	V	8.0	16.0	60
B2 (M8)	H	10.0	20.0	70
Circuit design				
#Insts	25000			
Utilization	0.7			
VI density	0.05			

A. Scalability Study

We study the scalability of our approach by varying design size is described. We perform routability analysis using variations of the reference PDN design.[5] We sweep the number of cells from 25K to 100K with a step size of 25K for a fixed utilization with a total of 24 #PDNs with 75% (small) and 175% (big) design-independent knobs respectively. Results in Figure 5 show that routability decreases as we increase the design size. Although there is a change in the absolute value of K_{th} when design size changes, the routability rank ordering of PDN designs remains the same. Based on the scalability observations, we fix the number of instances = 25K for the reference design in all experiments reported below.

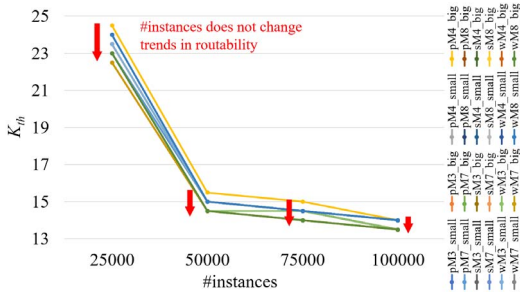

Fig. 5. Routability (K_{th}) versus #Insts reflecting various number of PDNs.

B. Sensitivity Study

To assess the impact of each PDN and circuit design knob on WIR drop and routability, we investigate the sensitivities of worst IR drop and routability to various design knobs discussed in Section III-B. For PDN design knobs, all circuit-independent design knobs of *width*, *spacing* and *pitch* for M3, M4, M7 and M8 are considered. For circuit-dependent design knobs, we consider utilization and VI density. Only one knob is swept at a time while all other knobs are fixed at their values in the reference design. Figure 6 shows the sensitivity results between WIR / routability (y-axis) and PDN density (x-axis) by varying design knobs. The PDN density of each layer is calculated as $2 \times width/pitch$.

***Width*:** We sweep *width* for M3, M4, M7 and M8 from 75% to 175% of the reference value. Figure 6(a) shows the worst IR drop as a function *width* for M4, M7 and M8 separately. Worst IR drop decreases as we increase the *width* since VDD/VSS stripes become less resistive. Figure 6(b) shows routability as a function of *width*. For all layers, routability decreases as *width* increases since less routing resource is available. Moreover, the higher layers show less sensitivity of routability to PDN layer utilization.

***Spacing*:** We sweep the VDD/VSS stripes *spacing* for M3, M4, M7 and M8 from 75% to 175% of the reference value. Since the space between VDD and VSS stripes is mainly used to reduce dynamic IR drop and it does not have a significant effect on static IR drop. The effect of spacing on routability is also negligible.

***Pitch*:** We sweep the M4 VDD/VSS stripe *pitch* for M3, M4, M7 and M8 from 75% to 175% of the reference value. Figure 6(c) shows that worst IR drop increases as we increase *pitch* (i.e., sparser power mesh). Figure 6(d) shows that routability decreases as PDN layer utilization increases. However, there is higher sensitivity to *pitch* than *width*, even with the same PDN layer utilization.

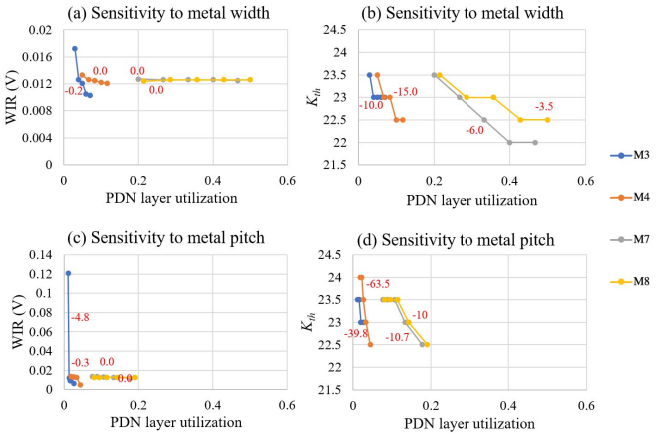

Fig. 6. WIR (left) and routability (right) sensitivity to circuit-independent knobs width (top) and set-to-set pitch (bottom). The red numbers indicate the slope of the K_{th} change with each knob.

Utilization: For our routability study, we use mesh-like placement. Therefore, current density is proportional to utilization in our study. Figure 7(a) shows WIR versus utilization and metal width, while Figure 7(c) shows WIR versus utilization and metal pitch, on M3, M4, M7 and M8. Since IR drop is proportional to current density, which is in turn proportional to utilization in a uniform placement, we see that WIR is proportional to utilization.

Designs with higher utilization tend to have DRVs on lower metal layers due to lack of routing resources for pin access and/or promotion. Therefore, we simultaneously sweep design utilization and metal width (resp. pitch) to study the routability

[5]WIR in 3D IC depends on specific boundary conditions. We experimentally confirm that there is no obvious correlation between #Insts and WIR for a given utilization.

impact of PDN design due to interactions between design utilization and stripe width (resp. pitch). Figure 7(b) shows the routability as a function of utilization and metal width, and Figure 7(d) shows the routability as a function of utilization and metal pitch, on layers M3, M4, M7 and M8. We observe that routability decreases as we increase the utilization. We also observe that for a given utilization, routability is more sensitive to changes in lower metal layers.

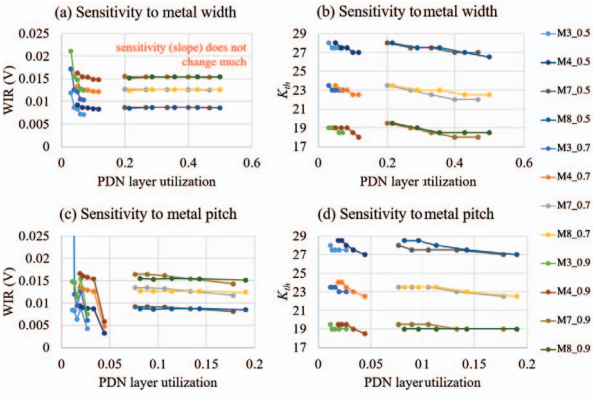

Fig. 7. WIR (left) and routability (right) sensitivity analysis results for circuit-independent knobs width (top) and set-to-set pitch (bottom) with various utilizations.

VI density: We sweep the VI density from 0.025 to 0.25. Similar to the utilization sensitivity study, we simultaneously sweep metal width or pitch along with VI density, as VI accessibility intuitively depends more on routing resource on higher metal layer. Since signal VIs are circuit-dependent that affect only routing resources, only the routability analysis is performed.[6] VI density is given in Table III. Figure 8(a) shows the routability as a function of VI density and metal width, and Figure 8(b) shows the routability as a function of VI density and metal pitch. We observe that routability suddenly decreases as we increase the VI density. Moreover, for a given VI density, routability is more sensitive to changes in higher metal layers, as we might expect.

TABLE III
SENSITIVITY TO VI DENSITIES (#NETS = 25172).

Target VI density	#VIs	VI density
0.025	684	0.027
0.05	1242	0.049
0.075	2052	0.082
0.01	2736	0.011
0.025	6266	0.025

C. IR Drop Model

To efficiently assess whether a PDN design satisfies the worst IR drop requirement, we build an IR drop model based on a dataset which includes combinations of knob values from *width*, *pitch* and utilization. In our experiment, we sweep the value of each knob from 75% to 125% of its reference value (e.g., 0.3μm to 0.5μm for M3 stripe width). Figure 9(a) shows actual versus predicted WIR for various PDN designs with

[6]There is a slight difference between the target and actual VI density, because the VI should be aligned to the cell grid in mesh-like placement to guarantee the same distance between the VI and the connected net.

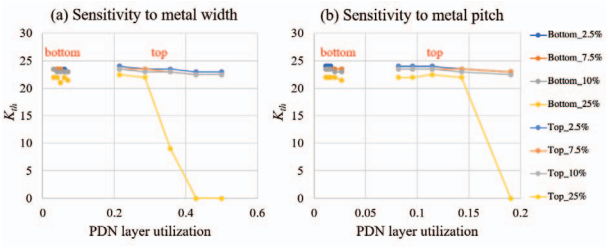

Fig. 8. Routability sensitivity analysis results for circuit-independent knobs (a) width and (b) set-to-set pitch with various VI densities.

combinations of PDN design knob values. Our model achieves an absolute average error of 4.02mV (resp. 4.05mV) for the training (resp. testing) dataset.

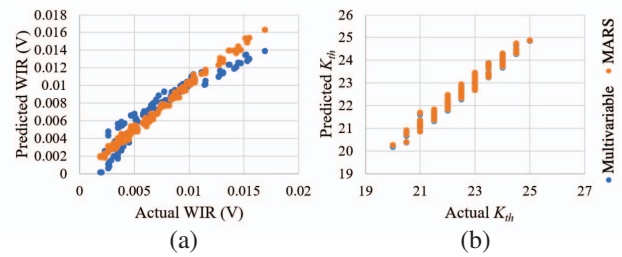

Fig. 9. Modeling results: (a) WIR model and (b) Routability model.

D. Routability Model

To find an optimal PDN, we must be able to rank PDN designs that satisfy the worst IR drop requirement by routability. We use the same dataset as in Section IV-C to build a routability model. The input of the model is a sequence of PDN design knobs for all metal layers in the BEOL stack, along with circuit design knobs. Figure 9(b) illustrates correlation between actual K_{th} and predicted K_{th} by the routability model.

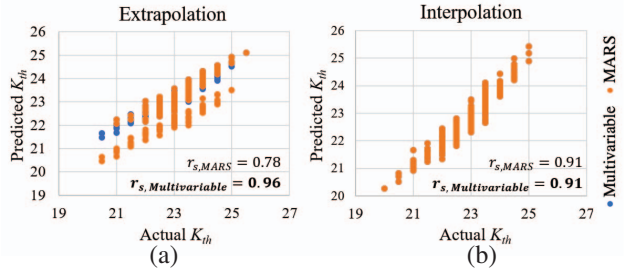

Fig. 10. Correlation of routability between actual K_{th} and predicted K_{th} values of (a) Extrapolation and (b) Interpolation. The scatter points displayed in the graph represent a total of 256 #testing points and a total of 256 #PDNs training points.

To assess the generality of our model, we also build another routability model based on a dataset that is composed of routability data with knob values of {85%, 115%} of its reference value (i.e., a "subset" of the original ({75%, 125%}) dataset). We then test our model in extrapolation case (i.e., from the "subset" to the original dataset) and interpolation case (i.e., from the original dataset to the "subset"). Figures 10(a) and (b) show that we achieve a Spearman's coefficient of 0.96 (resp. 0.91) with multivariable linear regression for extrapolation (resp. interpolation), which suggests that our model can be generalized and used for other testcases via interpolation and extrapolation.

E. Verification of Pathfinding on Real Design

We verify our routing capacity and WIR drop models by applying pathfinding methodology to a real design testcase. We use the AES encryption and JPEG encoder cores from OpenCores [23]. Each design is synthesized with *Synopsys Design Compiler L-2016.03-SP4-1* [26]. We perform experiments with 8-track standard cells from a 28nm FDSOI foundry technology library. Since cells of real designs do not have uniform width as in a mesh-like placement, we perform legalization before routing to eliminate overlap caused by random swapping of neighboring cells. We set a fixed utilization of 0.727 in light of scalability experiments shown in Section IV. To apply the proposed routability model, we add VIs as I/O pins, then place the pins uniformly on the top metal at the VI density used in the model (5% of #VIs/#nets). The additional VIs are connected to the nearest different nets. Without loss of generality, we use the WIR value of the reference PDN design as the IR drop requirement for each testcase. The BEOL stack of the PDN is the same as that of the reference PDN of Table II.

TABLE IV
SIMULATION RESULTS WITH AES AND JPEG TESTCASES, K_{th} VALUES ARE AVERAGES OVER FIVE DENOISING RUNS.

	AES				JPEG			
PDN	**clk (ns)**	**#inst**	K_{th}	**IR drop (V)**	**clk (ns)**	**#inst**	K_{th}	**IR drop (V)**
Best	1.4	10k	2.08	0.0113	1.4	24k	13.38	0.0431
Reference			1.90	0.0129			11.90	0.0438
Worst			1.76	0.0078			9.08	0.0309

Based on the trained routability model, PDNs with an IR drop greater than the IR drop for the reference PDN are filtered, then the design knobs that constitute the best PDN can be obtained through the predictive model. To validate the ranking of the routability model, we pick two best PDNs, two intermediate quality PDNs, and two worst quality PDNs for verification with the real designs. Table IV shows verification results with AES cipher and JPEG encoder testcases. In actual designs, the cell placement is not uniform, so the denoising is performed through five different random seeds, and the K_{th} of Table IV is the average value of five runs. As shown in Figure 11, although the predicted K_{th} value and the actual K_{th} absolute value are different depending on the netlist, the ranking order is maintained. Thus, an optimal PDN with design knobs is found that has an IR drop less than the reference PDN, along with a best routability.

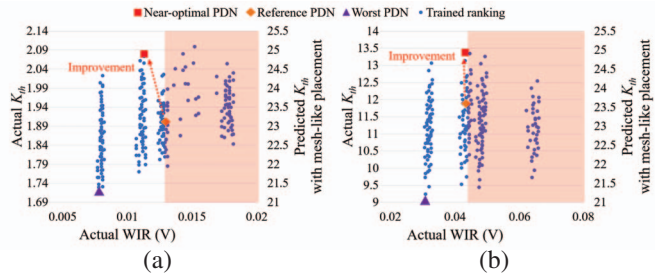

Fig. 11. Routability (K_{th}) versus IR drop data with PDN design knobs for (a) AES encryption core and (b) JPEG encoder testcases. Blue dots denote trained ranking of PDNs and are represented by the second y-axis as K_{th} values. Optimal, reference and worst PDNs are verified by real designs. The red arrows indicate improvement from the reference PDN. The red region indicates WIR greater than the WIR drop of the reference PDN.

V. CONCLUSIONS

In this work, we present a novel power delivery pathfinding methodology for emerging die-to-wafer face-to-face integration. Our work offers several advances as compared to previous works: (i) BEOL routability analysis with consideration of pre-routed PDN; (ii) a new study of interactions between IR drop analysis and routability analysis; and (iii) a PDN pathfinding flow that identifies a high-routability, satisfying PDN design with respect to prescribed worst IR drop constraints for a given design and given BEOL stack options. Experimental studies confirm the stability of the routability ranking of PDN design options across design sizes, as well as "scale-independence" of IR drop behavior due to regular power and ground TSVs; these phenomena are enabling to our pathfinding strategy. In experiments with a 28nm FDSOI enablement, the pathfinding model also accurately predicts the most routable PDN satisfying prescribed IR drop limits. Our ongoing and future works include (i) exploration of additional BEOL stack options, particularly in advanced nodes, and (ii) extension of our approach to integration technologies other than face-to-face integration.

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