Post-Routing Back-End-Of-Line Layout Optimization for Improved Time-Dependent Dielectric Breakdown Reliability

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Abstract

Time-dependent dielectric breakdown (TDDB) is becoming a critical reliability issue, since the electric field across dielectric increases as technology scales. Moreover, dielectric reliability is aggravated when interconnect spacings vary due to (vias and wires) mask misalignment. Although dielectric reliability can be mitigated by a larger interconnect pitch, such a guardband leads to significant area overhead.

In this paper, we propose to improve dielectric reliability through a post-layout optimization. In the layout optimization, we locally shave and/or shift a fraction of wire width to increase the spacing between wires, and/or between adjacent-layer vias and wires. Our experimental results show that the layout optimization can improve interconnect lifetime by 9% to 10%. Separately, we also propose a signal-aware chip-level TDDB reliability estimation method which estimates TDDB stress time of interconnects using net signals obtained from a vectorless analysis. By using the signal-aware analysis method, we show that chip-level TDDB lifetime is approximately twice that obtained using the conventional analysis approach which assumes interconnects are always under electrical stress.

1. INTRODUCTION

Signal levels on adjacent back-end-of-line (BEOL) interconnects induce an electric field (E) across the insulating dielectric. Time-dependent dielectric breakdown (TDDB) occurs when the electrically stressed dielectric forms a conducting path between the interconnects. The dielectric time-to-failure (t_F) due to TDDB can be empirically modeled as

$$t_F = Ae^{(-\gamma E^m)} = Ae^{(-\frac{\gamma V^m}{S^m})} \quad (1)$$

where A is a fitting parameter, γ is the field enhancement factor, V is the voltage difference across the dielectric, S is the spacing between interconnects, and m is a model-dependent scalar. The common values of m are $\{-1.0, 0.5, 1.0\}$, which correspond to the $\{1/E, \sqrt{E}$ and $E\}$ models.[3, 7, 9, 15, 16]

Figure 1(a) shows that the spacing and voltage trends projected by the *International Technology Roadmap for Semiconductors* (ITRS)[10, 11] lead to an increasing electric field as technology scales. Since t_F reduces with an increasing electric field, it is expected that TDDB will be a major reliability concern for BEOL dielectric. Indeed, at the 20nm node (sub-70nm local metal pitch) with litho-etch-litho-etch (LELE) double-patterning, TDDB reliability is a primary limiter to further wiring density improvement.[2] Figure 1(b) shows that 5% spacing increase can improve interconnect lifetime by 20% (in the year 2011) and that the improvement increases as technology scales.*

Recent studies[13, 17, 18] show that mask misalignment between via and wire leads to smaller via-to-wire spacings compared to the wire-to-wire spacings. As a result, dielectric in between via and wire has a higher electric field and a shorter lifetime. Since the lifetime of a chip is affected by the first dielectric that fails, TDDB reliability improvement should focus on via-to-wire spacings. The study conducted by Xia et al.[18] further clarifies, based on measurement results, that TDDB is dominated by via-to-wire spacing (rather than wire-to-wire spacing). To illustrate the impact of a misaligned via, we simulate the electric field of the dielectric between interconnects using a commercial 3D field solver tool.[22] Figure 2 shows that when the via-to-wire spacing is reduced from 70nm to 60nm due to via misalignment, the

*We calculate interconnect lifetime using Equation (1) with $m = 0.5$ and $\gamma = 15.5(\text{cm/MV})^{0.5}$.[14] The values of V and S are obtained from ITRS reports.[10, 11]

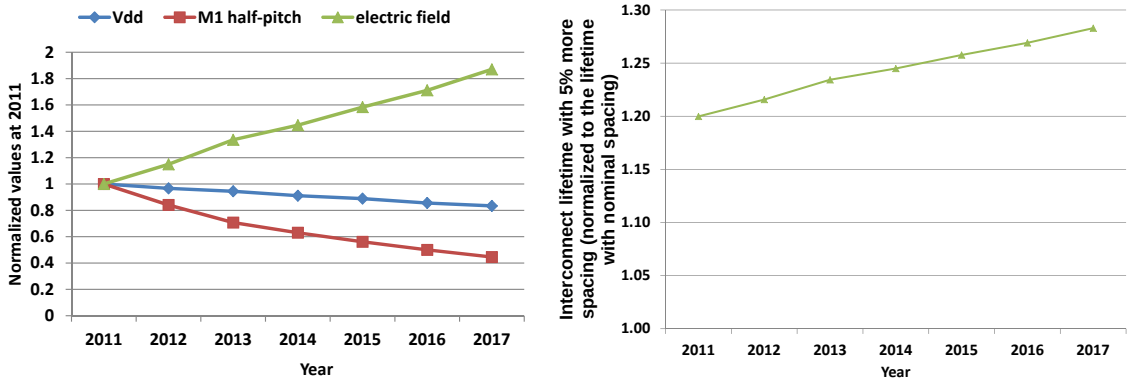

Figure 1. (a) Scaling trend of electric field derived from spacing and supply voltage projections.[10, 11] (b) Lifetime improvement due to 5% spacing increase as technology scales.

electric field around the via is 25% higher than the average electric field between the wires. Moreover, the via-to-wire misalignment is expected to worsen in advanced technology when the vias must land on wires that are misaligned due to LELE double-patterning. Such a worsening TDDB reliability trend will limit wiring pitch and/or the maximum allowed supply voltage.

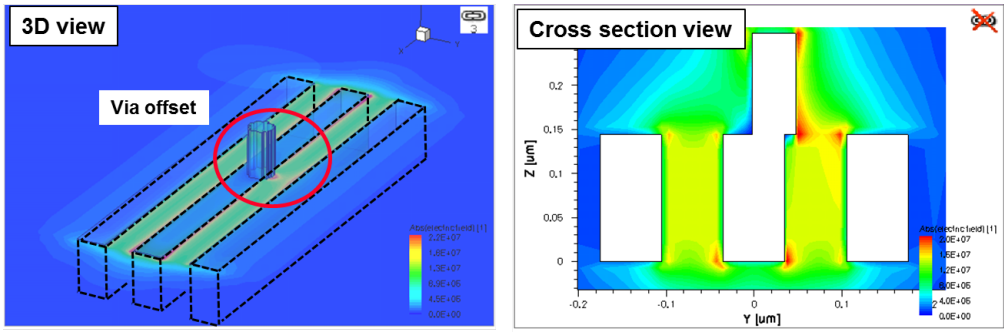

Figure 2: Misaligned via reduces interconnect spacing and enhances electric field.

To reduce design margin due to BEOL TDDB reliability, processing techniques such as self-aligned via patterning[4] and optimization of etch stop layer[6] have been proposed. In this paper, we propose alternative approaches to reduce the margin through (1) signal-aware TDDB reliability estimation and (2) post-detailed routing layout optimization. First, conventional TDDB reliability estimation is based on the worst-case assumption in which each interconnect pair is under DC TDDB stress (i.e., each pair of wires always carries opposite logic signals). Such estimation is clearly pessimistic. To reduce the pessimism, we estimate total stress time for interconnects using state probabilities (i.e., the probability that an interconnect has a logic state '1') that are available from simulation during the logic design phase of IC implementation. In particular, the state probability of all interconnects can be obtained from EDA tools through vectorless logic simulation.[21] Second, our post-routing optimization improves TDDB reliability by local shifting of the edges of small wire segments to enlarge the particular interconnect spacing (dielectric) that is at risk (see Figure 8). Our experimental results in Section 4 show that this layout optimization has negligible impact on both circuit timing and circuit design and design-to-manufacturing flows because the layout optimization makes only small changes to segments of wire edges adjacent to vias.

In summary, the contributions of this paper are:

- A signal-aware TDDB reliability estimation that reduces pessimism in TDDB reliability analysis.

- A post-routing layout optimization technique to improve TDDB reliability.

The remainder of this paper is organized as follows. Section 2 gives a brief review of the TDDB model and our signal-aware TDDB reliability estimation. Section 3 describes the proposed layout optimization method and implementation details. Section 4 presents experimental results and discussion. Section 5 concludes the paper.

2. TDDB MODEL

Equation (1) is commonly used to describe the relationship between electric field strength and the time-to-failure of a given TDDB test structure. To determine the lifetime of a chip, we must account for the chip area vulnerable to TDDB as well as the statistics of TDDB. In this work, we use the chip-level TDDB model developed by Bashir and Milor[1] and extend it to include the effect of via misalignment as well as different stress time among the interconnects with small via-to-wire spacings.

2.1. Chip-Level TDDB Model

Under the same electrical field, identical dielectric may break down at different times. The statistics of dielectric breakdown time can be described by the Weibull or log-normal distributions.[5,8] Chen et al. show that the Weibull distribution fits (large-sample-size TDDB measurement) data better than the log-normal distribution.[8] Therefore, we use the Weibull distribution to describe the statistics of breakdown time and model the failure rate of a dielectric between interconnects i and j as[1,8]

$$F_{ij}(t) = 1 - exp(-(\frac{t}{\eta_{ij}})^{\beta}) \tag{2}$$

where β is the shape factor of the Weibull distribution, t is the total stress time of the dielectric, $F_{ij}(t)$ is the probability of the dielectric breaking down before time t, and η_{ij} is the *characteristic lifetime* of the dielectric, i.e., the total stress time until 63.2% of the dielectric samples fail. Given a via-to-wire test structure,[18] the failure probability of the test structure ($F_{ref}(t)$) can be modeled as

$$\begin{aligned} F_{ref}(t) &= 1 - exp(-(\frac{t}{\eta_{ref}})^{\beta}) \\ \eta_{ref} &= A \cdot exp(\frac{-\gamma V^m}{S_{ref}^m}) \end{aligned} \tag{3}$$

where η_{ref} is the characteristic lifetime of the test structure, m is the scalar of a TDDB model and S_{ref} is the via-to-wire spacing. Since the via-to-wire spacings in a chip can be different from that in the test structure, we apply Poisson area-scaling law to model chip-level TDDB reliability:[1]

$$\begin{aligned} F_{ij}(t) &= 1 - exp[-(\frac{t}{\eta_{ij}})^{\beta}] \\ &= 1 - exp[-(\frac{t}{A \cdot exp(-\gamma V^m / S_{ij}^m)(L_{ref}/L_{ij})^{1/\beta}})^{\beta}] \\ &= 1 - exp[-(\frac{t}{(L_{ref}/L_{ij})^{1/\beta} \cdot \eta_{ref} \cdot exp(-\gamma V^m (S_{ij}^{-m} - S_{ref}^{-m}))})^{\beta}] \\ &= 1 - exp[-(\frac{t}{\eta_{ref}\zeta_{ij}})^{\beta}] \\ \text{where } \zeta_{ij} &= (L_{ref}/L_{ij})^{1/\beta} \cdot exp(-\gamma V^m (S_{ij}^{-m} - S_{ref}^{-m})). \end{aligned} \tag{4}$$

Here, we use S_{ij} and L_{ij} to define the *critical dielectric area* in between via-wire pairs that is vulnerable to TDDB reliability risk. As shown in Figure 3, W_j denotes the width of the j^{th} wire segment, S_{ij} is the spacing between the i^{th} via and the j^{th} wire, and L_{ij} is the length of the critical dielectric area in between the via-wire pair . We define L_{via} (resp. W_{via}) as the dimensions of a rectangular via in the preferred (resp. non-preferred) routing direction in the corresponding via layer. In this work, we only consider square vias; therefore, L_{via} is always the same as W_{via}. Since the via can be

misaligned in the direction parallel to the wire, we extend the length of the critical dielectric area by L_m on each side of the via (in the direction parallel to the wire). Note that we use several pairs of S_{ij} and L_{ij} to represent the critical dielectric area when the area is not a rectangular. Similarly, S_{ref} is the via-to-wire spacing in a teststructure, and L_{ref} is the total length of the critical dielectric areas in the test structure. We assume the dielectric in test structure is the same as the dielectric in actual chips. Thus, A, β and γ of the chip are the same as those extracted from the test structure.

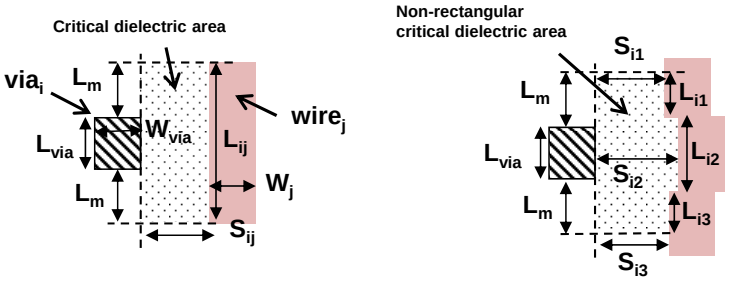

Figure 3: Descriptions of geometrical parameters of a via-wire pair.

Equation (4) shows that the characteristic lifetime of a dielectric, η_{ij}, can be represented in term of test structure characteristic lifetime (η_{ref}) with a scaling factor, ζ_{ij}. To estimate chip-level failure probability, we apply the weakest link model which defines that a chip malfunctions whenever there is a single failure in any interconnect pair. That is,

$$\begin{aligned} F_{chip}(t) &= 1 - \prod_{ij} exp(-(\frac{t}{\eta_{ij}})^{\beta}) \\ &= 1 - exp(-(\frac{t}{\eta_{ref}} \cdot \sum_{ij} \zeta_{ij}^{-1})^{\beta}) \end{aligned} \tag{5}$$

where F_{chip} denotes the chip-level failure probability.

2.2. Signal-Aware TDDB Analysis

Note that the (F_{chip}) Equation (1) implicitly assumes that the dielectric is under DC stress, i.e., interconnects around the dielectric always have opposite logic signals. This assumption is clearly pessimistic because interconnect pairs in a chip may not always be stressed. To reduce the pessimism, we model that an interconnect pair is being stressed only when the interconnects have opposite signals. The chip-level failure probability that accounts for actual stress time is given as

$$F_{chip}(t) = 1 - exp(-(\frac{t}{\eta_{ref}} \cdot \sum_{ij} \alpha_{ij} \zeta_{ij}^{-1})^{\beta}) \tag{6}$$

where α_{ij} is the ratio of total stressed time between the via i and the wire j to the lifetime of the interconnects.

Although Equation (6) is more accurate, extracting the exact stress ratios for all via-wire pairs in a chip is difficult. This is because the logic states of the interconnects (via and wires) are affected by input patterns of the chip, which may be inaccurate or unavailable during chip design time. Even if the input patterns are available, simulating the logic states and extracting the total stress time of all interconnects are time-consuming. To solve the problem of lack of input vectors and slow runtime, we propose to estimate total stress time for interconnects with *state probability* (i.e., the probability that an interconnect has a logic state '1'). The state probability of all interconnects can be obtained from electronic design automation (EDA) tools through vectorless logic simulation,[21] which is much faster than cycle-by-cycle simulation based on input vectors. Since the state probability only specifies the probability of logic state '1' but not the timing information of the logic state (i.e., when the logic state occurs, and time duration of the logic state), we assume that the interconnects have the worst-case signal distribution along the time axis, so that the resulting stress time and lifetime estimation is conservative. Given the state probabilities of two interconnects, the worst-case scenario (maximum stress time) is when one interconnect has logic state '1' at the beginning of a period of time and the other interconnect has logic state '0' at the

beginning of the same period of time. In this case, the interconnect pair is being stressed at the beginning and at the end of the time period. Based on this observation, we can calculate the worst-case *stress ratio*, α_{ij}, for each interconnect pair. The *stress ratio* is defined as the fraction of the time when a pair of interconnects have opposite logic signals.

$$\alpha_{ij} = \begin{cases} q_i + q_j, & \text{if } = (1-q_i) > q_j \\ (1-q_i) + (1-q_j), & \text{otherwise} \end{cases} \tag{7}$$

where q_i is the probability of the i^{th} interconnect to be logic '1'. Estimation of the maximum stress time using Equation (7) is illustrated in Figure 4. In this example, the logic states of interconnect i (resp. j) over time are "lumped" into a continuous logic "1" signal with a time duration proportional to q_i (resp. q_j). By aligning the signals of interconnects i and j according to the worst case scenario mentioned above, we can estimate the stress ratio using Equation (7). We see that the stress ratio obtained by the proposed method is always pessimistic compared to the actual stress ratio.

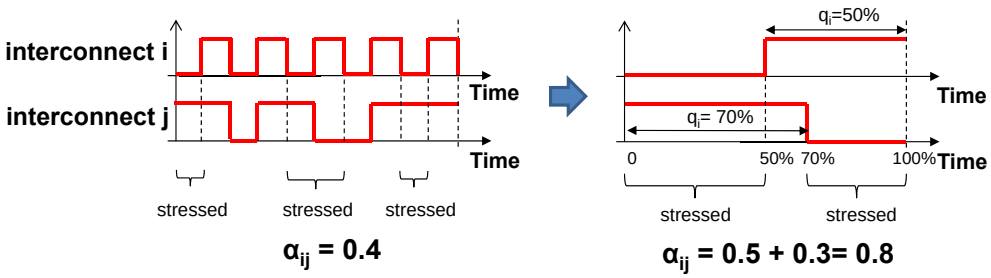

Figure 4: Worst-case stress time estimation based on state probability.

2.3. Modeling Via Misalignment

BEOL via-to-wire spacing can vary due to mask misalignment, lithography-induced spacing variation, etc. To account for the impact of via-to-wire spacing variation on chip-level TDDB reliability, we model the via-to-wire as a normal distribution with zero mean and a standard deviation σ_S. The expectation of ζ_{ij} under spacing variation ($\hat{\zeta}_{ij}$) is given by

$$\hat{\zeta}_{ij} = \int_{x_{ij}=S_{ij}-3\sigma_S}^{x_{ij}=S_{ij}+3\sigma_S} P(x_{ij}) \cdot (L_{ref}/L_{ij})^{1/\beta} \cdot exp(-\gamma V^m (x_{ij}^{-m} - S_{ref}^{-m}))dx_{ij} \tag{8}$$

where $\hat{\zeta}_{ij}$ denotes the expectation of ζ_{ij}, x_{ij} is the value of via-to-wire spacing between via i and wire j and $P(x_{ij})$ is the probability of the spacing equal to x_{ij}. Since there is no analytical closed-form solution for $\hat{\zeta}_{ij}$, we approximate it by discretizing the distribution of x_{ij} into N equal intervals from $S_{ij} - 3\sigma_S$ to $S_{ij} + 3\sigma_S$.

$$\hat{\zeta}_{ij} \approx \sum_{n=1}^{N} \text{cdf}(x_{ij}(n)) \cdot (L_{ref}/L_{ij})^{1/\beta} \cdot exp(-\gamma V^m (x_{ij}(n)^{-m} - S_{ref}^{-m})) \tag{9}$$

Here, $x_{ij}(n)$ is the n^{th} interval of the discretized x_{ij}, and $\text{cdf}(x_{ij}(n))$ is the corresponding cumulative probability for the n^{th} interval of the discretized x_{ij}.

3. POST-ROUTE LAYOUT OPTIMIZATION

Equations (4) and (6) show that $F_{chip}(t)$ can be reduced by increasing S_{ij}. We therefore propose to improve BEOL TDDB reliability by shifting a small fraction of the wire edges around vias to increase S_{ij}. Note that we want only to make small changes on the wire edges because major layout changes to a routed layout may incur additional design iterations and increase design turnaround time.

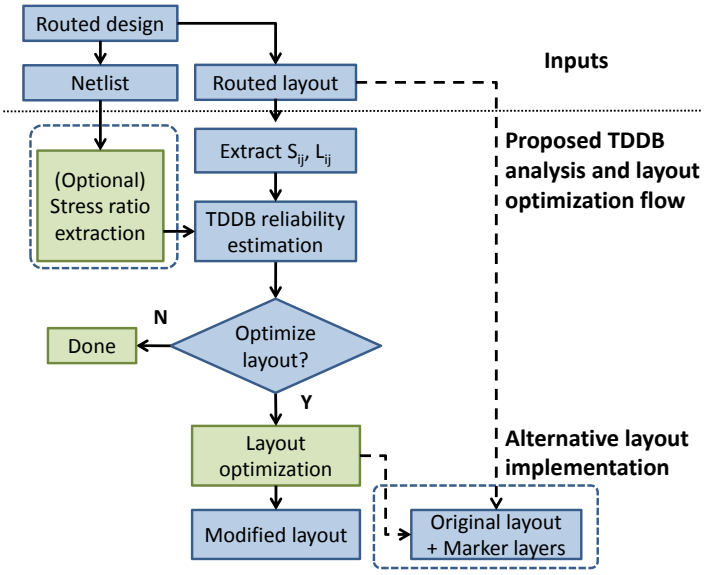

Figure 5: Proposed TDDB reliability estimation and layout optimization flow.

3.1. Overview

Figure 5 shows the overview of our layout optimization flow. Given a routed layout, we can extract the via-to-wire spacings S_{ij} and L_{ij} to calculate the chip lifetime, t, that corresponds to a failure rate, F_{chip} (e.g., 0.5%). If the design netlist is provided (optimally, with input stimuli), we can also extract the state probabilities to account for the stress ratio between interconnects instead of assuming that the interconnects are always stressed. Based on the results of reliability estimation, a chip designer can decide whether layout optimization is needed. If the designer chooses to apply the layout optimization, the layout optimization will generate an optimized layout in which the via-to-wire spacings are increased. We can also generate marker layers in tapeout GDSII to represent the layout modifications. The marker layers can then be read by an OPC tool flow to shift targeted wire edge locations appropriately during mask data preparation.

3.2. Optimizing Layout

Given a routed layout, we collect the via-wire pairs which have via-to-wire spacing smaller than the *safe distance*, S_{safe}. We define S_{safe} as the distance, i.e., spacing, beyond which a dielectric is safe from TDDB (e.g., $S_{safe} \approx$ 95nm in the 32/28nm foundry node with 80nm Mx pitch). We only consider via-wire pairs in which the via is located on the layer above the wire. This is because a via located on the layer below a wire is self-aligned to the wire in a typical dual-damascene process. These self-aligned via-wire pairs have small misalignments and we assume that they are less susceptible to TDDB.[12] For each via-wire pair, we identify *movable* wire edges on each side of the wire segment, such that we can increase the via-to-wire spacing and/or adjust the wire width by shifting the movable edges. As illustrated in Figure 6(a), we first define length of the movable wire edges to be the same as the via edge length (L_{via}) and align the movable wire edges to the via edges. Then, we extend each wire edge by L_m at each end point to account for via misalignment in the direction parallel to the wire. Note that the L_m for each end point can be different, to match the magnitude of via misalignment. For example, in Figure 6(a), L_m at the top (larger y-coordinate) can be larger than that at the bottom (smaller y-coordinate) if the via misalignment magnitude is larger toward the top compared to the bottom. If movable wire edges are overlapped (see Figure 6(b)), we split the movable edges into disjoint, independently movable edges by defining the overlapped region of the edges as new movable edges.

After creating the movable wire edges, we check the vias around the wire segment defined by the movable wire edges. If a via is located in the layer immediately above the wire segment, we do not move the wire edges because moving them may reduce the via landing area, which would lead to lower manufacturing yield. If a via is located in the layer immediately below the wire segment, we can choose to shift the wire edges if the via is self-aligned to the wire in the manufacturing process.[4, 12] With this in mind, we define two layout optimization regimes.

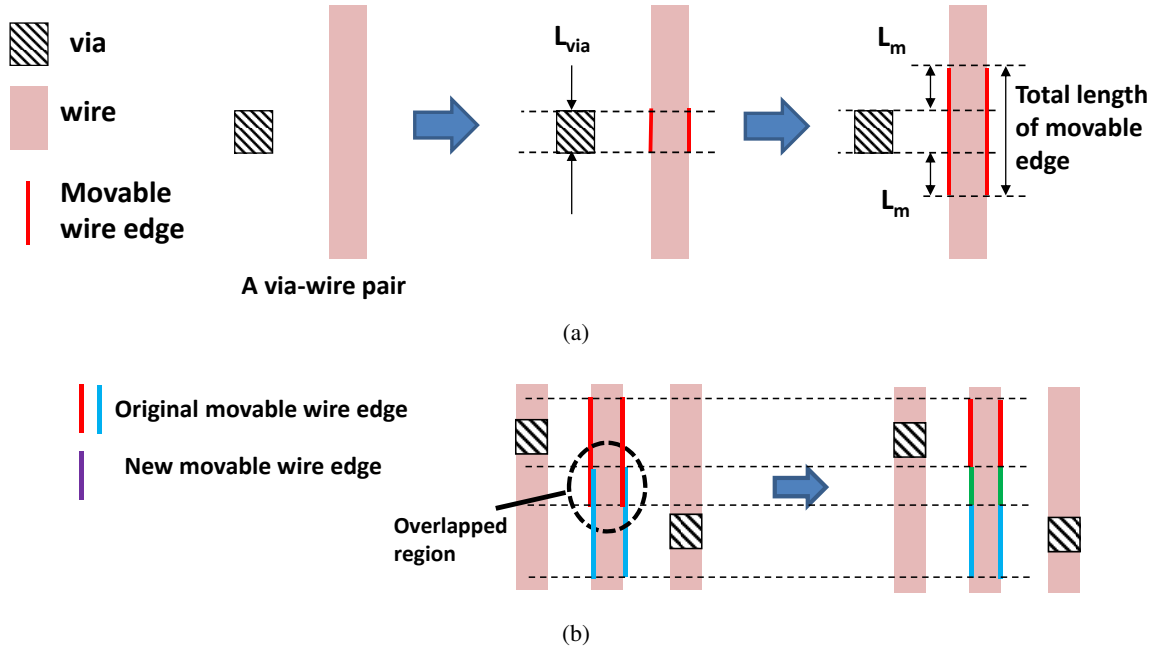

Figure 6. (a) When there is a via next to a wire (at the layer below the via), we define movable edges at both sides of the wire. (b) If movable wire edges are overlapped (dashed oval on left), then the intervals of overlap define new movable edges. The new movable edges are moved independently from other movable wire edges.

- In Regime 1, we do not shift movable wire edges if a via is located in the layer immediately above or below the layer of the wire segment corresponding to these movable wire edges.
- In Regime 2, we do not shift movable wire edges if a via is located in the layer immediately above the layer of wire segment corresponding to these movable wire edges. We can shift the wire edges if the via is located below the wire segment and there is no via located above the wire segment.

For the remaining movable edges, we apply the following shifting rules. Illustrations of the wire shifting are shown in Figure 7.

- If there are vias on both sides of the wire, we shift the movable wire edge inward by ε on both sides, to increase via-to-wire spacings.
- If only one side of the wire has vias, we shift the movable wire edge on that side away from the vias by ε to increase via-to-wire spacing. We also shift the movable wire edge on the other side by ε to preserve wire width.

4. EXPERIMENTAL RESULTS

Our experiments use four register-transfer level designs {AES, MPEG2, JPEG, Sparc_EXU} obtained from the OpenCores[20] and OpenSPARC[19] websites. The designs are implemented using Synopsys 32/28nm NVT, LVT and HVT libraries and BEOL technology files.[†] We synthesize the designs using *Synopsys Design Compiler vC-2009.06-SP2*[25] and then place and route them using *Cadence SoC Encounter vEDI10.1*.[24] In the experiment setup, we analyze interconnects at layers M2, M3 and M4, which have the same layout parameters. We do not consider interconnects above layer M4

[†]We have modified the minimum wire width and spacing in the original library exchange format (LEF) file[23] so that minimum width plus minimum spacing is equal to the minimum pitch defined in the LEF.

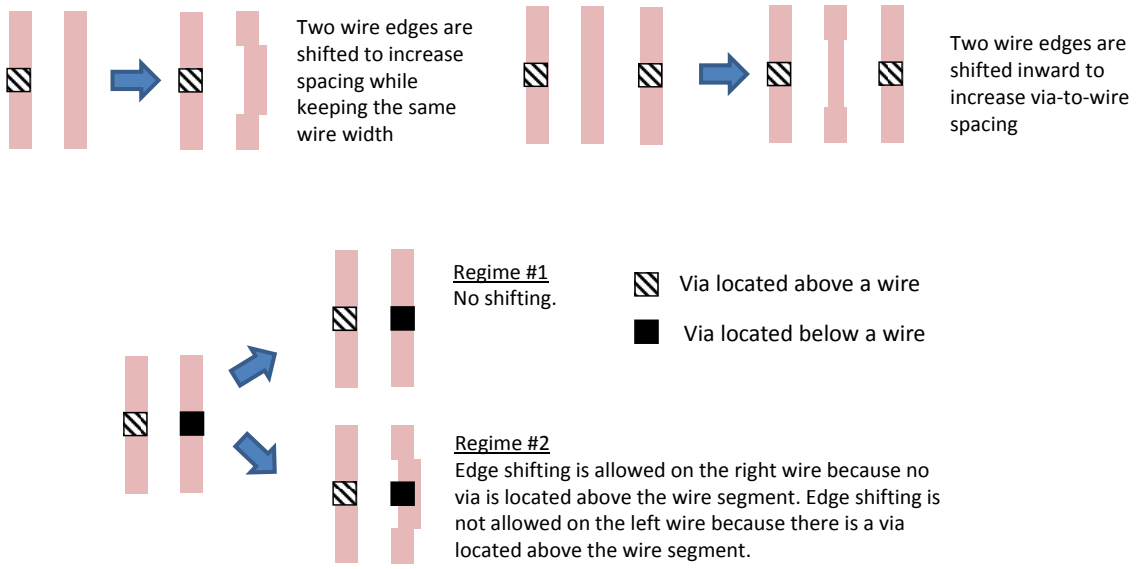

Figure 7: Illustrations of wire shifting.

because in this technology they have via-to-wire spacings larger than S_{safe} (i.e., interconnects at layer M4 and above are not vulnerable to TDDB). On the other hand, we do not consider layer M1 because it is used for standard-cell routing, and we assume that the routing in any standard cell is already optimized for TDDB. The parameters of interconnects and related TDDB model parameters are listed in Table 1. We assume that σ_S is approximately 3% of the pitch, and define $L_m = 6\sigma_S$. The values β, m, and γ of the TDDB model are obtained from published literature.[8, 14] We fit the values of A, S_{ref} and L_{ref} such that chip lifetime is approximately 10 years. (Although the values of A, S_{ref} and L_{ref} change the TDDB lifetime estimation of a chip, they do not affect the ratio of lifetime estimation of layout optimization compared to the original layout.) We implement the TDDB reliability estimation and layout optimization flow in Figure 5 using C++.

Table 1: Layout and TDDB model parameters

Layout parameters	Values	TDDB model parameters	Values
minimum wire spacing	80 nm	A	2e17 seconds
minimum wire width	80 nm	β	1.0
minimum via-to-wire spacing	80 nm	γ	15.5 (cm/MV)$^{0.5}$
via width (L_{via})	70 nm	m	1.0
σ_S	5.0 nm	S_{ref}	80 nm
L_m	30 nm	L_{ref}	80 nm
ε	4.0 nm	V	1.0 V

In our experiment, we apply the layout optimization to each routed layout of the implemented designs. Figure 8 shows an example of wires before and after the layout optimization described in Section 3. In this example, we do not apply edge shifting when there is a via either in the layer immediately above or below the wire segment (defined by the edges). From the figure, we can clearly see that the via-to-wire spacing is increased by shifting the wire edges.

To evaluate the benefits of our proposed methods, we calculate the lifetime, t, of every design by using Equations (6), (7) and (9), with failure rate $F_{chip} = 0.5\%$. For signal-aware TDDB analysis, we extract the state probability of each net obtained from a vectorless analysis.[21] [‡] Results in Table 2 show that by applying our layout optimization method, we can improve chip TDDB lifetime by 9% to 10% (compared to the original layout). The improvement is slightly larger

[‡]In the vectorless analysis, we assume that all primary inputs have 50% probability to be logic '1'. Based on the extracted state probabilities, we calculate the stress ratios α_{ij} for all four designs.

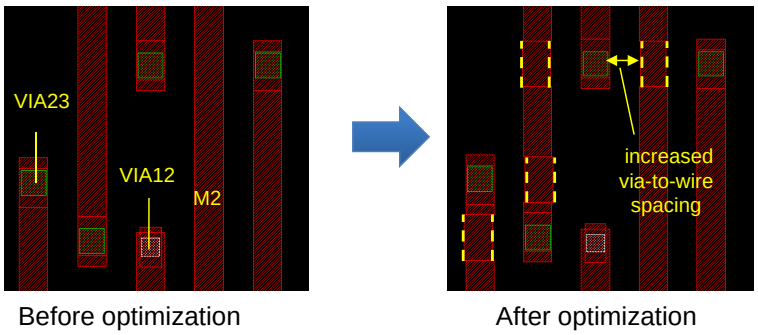

Figure 8. Example of BEOL layout modification. The yellow dotted lines indicate the edges of wire segments that are shifted (locally) to increase via-to-wire spacings and improve TDDB reliability.

in layout optimization Regime 2, which allows edge shifting whenever there is no via located above the edges. Table 2 shows that the lifetime improvements across the two layout optimization regimes only differ by only 1%. This means that there are not many movable wire edges that have a via below them.

Table 2 also shows that our signal-aware TDDB reliability analysis gives chip lifetime estimates that are 1.7 to 2.8 times the lifetime estimates obtained with a pessimistic DC stress assumption (both estimates obtained without layout optimization). This confirms that TDDB reliability is design-specific, i.e., dependent on the stress ratio of interconnect pairs in the design. In all four designs, we can see a marked reduction of pessimism if we use signal-aware TDDB reliability estimation.

Table 2: Chip lifetime (TDDB reliability), normalized to lifetime before layout optimization and with DC stress assumption.

	DC stress			Design-specific stress ratio		
	no opt.	shift edges when there is no via		no opt.	shift edges when there is no via	
		above or below	below only		above or below	below only
AES	1.000	1.087	1.099	1.696	1.846	1.865
JPEG	1.000	1.085	1.097	2.146	2.333	2.359
MPEG2	1.000	1.087	1.102	2.763	3.017	3.052
SPARC_EXU	1.000	1.089	1.100	1.964	2.138	2.158
average	1.000	1.087	1.099	2.142	2.334	2.359

We also study the impact of our layout optimization on BEOL resistance and capacitance as well as circuit timing. (1) We extract the total changes of resistance (ΔR) and capacitance (ΔC) on each net by extracting the changes in wire width and spacing due to the layout optimization. The third column in Tables 3 and 4 show that 5.4k (resp. 6.4k) nets are perturbed by the layout optimizations in Regime 1 (resp. Regime 2). This corresponds to approximately 32% (resp. 37%) of the total nets. The results in Tables 3 and 4 show that the maximum ΔR and ΔC in all the nets in benchmark designs are $< 0.1\Omega$ and $< 0.05fF$, respectively, for both layout optimization regimes. This confirms that our proposed layout optimizations have negligible impact on the wire resistance and capacitance. (2) We attempt to bound the delay changes due to the layout optimization by analyzing two extreme scenarios. In a *gate-worst* scenario, we add the ΔC of a net to the output pin of the driver cell and do not include any ΔR.[§] Then, we run timing analysis to extract the possible stage delays of the net[¶] and calculate the change in delay with respect to each original stage delay without layout optimization. This scenario is designed to estimate the worst-case gate delay impact due to our layout optimization. In a *wire-worst* scenario, we add the ΔC resulting from the layout optimization to the leaf nodes of the net (e.g., input pins of cells driven by the net) and connect the ΔR in series to the output pin of the cell that drives the net. When there is more than one

[§]These changes are made by modifying the original *standard parasitic exchange format* (SPEF) file.

[¶]We define the stage delays of a net to be the signal delays of all feasible timing paths from all input pins of the driver cell to all input pins of cells driven by the net.

leaf node, we assume that the total ΔC is distributed uniformly among all the leaf nodes. Although this may not be the worst-case setup for wire delay variation, having all ΔR at the output pin and all ΔC at leaf nodes is likely to increase the wire delay variation. By adding up the delay differences of gate-worst and wire-worst scenario, we obtain a pessimistic estimation of delay variation due to the layout optimization. Results in Table 3 shows that the maximum Δdelay due to layout optimization in Regime 1 is less than 0.5ps for both gate-worst and wire-worst scenarios. Meanwhile, the average delay variation is less than 0.01ps for both scenarios. Similarly, Table 4 shows that layout optimizations in Regime 2 also have very small Δdelay for both gate-worst and wire-worst scenarios. Together, in Tables 3 and 4 show that our layout optimization has negligible timing impact in both Regimes 1 and 2.

Table 3: Impact of layout optimization in Regime 1 (no edge shifting when a via is above or below the wire segment).

	#Total Nets	#Opt Nets	Max ΔR (Ω)	Max ΔC (fF)	Worst Δdelay (gate) (ps)		Worst Δdelay (wire) (ps)	
					Max	Average	Max	Average
AES	14k	6.5k	0.037	0.023	0.580	0.010	0.580	0.010
JPEG	29k	7.2k	0.050	0.029	0.263	0.004	0.228	0.004
MPEG2	10k	2.5k	0.054	0.028	0.320	0.005	0.320	0.005
SPARC_EXU	15k	5.5k	0.081	0.041	0.649	0.006	0.850	0.006
Average	17k	5.4k	0.056	0.031	0.453	0.006	0.495	0.006

Table 4: Impact of layout optimization in Regime 2 (no edge shifting when a via is above the wire segment).

	#Total Nets	#Opt Nets	Max ΔR (Ω)	Max ΔC (fF)	Worst Δdelay (gate) (ps)		Worst Δdelay (wire) (ps)	
					Max	Average	Max	Average
AES	14k	7.3k	0.037	0.024	0.580	0.010	0.580	0.010
JPEG	29k	8.7k	0.050	0.030	0.263	0.004	0.228	0.004
MPEG2	10k	3.0k	0.070	0.030	0.320	0.005	0.320	0.005
SPARC_EXU	15k	6.4k	0.091	0.041	0.649	0.006	0.850	0.006
Average	17k	6.4k	0.062	0.031	0.453	0.006	0.495	0.006

5. CONCLUSIONS

TDDB is becoming a critical reliability issue for BEOL as technology scales. In the presence of large via-to-wire misalignment, BEOL TDDB limits wire density scaling. To reduce the design margin due to TDDB, we propose a signal-aware chip-level TDDB reliability estimation methodology. Unlike conventional TDDB reliability estimation which assumes that the dielectric is always under DC stress, we estimate the stress ratio based on state probability of the routed signal nets in the chip. By using the signal-aware estimation, we show that chip-level TDDB lifetime is approximately twice that obtained from the conventional analysis approach. We also propose a layout optimization method which shifts wire edges to increase via-to-wire spacings to improve BEOL TDDB reliability. Our experimental results using parameters reflective of the 32nm foundry node show that the layout optimization can increase chip-level lifetime by 9% to 10%; impact at 20nm and below foundry node is expected to be more substantial. The improvement in chip lifetime also means that the chip can operate at a higher supply voltage with the same lifetime if TDDB is the primary factor that limits the maximum allowed supply voltage.

Our proposed layout optimization method may affect other aspects of the layout such as printability, electromigration, etc. Thus, our ongoing work seeks to include electromigration in the reliability analysis, and to develop a layout optimization method that accounts for both TDDB and EM reliability.

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