Performance and Variability Driven Guidelines for BEOL Layout Decomposition with LELE Double Patterning

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Abstract

Litho-etch-litho-etch (LELE) double patterning lithography (DPL) is a strong candidate for BEOL patterning at the 20*nm* logic half-node (sub-80*nm* pitch). In double patterning lithography, layout pattern features must be assigned opposite colors if their spacing is less than the *minimum coloring spacing*. However, complex layouts usually have features that are separated by less than the minimum coloring spacing for any coloring assignment. To resolve the minimum coloring spacing constraint, a pattern feature (polygon) can be split into two different-color segments, introducing a *stitch* at the splitting location. Although many DPL layout decomposition heuristics have been proposed, the impact of stitches on circuit performance is not clearly analyzed. In this work, we study the impact of stitches on BEOL electrical performance based on analytical RC equations. Our studies with 45*nm* (commercial) and 22*nm* (ITRS) technology parameters show that (1) optimal stitching location can reduce delay variation by 5%, and (2) introducing redundant stitches (i.e., splitting an interconnect segment intentionally) can potentially reduce circuit delay variation.

1. INTRODUCTION

In litho-etch-litho-etch (LELE) double patterning lithography (DPL), layout patterns are decomposed into two masks – denoted henceforth as Color 1 and Color 2 – such that all polygons on a given mask satisfy an inter-polygon minimum spacing requirement. If a spacing violation, or *coloring conflict*, arises during decomposition, a polygon (net) can be split into two different-color segments to resolve the violation; this introduces a *stitch* where the two segments are overlapped to avoid disconnection due to overlay and/or line-end shortening. Each segment has different parasitic resistance (R) and capacitance (C), and a stitch also affects total RC delay values of the net, depending on its color, geometric dimensions, overlay, stitching location and length, etc.

In this work, we study the impact of stitch insertion on interconnect RC as well as on circuit performance. Our motivation is that Color 1 and Color 2 interconnect segments have independent CD distributions (bimodal CD distribution) due to two independent exposures in DPL. Gupta et al.[5] note that bimodality of CD variation on poly-silicon features causes delays across spatially adjacent transistors have less correlation. When a signal path passes through the transistors, its delay variability is reduced due to the averaging of uncorrelated transistor delays. Following the observation that bimodality of CD variation can reduce delay variability, we study the impact of stitching insertion, which induces bimodality in interconnects.

Conventional layout decomposition algorithms[2,3,8] focus on solving the color assignment problem, and ignore the impact of stitches on circuit performance. Yang et al.[12] propose a multi-objective layout decomposition framework that accounts for circuit timing. In their algorithm, stitching locations are defined based on the result of initial layout segmentation. Their experimental results show that introducing more stitches (at arbitrary locations on interconnect) help reduce circuit delay variation. However, detailed analysis for stitch insertion is not discussed. Oosten et al.[9] study overlay margin in stitch insertion but do not extend their work on the impact of stitching on circuit performance.

Our studies using 45*nm* (commercial) and 22*nm* (ITRS) technology parameters show that 3σ delay variation varies by as much as 5% when a stitch location is swept along an interconnect. We notice that delay variations are higher when a stitch is located at the driver or receiver end, but lower in the middle. This is because the split segments have different colors and their RC values deviate differently under lithographic variations. Due to the averaging effect across the segments, the delay deviations compensate each other and reduce overall delay variation of the interconnect. This result suggests a design guideline whereby timing-critical routes in dense patterns should preferentially receive stitches to reduce delay variation in the regime of combined CD bimodality and overlay error.

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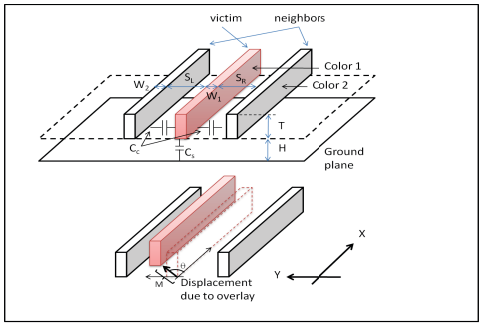
The remainder of this paper is organized as follows. Section 2 introduces analytical formulas to evaluate interconnect RC values and their variations. Section 3 shows the impact of stitching location on interconnect RC and circuit performance. Section 4 summarizes guidelines for DPL layout decomposition and concludes the paper.

2. RESISTANCE AND CAPACITANCE VARIATION MODEL

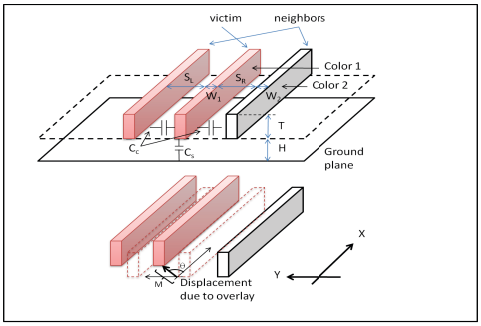
Ghaida et al.[4] study the impact of overlay on parasitic RC but they do not clarify the impact of stitching location. Here, we study RC variation of VLSI interconnects with layout configurations as illustrated in Figure 1. For each layout configuration, we define an interconnect under test as victim and other interconnects as neighbors. T, $W_{1,2}$, $S_{L,R}$ and H are respectively the thickness, width, spacing and dielectric thickness of the interconnects. C_s and C_c are ground capacitance and coupling capacitance of the victim. Displacement between interconnects with different colors is modeled as a vector (M, θ) in polar coordinates, where M is magnitude and θ is polar angle of the displacement. To account for CD variation, we define interconnect width and spacing as follows.

$$
\begin{aligned}
W_1 &= W_0 + \Delta W_1 \\
W_2 &= W_0 + \Delta W_2 \\
S_R &= S_0 - 0.5(\Delta W_1) - 0.5(\Delta W_2) - M \times cos\ \theta \\
S_L &= \begin{cases} S_0 - 0.5(\Delta W_1) - 0.5(\Delta W_2) + M \times cos\ \theta & \text{for case (a) and (c) of Figure1} \\ S_0 - (\Delta W_1) & \text{for case (b) of Figure1} \end{cases}
\end{aligned} \tag{1}
$$

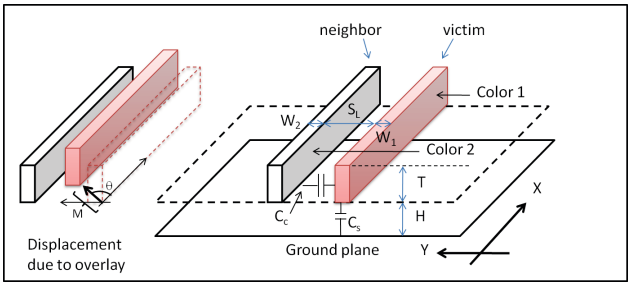
where ΔW_1 and ΔW_2 are width variations due to two independent CD distributions in DPL, W_0 is nominal width, and S_0 is nominal spacing. We model ΔW_1, ΔW_2 and M as Gaussian distributions, and θ as a uniform distribution from 0 to 2π. The values of nominal geometric dimensions and lithography variation parameters are summarized in Table 1. It should be noted that S_{min} in Table 1 corresponds to the minimum spacing achievable between different-color segments. Since the spacing requirements are different among the interconnect cases in Figure 1(a)*, we use $S_0 = 2 \times S_{min}$ for all interconnect cases to enable a fair comparison.



(a) Three interconnects with symmetric coloring.



(b) Three interconnects with asymmetric coloring.



(c) Two interconnects.

Figure 1: Interconnect dimensions and displacement due to overlay.

*A larger minimum spacing must exist between same-color segments as in the asymmetric case (b) of Figure 1.

Table 1: Geometric dimensions and lithography variation parameters for 45*nm* (commercial) and 22*nm* (ITRS[6]) technologies.

Parameter	**unit**	**45***nm*	**22***nm*
S_{min}	*nm*	70	32
S_0	*nm*	140	64
W_0	*nm*	70	32
T	*nm*	140	60
H	*nm*	140	60
Mean(W_1)	*nm*	0	0
Mean(W_2)	*nm*	0	0
Mean(M)	*nm*	0	0
3 σ (W_1)	*nm*	14	6.4
3 σ (W_2)	*nm*	14	6.4
3 σ (M)	*nm*	14	6.4
ε_{eff}	-	3.3	2.75
ρ	Ω	27×10^9	50×10^9

In our study, we assume that the interconnects in Figure 1 have stitch locations as defined in Figure 2, where x_1 and x_2 are lengths of victim interconnects with Color 1 and Color 2, respectively. Although interconnects with different colors will overlap at stitching locations, the overlap length is much smaller than the interconnect length (e.g. 30*nm* out of 50,000*nm*). Hence, we do not separately model the parasitic RC of the overlapping region.

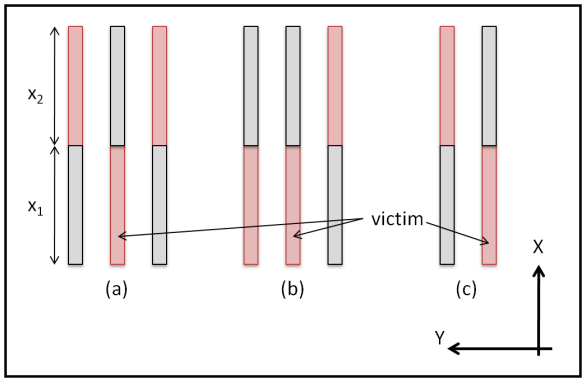


Figure 2: Top view of interconnect configurations from Figure 1, with stitches.

2.1. Capacitance Formulas for Three Parallel Interconnects with Symmetric Coloring

We use formulas from Chang[1] for ground capacitance (C_s) and from Sakurai et al.[10] for coupling capacitance (C_c). Then, total capacitance (C_v) for three parallel interconnects with symmetric coloring (Figure 1(a)) is given as follows.

$$\begin{aligned}
C_v &= (C_s + C_c) \\
C_s &= \varepsilon_{ox}\left[\frac{x_1}{x_1+x_2}\times h(W_1) + \frac{x_2}{x_1+x_2}\times h(W_2)\right] \\
C_c &= \varepsilon_{ox}\left[\frac{x_1}{x_1+x_2}\times f(W_1)\times g(W_1,W_2,Y) + \frac{x_2}{x_1+x_2}\times f(W_2)\times g(W_2,W_1,-Y)\right] \\
h(W_1) &= k_1 + k_2\left(\frac{W_1}{H}\right) + k_3\left(\frac{W_1}{H}\right)^{m_1} + k_4\left(\frac{T}{H}\right)^{m_2} \\
f(W_1) &= k_5\left(\frac{W_1}{H}\right) + k_6\left(\frac{T}{H}\right) + k_7\left(\frac{T}{H}\right)^{m_3} \\
g(W_1,W_2,Y) &= \left[\left(\frac{S_0 - 0.5(W_1-W_0) - 0.5(W_2-W_0) - Y}{H}\right)^{m_4} + \left(\frac{S_0 - 0.5(W_1-W_0) - 0.5(W_2-W_0) + Y}{H}\right)^{m_4}\right] \\
Y &= M \times cos\,\theta \\
\varepsilon_{ox} &= \varepsilon_{eff}\times\varepsilon_0
\end{aligned} \tag{2}$$

In the above, $k_1,...,k_7$ and m_1, ..., m_4 are unitless constants, ε_{eff} is dielectric constant, and ε_0 is free-space permittivity. Values of these parameters are summarized in Table 1 and Table 2. To derive the impact of dimensional variations, we linearize the capacitance formulas using first-order Taylor series expansion:†

$$\begin{aligned}
C_s &\approx C_s|_{W=W_0,\ S=S_0} + \frac{\partial C_s}{\partial W_1}(\Delta W_1) \\
C_c &\approx C_c|_{W=W_0,\ S=S_0} + \frac{\partial C_c}{\partial W_1}(\Delta W_1) + \frac{\partial C_c}{\partial W_2}(\Delta W_2) + \frac{\partial C_c}{\partial Y}(\Delta Y)
\end{aligned} \tag{3}$$

Since C_c and C_s are linear functions of W_1, W_2 and Y, we calculate the mean and variance of C_c and C_s as follows.

$$\begin{aligned}
Mean(C_v) &= C_s|_{W=W_0,\ S=S_0} + C_c|_{W=W_0,\ S=S_0} \\
Var_{DPL}(C_v) &= \left[\left(\frac{\partial C_s}{\partial W_1}\right) + \left(\frac{\partial C_c}{\partial W_1}\right)\right]^2 Var(W_1) + \left(\frac{\partial C_c}{\partial W_2}\right)^2 Var(W_2) + \left(\frac{\partial C_c}{\partial Y}\right)^2 Var(Y) \\
Var(Y) &= E\left[Y^2\right] - [Mean(Y)]^2 \\
&= E[M^2]E[cos^2\theta] \\
&= \sigma_M^2 \times \int_0^{2\pi} \frac{cos^2\theta}{2\pi} d\theta \\
&= \frac{\sigma_M^2}{2}
\end{aligned} \tag{4}$$

In the case of conventional single-patterning lithography (SPL), all interconnects have identical widths and there is no variability due to overlay. Therefore, W_1 and W_2 are fully correlated, and $Y = 0$. The capacitance variance for SPL is given as follows.

$$Var_{SPL}(C_v) = \left[\left(\frac{\partial C_s}{\partial W_1}\right) + \left(\frac{\partial C_c}{\partial W_1}\right) + \left(\frac{\partial C_c}{\partial W_2}\right)\right]^2 Var(W_1) \tag{5}$$

†Detailed derivations for $\frac{\partial C_s}{\partial W_1}$, $\frac{\partial C_c}{\partial W_1}$, $\frac{\partial C_c}{\partial W_2}$ and $\frac{\partial C_c}{\partial Y}$ are given in Appendix A.

Table 2: Capacitance model parameters.[1, 10]

Parameters	Values
k_1	0.770
k_2	1.000
k_3	1.060
k_4	1.060
k_5	0.030
k_6	0.830
k_7	-0.070
m_1	0.250
m_2	0.500
m_3	0.222
m_4	-1.340
ε_0	8.854 $F \cdot m^{-1}$

2.2. Capacitance Formulas for Three Parallel Interconnects with Asymmetric Coloring

The capacitance formulas for the asymmetric case are as follows (see Appendix B for detailed derivation).

$$\begin{aligned} g_{asym}(W_1,W_2,Y) &= \left[\left(\frac{S_0-(W_1-W_0)}{H}\right)^{m_4}+\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4}\right] \\ C_{s-asym} &= C_s \\ C_{c-asym} &= \varepsilon_{ox}\times\left[\frac{x_1}{x_1+x_2}\times f(W_1)\times g_{asym}(W_1,W_2,Y)+\frac{x_2}{x_1+x_2}\times f(W_2)\times g_{asym}(W_2,W_1,-Y)\right] \end{aligned} \tag{6}$$

$$\begin{aligned} Mean(C_{v-asym}) &= C_{s-asym}|_{W=W_0,\ S=S_0}+C_{c-asym}|_{W=W_0,\ S=S_0} \\ Var(C_{v-asym}) &= \left[\left(\frac{\partial C_{s-asym}}{\partial W_1}\right)+\left(\frac{\partial C_{c-asym}}{\partial W_1}\right)\right]^2 Var(W_1)+\left(\frac{\partial C_{c-asym}}{\partial W_2}\right)Var(W_2)+\left(\frac{\partial C_{c-asym}}{\partial W_2}\right)Var(Y) \end{aligned} \tag{7}$$

Note that the form of the Equation (7) is not changed compared to Equation (4), but we label all the terms with *asym* to indicate that the parameters are different from those in the symmetric interconnect case. Based on the equations, victim interconnects in Figure 1(a) and Figure 1(b) have the same mean capacitance value (if $S_L = S_R$) but different variations.

2.3. Capacitance Formulas for Two Parallel Interconnects

Capacitance of the victim in Figure 1(c) is different from that in Figure 1(a) as there is no right-hand side neighbor. Capacitance for two parallel interconnects (see Appendix C for detailed derivation) is given as follows, with a subscript *dual* to indicate there are two parallel interconnects.

$$\begin{aligned} C_{s-dual} &= \varepsilon_{ox}\times\left[\frac{x_1}{x_1+x_2}\times h(W_1)+\frac{x_2}{x_1+x_2}\times h(W_2)\right] \\ C_{c-dual} &= \varepsilon_{ox}\times\left[\frac{x_1}{x_1+x_2}\times f(W_1)\times g_{dual}(W_1,W_2,Y)+\frac{x_2}{x_1+x_2}\times f(W_2)\times g_{dual}(W_2,W_1,-Y)\right] \\ g_{dual}(W_1,W_2,Y) &= \left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4} \end{aligned} \tag{8}$$

where C_{s-dual}, and C_{c-dual} are ground and coupling capacitance, respectively. Consequently, the linearized expressions for capacitance mean and variance of two parallel interconnects are as follows.

$$\begin{aligned}
C_{s-dual} &\approx C_{s-dual}|_{W=W_0,\ S=S_0} + \frac{\partial C_{s-dual}}{\partial W_1}(\Delta W_1) \\
C_{c-dual} &\approx C_{c-dual}|_{W=W_0,\ S=S_0} + \frac{1}{2}\left[\frac{\partial C_{c-dual}}{\partial W_1}(\Delta W_1) + \frac{\partial C_{c-dual}}{\partial W_2}(\Delta W_2) + \frac{\partial C_{c-dual}}{\partial Y}(\Delta Y)\right] \\
Mean(C_{v-dual}) &= C_{s-dual}|_{W=W_0,\ S=S_0} + C_{c-dual}|_{W=W_0,\ S=S_0} \\
Var_{DPL}(C_{v-dual}) &= \left[\left(\frac{\partial C_{s-dual}}{\partial W_1}\right) + \left(\frac{\partial C_{c-dual}}{\partial W_1}\right)\right]^2 Var(W_1) + \left(\frac{\partial C_{c-dual}}{\partial W_2}\right)^2 Var(W_2) + \left(\frac{\partial C_{c-dual}}{\partial Y}\right)^2 Var(Y) \\
Var_{SPL}(C_{v-dual}) &= \left[\left(\frac{\partial C_{s-dual}}{\partial W_1}\right) + \left(\frac{\partial C_{c-dual}}{\partial W_1}\right) + \left(\frac{\partial C_{c-dual}}{\partial W_2}\right)\right]^2 Var(W_1)
\end{aligned} \tag{9}$$

2.4. Interconnect Resistance Formulas

Resistance variation on the victim interconnect is only affected by the width of the victim. Therefore, all interconnect segments in Figure 2 have the same parasitic resistance model:

$$\begin{aligned}
R_v &= \frac{\rho}{W \times T} \\
Mean(R_v) &= R_v|_{W_1=W_0} \\
Var(R_v) &\approx \left(\frac{-\rho}{TW_0^2}\right)^2 \times Var(W_1)
\end{aligned} \tag{10}$$

3. EXPERIMENTAL RESULTS

3.1. RC Variation Analysis

Based on the RC equations in Section 2, we calculate capacitance values of interconnects in Figure 1 (i.e., there is no stitching, and each victim interconnect is assigned to a single color). To compare different interconnect cases, we use $S_0 = 2 \times S_{min}$ so that all interconnect patterns satisfy minimum coloring spacing. Results in Table 3[‡] show that capacitance variation with DPL is marginally smaller than with SPL. This is because the width and spacing variations of DPL interconnects are not correlated, as a consequence of the two independent exposures. Even though DPL interconnects are affected by overlay, the overall variation is less than the SPL case. As one would expect, the two-line interconnect pattern has smaller variance (relative to mean) than the three-line interconnect pattern. This is because the victim in the two-line interconnect pattern has less coupling capacitance that is sensitive to width or spacing variation (ground capacitance is identical for all interconnect patterns).

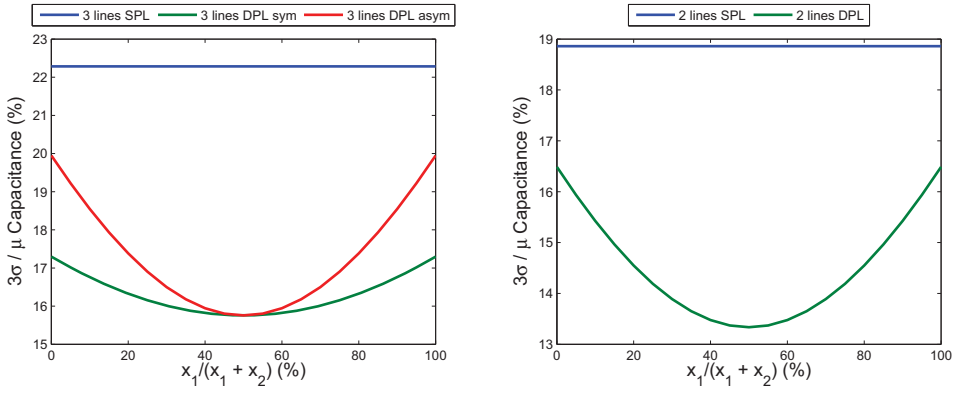
Table 3: Capacitance values of victim interconnects in Figure 1.

	22*nm* technology					45*nm* technology				
	3 lines			2 lines		3 lines			2 lines	
	SPL	DPL sym	DPL asym	SPL	DPL	SPL	DPL sym	DPL asym	SPL	DPL
$\mu\ (aF/um)$	114.3	114.3	114.3	96.9	96.9	139.4	139.4	139.4	116.8	116.8
$3\sigma(aF/um)$	25.5	19.8	22.8	18.3	16.0	31.4	24.1	28.0	22.0	19.2
$\frac{3\sigma}{\mu}$ (%)	22.3	17.3	19.9	18.9	16.5	22.5	17.3	20.1	18.9	16.4

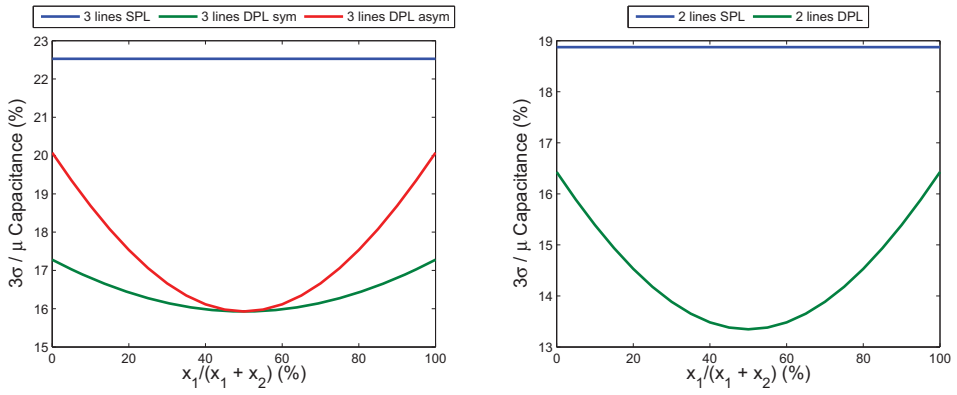
To study the effect of interconnect coloring and stitching location, we sweep the stitching location along the x-axis in Figure 2. Results in Figure 3 show that capacitance variation of DPL interconnect changes according to the stitching location. The minimal capacitance variation is achieved when stitching point is at the middle of interconnect (i.e., $x_1 = x_2$). These data suggest that

[‡]Jeong et al.[7] obtained capacitance values similar to the ones in Table 3 using a commercial 3D RC field solver tool (Synopsys Raphael, Version 2004.06[11]).

1. DPL interconnects always have lower capacitance variation (relative to mean) than SPL interconnects.
2. Redundant stitching in DPL is beneficial as it reduces capacitance variations compared to DPL with no stitching, i.e., $3\sigma/\mu$ capacitance of DPL interconnects reduce as x_1 changes from 0 (100% Color 2) to $x_1 = x_2$ (one stitch, Color 1 and Color 2 interconnect lengths are balanced.).



(a) 22*nm* technology



(b) 45*nm* technology

Figure 3. Capacitance variation of interconnects. Normal (SPL) interconnects have no stitching, hence their capacitance values do not vary with stitching location. Capacitance variation for DPL interconnects is minimized when the color assignment is balanced, i.e., stitching is located at the middle of the interconnect.

3.2. Delay Variation Analysis

To study the impact of stitching on circuit delay, we simulate a testing circuit illustrated in Figure 4. The testing circuit consists of a pair of inverters connected by a series of RC modules, each of which represents 5% of a victim interconnect (i.e., the victim interconnect is divided into 20 identical segments). The RC values for a given RC module are calculated using the analytical equations in Section 2, with dimensions according to its color assignment. In this study, the inverter cell is obtained from a commercial library (45*nm*) and predictive technology model[13] (22*nm*). The test circuit is simulated using SPICE with a 50*ps* ramp input signal and a Monte Carlo setup with 3000 trials[§]. The size of the inverter is scaled

[§]Small sample size for Color 1 and Color 2 CD random variables can induce additional (unwanted) mean CD shift between them. This may lead to incorrect interpretations on the impact of stitching.

according to the length of interconnect, e.g., a 100*um* interconnect uses a (1×) inverter while a 1000*um* interconnect uses a (10×) inverter.

Figure 5 shows the impact of stitching location on circuit delay. Stitching location is denoted by an index from 1 to 21 which corresponds to equally-spaced discrete locations from source to sink. In particular, stitching location = 1 (resp. = 21) means that the stitching location is immediately after the driver (resp. immediately before the receiver), and the entire interconnect is assigned to Color 2 (resp. Color 1). If the stitching location = 11, the driver-side half is Color 1 and the receiver-side half is Color 2.

All testcases in Figure 5 show that DPL interconnect has less delay variation compared to the SPL case. As mentioned earlier, this is due the averaging effect of DPL interconnects. We also notice that stitching around the middle of interconnect leads to minimal delay variation (long interconnect). This is expected because the capacitance variation of interconnect is minimal when the portions of Color 1 and Color 2 are equal (for DPL). Note that for all testcases, minimum $3\sigma/mean$ is attained when stitching location is slightly shifted towards the driver side. This is because circuit delay is more sensitive to RC changes on the driver side, due to the resistance shielding effect. Resistance shielding implies that driver-side capacitance has more contribution to RC delay than receiver-side capacitance. As a result, the stitching location shifts slightly toward the driver side to balance the effective RC of interconnects with Color 1 and Color 2.

To model the bimodal distribution in DPL, we perturb the mean of interconnect Color 1 by $\pm 2nm$. Figures 5(c) and (d) show that testcases with $\pm 2nm$ ΔCD mean behave similarly to those with ΔCD mean = 0. In other words, the impact of ΔCD mean is negligible for circuit delay analysis. Similarly, the delay variation trends for 45*nm* and 22*nm* technologies (Figures 5(b) and (e)) are qualitatively the same. This hints that we should expect similar delay variation phenomena in future technologies. Comparing Figure 5(a) and Figure 5(b), we see that the impact of stitching location on short interconnect (100*um*) is slightly less than that on long interconnects (1000 *um*), but the trends are similar.

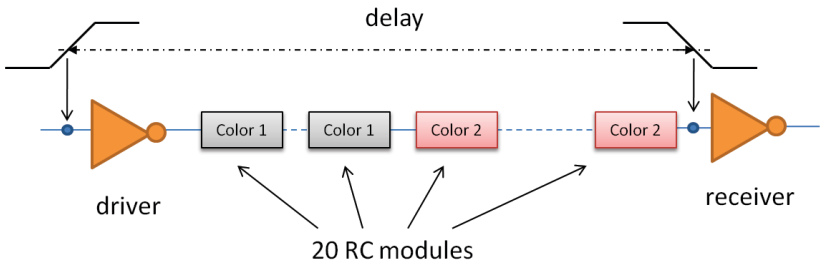


Figure 4. Testing circuit to study the impact of stitching locations. Each of the 20 RC modules represents 5% of the parasitic RC of the entire interconnect, and is assigned to either Color 1 or Color 2. There is only one splitting/stitching point along the modules.

4. CONCLUSIONS

In this work, we derive analytical RC equations for LELE DPL-based interconnects to study the impact of stitching insertion on interconnects RC and circuit performance. Our experimental results show that DPL without any stitching along victim interconnect has less delay variation compared to SPL. This suggests that layout decomposition algorithms should alternate color assignments of interconnects, so that delay variation is partially alleviated due to averaging effect. The results also show that interconnect with a stitch always has a smaller delay variation compared to interconnect without any stitch. This implies that, long interconnect should preferentially receive stitches to reduce delay variation. The results in Figure 5 suggest that stitching location should be placed along an interconnect such that the interconnect has equal proportion of segments. Although the stitching location is slightly shifted towards driver side, there is only a small difference between the minimum delay variation versus the case where a stitch is placed at the middle of the interconnect. Therefore, always splitting an interconnect at its midpoint could be a simple yet near-optimal mask optimization strategy for minimum performance variation.

Appendix A : Derivations for Symmetric 3-lines Interconnect

$$\text{let } h(W_1) = k_1 + k_2\left(\frac{W_1}{H}\right) + k_3\left(\frac{W_1}{H}\right)^{m_1} + k_4\left(\frac{T}{H}\right)^{m_2}$$

$$f(W_1) = k_5\left(\frac{W_1}{H}\right) + k_6\left(\frac{T}{H}\right) + k_7\left(\frac{T}{H}\right)^{m_3}$$

$$g(W_1,W_2,Y) = \left[\left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) - Y}{H}\right)^{m_4} + \left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) + Y}{H}\right)^{m_4}\right]$$

$$C_s = \varepsilon_{ox} \times \left[\frac{x_1}{x_1 + x_2} \times h(W_1) + \frac{x_2}{x_1 + x_2} \times h(W_2)\right]$$

$$C_c = \varepsilon_{ox} \times \left[\frac{x_1}{x_1 + x_2} \times f(W_1) \times g(W_1,W_2,Y) + \frac{x_2}{x_1 + x_2} \times f(W_2) \times g(W_2,W_1,-Y)\right]$$

$$\frac{\partial h(W_1)}{\partial W_1} = \frac{k_2}{H} + \frac{k_3 \times m_1 \times W_1^{(m_1 - 1)}}{H^{m_1}}$$

$$\frac{\partial h(W_2)}{\partial W_2} = \frac{k_2}{H} + \frac{k_3 \times m_1 \times W_2^{(m_1 - 1)}}{H^{m_1}}$$

$$\frac{\partial f(W_1)}{\partial W_1} = \frac{\partial f(W_2)}{\partial W_2} = \frac{k_5}{H}$$

$$\frac{\partial f(W_1)}{\partial W_2} = \frac{\partial f(W_2)}{\partial W_1} = 0$$

$$\frac{\partial g(W_1,W_2,Y)}{\partial W_1} = \frac{\partial g(W_1,W_2,Y)}{\partial W_2} = \frac{-m_4}{2H}\left[\left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) - Y}{H}\right)^{m_4 - 1} + \left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) + Y}{H}\right)^{m_4 - 1}\right]$$

$$\frac{\partial g(W_2,W_1,-Y)}{\partial W_1} = \frac{\partial g(W_2,W_1,-Y)}{\partial W_2} = \frac{-m_4}{2H}\left[\left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) + Y}{H}\right)^{m_4 - 1} + \left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) - Y}{H}\right)^{m_4 - 1}\right]$$

$$\frac{\partial g(W_1,W_2,Y)}{\partial Y} = \frac{\partial g(W_2,W_1,-Y)}{\partial Y} = \frac{-m_4}{H}\left[\left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) - Y}{H}\right)^{m_4 - 1} - \left(\frac{S_0 - 0.5(W_1 - W_0) - 0.5(W_2 - W_0) + Y}{H}\right)^{m_4 - 1}\right]$$

$$\frac{\partial C_s}{\partial W_1} = \varepsilon_{ox} \times \frac{x_1}{x_1 + x_2} \times \frac{\partial h(W_1)}{\partial W_1}$$

$$\frac{\partial C_s}{\partial W_2} = \varepsilon_{ox} \times \frac{x_2}{x_1 + x_2} \times \frac{\partial h(W_2)}{\partial W_2}$$

$$\frac{\partial C_c}{\partial W_1} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1 + x_2}\left(\frac{\partial f(W_1)}{\partial W_1} \times g(W_1,W_2,Y) + \frac{\partial g(W_1,W_2,Y)}{\partial W_1} \times f(W_1)\right) + \frac{x_2}{x_1 + x_2}\left(\frac{\partial g(W_2,W_1,-Y)}{\partial W_1} \times f(W_2)\right)\right]$$

$$\frac{\partial C_c}{\partial W_2} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1 + x_2}\left(\frac{\partial g(W_1,W_2,Y)}{\partial W_2} \times f(W_1)\right) + \frac{x_2}{x_1 + x_2}\left(\frac{\partial f(W_2)}{\partial W_2} \times g(W_1,W_2,Y) + \frac{\partial g(W_2,W_1,-Y)}{\partial W_2} \times f(W_2)\right)\right]$$

$$\frac{\partial C_c}{\partial Y} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1 + x_2}\left(f(W_1) \times \frac{\partial g(W_1,W_2,Y)}{\partial Y}\right) + \frac{x_2}{x_1 + x_2}\left(f(W_2) \times \frac{\partial g(W_2,W_1,-Y)}{\partial Y}\right)\right]$$

Appendix B : Derivations for Asymmetric 3-lines Interconnect

$$g_{asym}(W_1,W_2,Y) = \left[\left(\frac{S_0-(W_1-W_0)}{H}\right)^{m_4} + \left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4}\right]$$

$$C_{s-asym} = C_s$$

$$C_{c-asym} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2} \times f(W_1) \times g_{asym}(W_1,W_2,Y) + \frac{x_2}{x_1+x_2} \times f(W_2) \times g_{asym}(W_2,W_1,-Y)\right]$$

$$\frac{\partial g_{asym}(W_1,W_2,Y)}{\partial W_1} = \frac{-m_4}{2H}\left[2\left(\frac{S_0-(W_1-W_0)}{H}\right)^{m_4-1} + \left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4-1}\right]$$

$$\frac{\partial g_{asym}(W_1,W_2,Y)}{\partial W_2} = \frac{-m_4}{2H}\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4-1}$$

$$\frac{\partial g_{asym}(W_2,W_1,-Y)}{\partial W_1} = \frac{-m_4}{2H}\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4-1}$$

$$\frac{\partial g_{asym}(W_2,W_1,-Y)}{\partial W_2} = \frac{-m_4}{2H}\left[2\left(\frac{S_0-(W_2-W_0)}{H}\right)^{m_4-1} + \left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4-1}\right]$$

$$\frac{\partial g_{asym}(W_1,W_2,Y)}{\partial Y} = \frac{m_4}{H}\left[\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4-1}\right]$$

$$\frac{\partial g_{asym}(W_2,W_1,-Y)}{\partial Y} = \frac{-m_4}{H}\left[\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4-1}\right]$$

$$\frac{\partial C_{s-asym}}{\partial W_1} = \frac{\partial C_s}{\partial W_1}$$

$$\frac{\partial C_{s-asym}}{\partial W_2} = \frac{\partial C_s}{\partial W_2}$$

$$\frac{\partial C_{c-asym}}{\partial W_1} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2}\left(\frac{\partial f(W_1)}{\partial W_1} \times g_{asym}(W_1,W_2,Y) + \frac{\partial g_{asym}(W_1,W_2,Y)}{\partial W_1} \times f(W_1)\right) + \frac{x_2}{x_1+x_2}\left(\frac{\partial g_{asym}(W_2,W_1,-Y)}{\partial W_1} \times f(W_2)\right)\right]$$

$$\frac{\partial C_{c-asym}}{\partial W_2} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2}\left(\frac{\partial g_{asym}(W_1,W_2,Y)}{\partial W_2} \times f(W_1)\right) + \frac{x_2}{x_1+x_2}\left(\frac{\partial f(W_2)}{\partial W_2} \times g_{asym}(W_1,W_2,Y) + \frac{\partial g_{asym}(W_2,W_1,-Y)}{\partial W_2} \times f(W_2)\right)\right]$$

$$\frac{\partial C_{c-asym}}{\partial Y} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2}\left(f(W_1) \times \frac{\partial g_{asym}(W_1,W_2,Y)}{\partial Y}\right) + \frac{x_2}{x_1+x_2}\left(f(W_2) \times \frac{\partial g_{asym}(W_2,W_1,-Y)}{\partial Y}\right)\right]$$

Appendix C : Derivations for Asymmetric 2-lines Interconnect

$$\text{let } g_{dual}(W_1,W_2,Y) = \left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4}$$

$$C_s = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2} \times h(W_1) + \frac{x_2}{x_1+x_2} \times h(W_2)\right]$$

$$C_c = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2} \times f(W_1) \times g_{dual}(W_1,W_2,Y) + \frac{x_2}{x_1+x_2} \times f(W_2) \times g_{dual}(W_2,W_1,-Y)\right]$$

$$\frac{\partial g_{dual}(W_1,W_2,Y)}{\partial W_1} = \frac{\partial g_{dual}(W_1,W_2,Y)}{\partial W_2} = \frac{-m_4}{2H}\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4-1}$$

$$\frac{\partial g_{dual}(W_2,W_1,-Y)}{\partial W_1} = \frac{\partial g_{dual}(W_2,W_1,-Y)}{\partial W_2} = \frac{-m_4}{2H}\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4-1}$$

$$\frac{\partial g_{dual}(W_1,W_2,Y)}{\partial Y} = \frac{-m_4}{H}\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)-Y}{H}\right)^{m_4-1}$$

$$\frac{\partial g_{dual}(W_2,W_1,-Y)}{\partial Y} = \frac{m_4}{H}\left(\frac{S_0-0.5(W_1-W_0)-0.5(W_2-W_0)+Y}{H}\right)^{m_4-1}$$

$$\frac{\partial C_{s-dual}}{\partial W_1} = \frac{\partial C_s}{\partial W_1}$$

$$\frac{\partial C_{s-dual}}{\partial W_2} = \frac{\partial C_s}{\partial W_2}$$

$$\frac{\partial C_c}{\partial W_1} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2}\left(\frac{\partial f(W_1)}{\partial W_1} \times g_{dual}(W_1,W_2,Y) + \frac{\partial g_{dual}(W_1,W_2,Y)}{\partial W_1} \times f(W_1)\right) + \frac{x_2}{x_1+x_2}\left(\frac{\partial g_{dual}(W_2,W_1,-Y)}{\partial W_1} \times f(W_2)\right)\right]$$

$$\frac{\partial C_c}{\partial W_2} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2}\left(\frac{\partial g_{dual}(W_1,W_2,Y)}{\partial W_2} \times f(W_1)\right) + \frac{x_2}{x_1+x_2}\left(\frac{\partial f(W_2)}{\partial W_2} \times g_{dual}(W_1,W_2,Y) + \frac{\partial g_{dual}(W_2,W_1,-Y)}{\partial W_2} \times f(W_2)\right)\right]$$

$$\frac{\partial C_c}{\partial Y} = \varepsilon_{ox} \times \left[\frac{x_1}{x_1+x_2}\left(f(W_1) \times \frac{\partial g_{dual}(W_1,W_2,Y)}{\partial Y}\right) + \frac{x_2}{x_1+x_2}\left(f(W_2) \times \frac{\partial g_{dual}(W_2,W_1,-Y)}{\partial Y}\right)\right]$$

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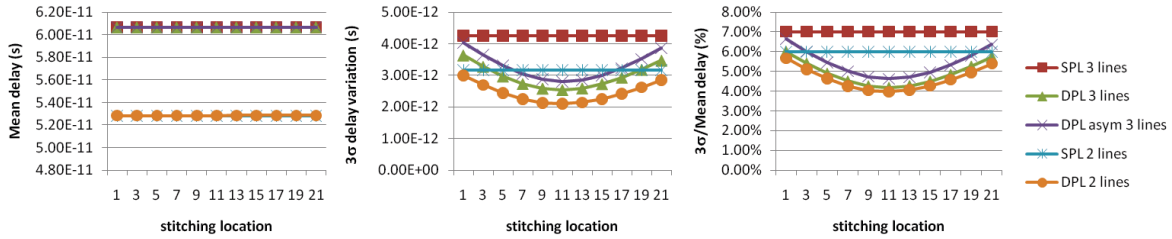
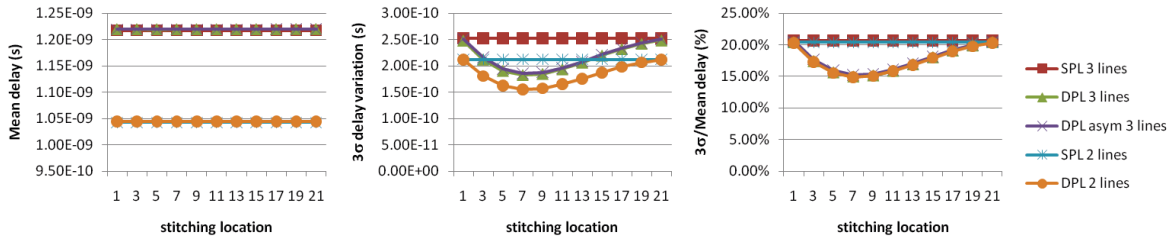
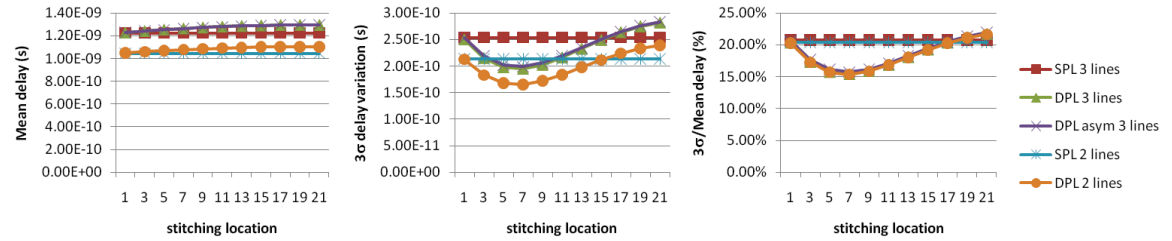


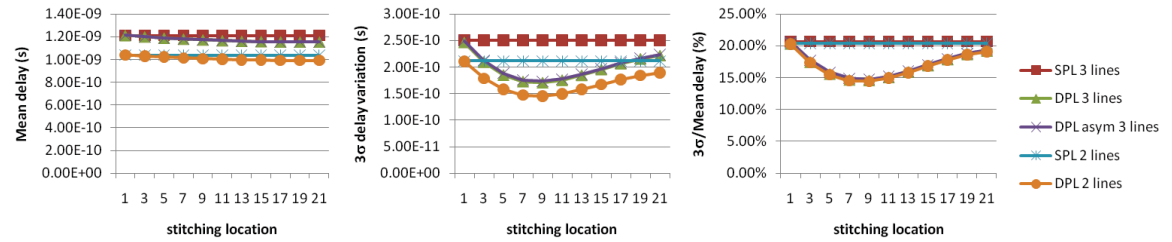
(a) 22*nm* technology, length = 100*um*, ΔCD mean = 0*nm*, inverter size = 1X.



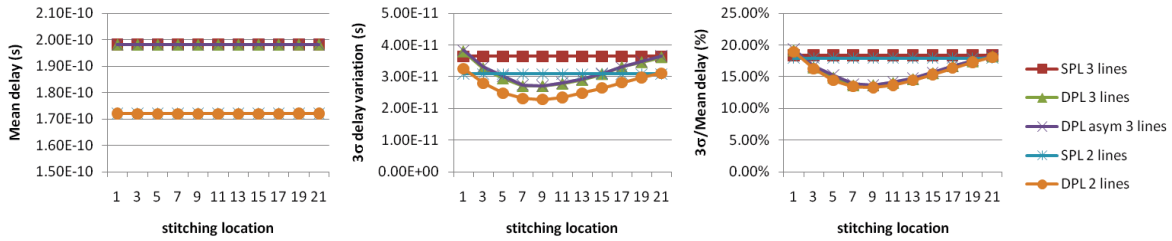
(b) 22*nm* technology, length = 1000*um*, ΔCD mean = 0*nm*, inverter size = 10X.



(c) 22*nm* technology, length = 1000*um*, ΔCD mean = -2*nm*, inverter size = 10X.



(d) 22*nm* technology, length = 1000*um*, ΔCD mean = 2*nm*, inverter size = 10X.



(e) 45*nm* technology, length = 1000*um*, ΔCD mean = 0*nm*, inverter size = 10X.

Figure 5: Average delay (rising and falling transitions) of an inverter and its variation due to interconnect.