Assessing Chip-Level Impact of Double Patterning Lithography

Kwangok Jeong[1], Andrew B. Kahng[1,2] and Rasit O. Topaloglu[3]
[1]ECE and [2]CSE Departments, University of California at San Diego, La Jolla, CA, USA
[3]GLOBALFOUNDRIES, Sunnyvale, CA, USA
kjeong@vlsicad.ucsd.edu, abk@cs.ucsd.edu, rasit.topaloglu@globalfoundries.com

***Abstract*—Double patterning lithography (DPL) provides an attractive alternative or a supplementary method to enable the 32*nm* and 22*nm* process nodes, relative to costlier technology options such as high refractive index materials, extreme ultraviolet (EUV), or e-beam lithography. DPL implements patterns on a single layer using either additional masks (e.g., double exposure or double patterning) or many additional processing steps (e.g., spacer double patterning). Overlay between the two layers introduces additional variability in both front-end-of-line (FEOL) and back-end-of-line (BEOL) by means of coupling capacitance variation. FEOL variability can be incorporated into standard characterization. However, the impacts of overlay in BEOL require new circuit analysis techniques. Furthermore, such techniques can guide technology developers toward DPL technology options that will have least variability impact on circuit performance.**

Today, the industry is nearing a critical juncture for choosing among various DPL technology options and process control capabilities. Accordingly, a rigorous, efficient framework is needed for variational performance analyses at chip level, and across many DPL technology options. Once a DPL method is chosen, a chip-level framework similar to what we present here will be required for circuit analysis and optimization. In this paper, we first analyze mechanisms of space and linewidth variation arising from overlay in various double patterning lithography options. We then develop a foundation of both TCAD-based and chip-level methods, along with an effective design of experiments, to assess electrical impacts of BEOL variations. We conclude with an assessment of relative viabilities of DPL technology options under a range of process control scenarios.

I. INTRODUCTION

Technology scaling to sub-45*nm* half-pitch has led to consideration of 193*nm* double patterning lithography (DPL) as an IC manufacturing technology option with cost and/or throughput advantages over EUV, e-beam and other next-generation possibilities. The ITRS [1] cites three DPL options:

- **Double exposure (DE).** DE consists of two successive exposures followed by a single etch. To suppress interference between exposures, a 'freezing' step may be used, resulting in a so-called litho-freeze litho-etch (LFLE) process [2] [6].
- **Double patterning (DP).** DP also requires two exposure steps, but each exposure is followed by an etch step, resulting in a litho-etch litho-etch (LELE) process. The main difference with respect to a DE process is the use of a second etch step.
- **Spacer double patterning (SDP).** After one exposure and etch on a hardmask, pattern doubling is accomplished by spacer formation and a second etch. The main idea of SDP is to utilize the space between a first set of printed features, dimensions of which are bloated by spacers. SDP is regarded as a viable option for regular poly gates [25] and bitlines [7] in recent memory processes. However, additional process steps for spacer generation, along with the cost of additional masks to trim undesired patterns, may be obstacles for irregular patterns [3] [25].

Sources of linewidth and linespace variation in DPL. According to SEMI standard P19 [22], *linewidth* is defined as, at a given cross-section of the line, the distance between the airline material boundaries at some specified height above the interface between the patterned layer in which the line is formed and the underlying layer. *Linespace* can be defined similarly, except the distance is measured between two lines.

In DE and DP, *overlay* causes linespace and linewidth variations. The sources of overlay are alignment error due to poor optics in the alignment system including reticle-to-tool alignment error and reticle-to-wafer alignment error; stepper-induced field errors including lens distortion, magnification and reticle rotations; wafer expansion or contraction; mask error; and nonlinear wafer deformation due to high temperature or stress in film deposition [5]. According to SEMI standard P18 [21], *overlay* is a vector quantity defined at every point on the wafer; it is the difference between a vector position in a substrate geometry and a vector position in an overlaying pattern. Linewidth and linespace variations due to overlay result in reliability and defect yield problems (open/short faults or electromigration-induced defects due to narrower overlaps between contacts and under-/overlying layers, etc.), as well as performance variations that cause loss of parametric yield. In SDP, spacer thickness and sidewall angle-induced footprint variation[1] result in linewidth and linespace variations.

Direct vs. indirect alignment. SEMI standard P18 [21] defines *alignment* as the mechanical positioning of reference points on the wafers ("alignment targets") to the corresponding points on the reticles. The measure of alignment is the overlay at the position on the wafer where the alignment targets are placed. Overlay in DPL can be measured and controlled in two ways, according to the alignment reference point: (1) indirect alignment (IA), and (2) direct alignment (DA). With DE or DP, (1) IA aligns the two masks for a given layer to a reference point in the underlying layer, while (2) DA aligns the second mask to the first mask [13]. DA and IA are illustrated in Figure

[1]Throughout this paper, we will refer to this as "spacer variation" for simplicity.

1, where dashed lines indicate alignment, and the reference layer may be a layer that has already been manufactured, such as a shallow trench isolation layer, or an interlayer dielectric layer.

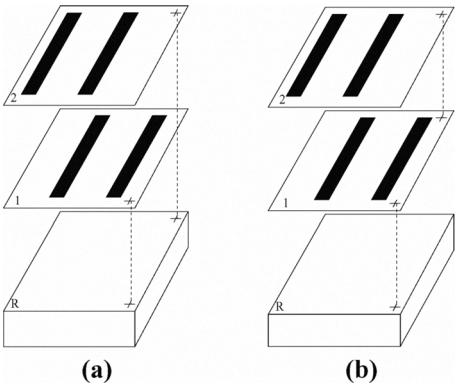

Fig. 1. Two masks (1 and 2) and a printed reference layer (R). (a) Indirect alignment. (b) Direct alignment.

Negative vs. positive photoresist. Double exposure (DE) and double patterning (DP) can be applied with either positive or negative photoresist processes. With positive photoresist in copper dual-damascene interconnect, trenches are patterned on the area exposed by light following the mask image, while with negative photoresist, trenches are patterned on the area not exposed by light. In this paper, we call the former 'P-DE' or 'P-DP' and the latter 'N-DE' or 'N-DP' following the type of photoresist.

With an SDP, mask patterns are transferred onto the hardmask but the hardmask itself does not convey the target patterns directly. Generated spacers, which define the drawn patterns (space or line), act analogously to photoresist. Hence, similar to the DE/DP processes, we define 'P-SDP' as the process that generates trenches in the area not under the spacers, and 'N-SDP' as the process that generates trenches in the area under the spacers.

We investigate the mechanisms of linewidth and linespace variation for known double patterning lithography techniques with different options, and thoroughly assess the impact on the electrical characteristics of interconnect, using simple structures to chip-level testcases. Our quantified comparisons of DPL technology options can guide designers or technologists to select the best technology option among the various choices of double patterning lithography based on performance.

The remainder of this paper is organized as follows. Section II briefly reviews the previous approaches on interconnect variational analysis. In Section III, we compare double patterning lithography briefly with traditional single patterning lithography. In Section IV, we analyze the impact of overlay on FEOL layers in standard cells, and the impact of via resistance variation due to overlay. We also provide our BEOL analysis setup for DPL process options. Section V provides the experimental flow and discusses the quantification of the impact of linewidth and linespace variation. We conclude the paper in Section VI with a summary of comparisons of the DPL methods.

II. PREVIOUS WORK

Interconnect variation due to process variation has been analyzed in a number of references. Mehrotra et al. [18] conduct a simulation-based study of the impact of manufacturing variation on interconnect performance. Lu et al. [17] provide a set of interconnect corner models using Monte Carlo simulations. Stine et al. [26] propose a practical methodology for determining the impact of interconnect pattern-dependent variation without using TCAD tools, and study the impact on simple circuit such as balanced clock networks and an SRAM array. Liu et al. [16] present a model order reduction technique for RLC interconnects including variational analysis based on matrix perturbation expansion theory.

Interconnect variation contributes to circuit delay uncertainty. Lin et al. [15] analyze circuit delay variation due to interconnect parameter variation using efficient experimental designs and sensitivity analysis. Narasimha et al. [19] study the effect of interconnect process variations induced by lithography and etch processes on crosstalk delay and noise. Venkatraman et al. [28] investigate the impact of process-induced parameter variation on global interconnects that require multi-level signaling with variational sensitivity parameters.

To relax the design constraints introduced by interconnect variations, [24] evaluates a tradeoff between capacitance and RC delay variation caused by fringing capacitances, and suggests a set of design guidelines for the interconnect structures that are insensitive to the process fluctuations. The authors of [11] develop additional matching rules to relax design pessimism via field solver analysis.

Laidler et al. [12] identify the sources of pattern distortions in FinFET technology and investigate overlay sources in [13]. Rigolli et al. [20] present the overlay budget for a double patterning lithography and propose an efficient overlay metrology. Yamamoto et al. [29] propose multi-layer reticle techniques with a single mask to reduce mask-to-mask overlay and mask cost. Sezginer et al. [23] develop a graphical method of visualizing the many-dimensional process window for double patterning lithography considering width and space variation from overlay.

A number of works have sought to quantify the impact of overlay in double patterning lithography, either analytically or empirically. The authors of [8] identify the impact of poly linewidth variation from DPL on design timing, and introduce the bimodal linewidth distribution problem in DPL. Ghaida et al. [4] quantify the impact on capacitance and RC delay of individual overlay components, and discuss the relative impact of each component. The impact of overlay in the coupling and total capacitance in BEOL double patterning lithography is addressed with TCAD simulations in [27]. Yang et al. [30] present capacitance and delay variation from overlay in double patterning lithography with analytical modeling of overlay and capacitance variation. In [9], we have recently conducted an experimental study on the impact of overlay in BEOL layers of a chip-level testcase; we also compare the impact of the overlay on design timing parameters (e.g., timing slack and coupling-induced delay variations) with other traditional interconnect variation sources. However, the impact of overlay on FEOL layers or different impact from different double

patterning lithography options is not analyzed in [9].

There is a need for variational chip-level simulation methodology for different DPL techniques. Furthermore, chip-level performance comparisons are needed to decide on which technology to give importance to in the near future.

III. PARAMETER VARIATIONS DUE TO DOUBLE PATTERNING LITHOGRAPHY

Various interconnect structures in a given interconnect layer interact with each other and form complicated electric fields. To account for these different interconnect structures during circuit design, capacitance tables for each pattern are utilized by designers or RC extractors. The capacitance tables are generated using two- or three-dimensional field solvers for various combinations of width and spacing to neighbors per each interconnect layer. Due to the different metal density and patterns, each pattern can have different process variation, so that widths and heights vary based on the context of patterns. Therefore, variational capacitance tables are required. We generate worst-case corners for each capacitance between interconnect pairs using statistical variation information from the semiconductor foundry per each width-height combination. First, we describe a methodology to generate a variational capacitance table for traditional single-patterning lithography.

TCAD-based BEOL analysis. There are four major parameters in the traditional interconnect variational analysis, i.e., interconnect width (W), height, space, and dielectric height. An interconnect has intralayer coupling capacitances C^{intra} with neighbor nets in the same layer, and interlayer coupling capacitances C^{up} and C^{down} with upper and lower layers.

Figures 2 and 3 show the variation impact due to overlay or spacer thickness variation for known DPL technologies. In the figures, interconnects are decomposed into *mask1* and *mask2*, and are marked with '1' and '2', correspondingly.

In Figure 2(a), we shift interconnects printed on *mask2* by a positive value of S to account for overlay in P-DE/DP. A negative value of S implies a shift in opposite direction for the edges of interconnects. Due to the shifting, intralayer coupling increases on one side of the interconnect but decreases on the other side. We shift a mask by overlay parameter S which varies from -3σ to 3σ with 1σ increments. Figure 2(b) shows the impact of overlay on N-DE/DP processes.

In Figures 3(a) and (b), we show the printed interconnects in P-SDP and N-SDP processes, respectively.[2]

Figure 4(a) shows the impact of rotational overlay on printed features with positive photoresist in DE/DP processes. Negative photoresist would not result in spacing errors due to a rotational overlay component. Figure 4(b) shows worst-case rotational impact, where features printed by both masks are inclined towards each other. Below, we conduct 3-dimensional TCAD analysis and compare the impact due to the rotational component of the overlay.[3]

[2] S is a parameter for overlay in DE/DP, for which the 3σ value is specified by lithography tool suppliers. For an SDP process, S is a parameter for the spacer thickness variation determined by manufacturers.

[3] While rotational error is already in the overlay budget, we separately study it in case it requires its own specification in future.

In assessing these double patterning lithography options, we may vary the width and pitch of the interconnects as necessary to simulate impact of overlay. We focus on the translational overlay component which appears to have the largest electrical impact [4].[4]

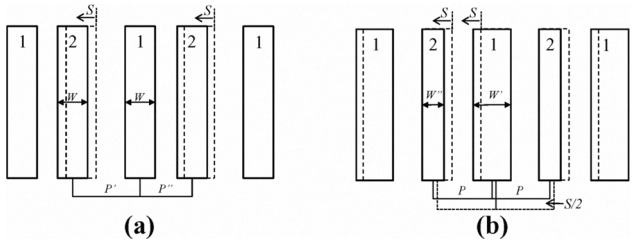

Fig. 2. (a) P-DE/DP process. Patterns printed using *mask2* are shifted by S due to overlay, which causes pitch and space variation between patterns (P" $\leq P \leq P$'). (b) N-DE/DP process. Overlay varies linewidth (W" $\leq W \leq W$'), but does not affect pitch and space.

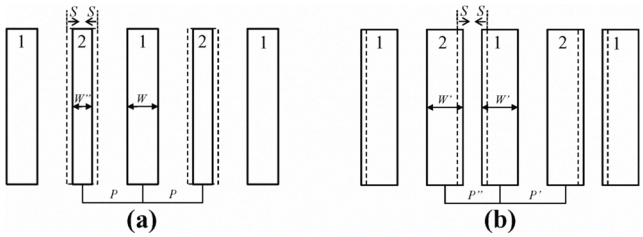

Fig. 3. (a) P-SDP process. Patterns printed after spacer formation can differ in width due to spacer thickness variations S (W" $\leq W$). Spacer thickness variation does not affect pitch but varies space. (b) N-SDP process. Linewidth, space and pitch are varied due to spacer thickness variation. (P" $\leq P \leq P$' and $W \leq W$'.)

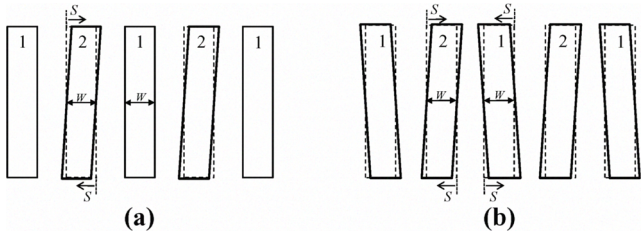

Fig. 4. (a) Rotational overlay due to *mask1* in DE/DP. (b) Worst-case rotational overlay due to *mask1* and *mask2* in different directions.

IV. CHIP-LEVEL ANALYSIS

We target FEOL and BEOL analysis separately as cell library characterization should be decoupled as much as possible from RC extraction in order to reduce design flow cycles. In this section, we explain the FEOL and BEOL analysis flows.

A. FEOL Analysis

To evaluate the impact of the overlay in double patterning lithography on the front-end-of-line (FEOL), we introduce overlay to FEOL layers, e.g., poly, contact, and M1, and measure delay variation.

We select the five most commonly instantiated standard cells in our testcase as implemented using the *Nangate 45nm*

[4] Although the translational overlay can be reduced by enhanced overlay control, complete elimination is not possible [1].

Open Cell Library [31], i.e., INV_X2, INV_X4, NOR2_X2, NOR2_X4 and NAND2_X2. These account for more than 60% of the instances in our testcase. We decompose each cell layout into five sub-layouts; '*BASE*' including diffusion, P+/N+ masks and n-well; '*P*1' and '*P*2' for odd and even poly lines counting from the leftmost cell boundary; '*C*' for contact layer; and '*M*' for M1 metal layer as shown in Figure 5. We then merge sub-layouts shifting each sub-layout by the amount {-3,-2,-1,0,1,2,3}σ of overlay of each layer. We shift patterns in the horizontal direction only, since the most important patterns for delay are the poly gates which are drawn in the vertical direction, and that have coupling to contacts and neighboring poly gates.[5]

We measure both rise and fall delay of the cells for all possible combinations of overlay between layers. The maximum impact of overlay on cell delay is as small as 2%, since the coupling capacitance between poly gate and contact or metal is very small, compared with gate capacitance due to less than 2*nm* thick gate oxide in a 45*nm* bulk technology.[6] Our FEOL analysis indicates that for this technology, FEOL variation will not be significant, and standard variability analysis techniques employed for library characterization will be sufficient. Hence, we focus our study on BEOL.

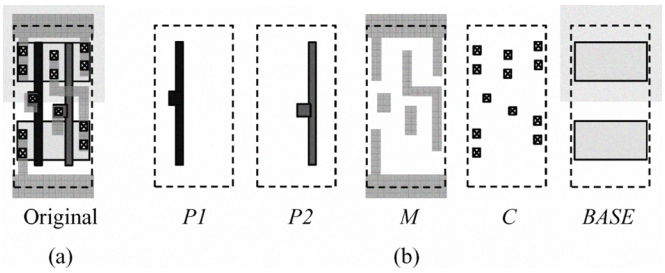

Fig. 5. Mask decomposition for FEOL overlay simulation. (a) Original NAND2_X2 cell layout. (b) Five decomposed sub-layouts.

B. Impact of Via Resistance Variation Due to Overlay

Due to the overlay between metal layers and via layers, via area enclosed by metal layer can be reduced, causing resistance increase as well as reliability problems such as electromigration. Thus, we also evaluate the impact on design timing of via resistance variation due to overlay.

In design-level analysis, traditional RC extractors use a resistance table defined in a technology file, e.g., Interconnect Technology File (ITF). We increase via resistance values, extract RC values from our testcase, and analyze timing. Detailed parameters of our testcase will be presented in Section V-C. We make the pessimistic assumption that via resistance can vary up to 2X from its original specification solely due to overlay. Table I summarizes timing variation due to this pessimistic, overlay-specific via resistance variation. We measure the critical path delay as well as total negative slack (TNS) of our testcase. From the table, we can observe that the impact of via resistance variation on timing is as small as 0.1%. Of course, these results are highly technology- and circuit-specific. If via resistance variation substantially impacts performance in a given technology and circuit, via resistances may be updated using enclosed areas as input in via resistance formulas.

TABLE I
CRITICAL PATH DELAY (*ns*) AND TOTAL NEGATIVE SLACK (*ns*) WITH THE ORIGINAL VIA RESISTANCE AND WITH 2× LARGER VIA RESISTANCE.

		Original	2×
Via resistance (Ω)	V1, V2	3.3	6.6
	V3, V4, V5	2.5	5.0
	V6	1.7	3.4
Critical Path Delay (*ns*)		4.994	4.999
Total Negative Slack (*ns*)		-140.995	-141.185

C. BEOL Analysis

We describe the BEOL variation analysis flow for different DPL options. We assume direct alignment (DA) for design-level overlay analysis, since IA is expected to have $\sqrt{2}$ times larger pattern shifts within a layer. In DE/DP with DA, we assume that 3σ overlay is S between two DPL masks. Although both masks can be shifted in arbitrary directions and by different amounts, shifts of *mask1* and *mask2* in opposite directions, orthogonal to the preferred routing direction, will induce worst-case space variation between patterns.[7] In SDP, we assume the 3σ spacer thickness variation to be $S/2$, so that the maximum CD variation from nominal is set to S as in DE/DP. From our TCAD studies, we have observed that interlayer coupling and via capacitances are insignificant. Therefore, we decrease the number of combinations by excluding the interlayer overlay.

Since the width and space variation differ for each double patterning lithography option, we use different design of experiments (DOE) for each.[8] As inputs of the DOEs, '$layer_{mask1}$' and '$layer_{mask2}$' denote two DPL masks for each DPL-applied BEOL '*layer*' from interconnect layers M2 to M5.

DOE for P-DE/DP. Assuming the width variation from resist or etch variation is sufficiently smaller than the overlay that it is negligible,[9] we perform simulations to analyze impact of space variation due to overlay. From the overlay S, one space increases by S while the other space decreases by S as shown in Figure 2(a). The DOE is given as:

1. **foreach** *layer* ∈ {M2, M3, M4, M5}
2. **foreach** $S \in$ {-3σ, -2σ, -1σ, 0σ, 1σ, 2σ, 3σ}
3. shift $layer_{mask1}$ by $+S/2$
4. shift $layer_{mask2}$ by $-S/2$
5. merge $layer_{mask1}$ and $layer_{mask2}$ with remaining layers
6. RC parasitic extraction and timing analysis

[5]Shifting patterns in the y-direction does not change space between the poly gates and neighboring contacts; thus, gate capacitance variation from y-direction overlay is expected to be smaller than that from x-direction overlay.

[6]Note that this delay variation is only from the parasitic capacitance variation due to the overlay. Overlay can amplify the poly and diffusion shape rounding after lithography, and channel-stress variation from contact overlay can have larger impact on delay than coupling capacitance variation. Yet, such effects are supposed to be embedded in silicon measurement data and the characterized library.

[7]The shift of the first mask is with respect to a reference layer similar to a traditional process. We apply necessary computations to ensure that overlay between *mask1* and *mask2* meets ITRS guidelines.

[8]We use the term DOE to indicate a set of experiments to evaluate a process variation scenario.

[9]CD control requirement in DRAM at the 32*nm* half-pitch technology node is 3.3*nm*, which is around half of the overlay control requirement 6.4*nm* in ITRS 2008 [1].

DOE for N-DE/DP. Overlay S contributes to width increase for patterns in DPL *mask1* by S and width decrease of patterns in DPL *mask2* by S. However, the space between patterns in different DPL masks remains nominal as shown in Figure 2(b). The DOE is given as:

1. **foreach** *layer* $\in$ {M2, M3, M4, M5}
2. **foreach** $S \in \{-3\sigma, -2\sigma, -1\sigma, 0\sigma, 1\sigma, 2\sigma, 3\sigma\}$
3. shift $layer_{mask1}$ by $+S/2$
4. resize $layer_{mask1}$ by $+S$
5. shift $layer_{mask2}$ by $+S/2$
6. resize $layer_{mask2}$ by $-S$
7. merge $layer_{mask1}$ and $layer_{mask2}$ with remaining layers
8. RC parasitic extraction and timing analysis

DOE for P-SDP. Due to the spacer thickness variation by $S/2$, the width of the even patterns that are generated by the space between spacers in Figure 3(a) can change by S (two times $S/2$). Since there is no pitch change in P-SDP, when the width of the even patterns increases (decreases) by S, space between adjacent patterns decreases (increases) by $S/2$. The DOE is given as:

1. **foreach** *layer* $\in$ {M2, M3, M4, M5}
2. **foreach** $S \in \{-3\sigma, -2\sigma, -1\sigma, 0\sigma, 1\sigma, 2\sigma, 3\sigma\}$
3. resize $layer_{mask1}$ by 0
4. resize $layer_{mask2}$ by S
5. merge $layer_{mask1}$ and $layer_{mask2}$ with remaining layers
6. RC parasitic extraction and timing analysis

DOE for N-SDP. In N-SDP, spacer thickness variation results in width variation of all lines, and in pitch variation as shown in Figure 3(b). We resize adjacent lines by $S/2$ to represent the global width variation, and then shift adjacent lines that are facing each other with the varying edges by $S/4$ to represent the pitch variation. The DOE is given as:

1. **foreach** *layer* $\in$ {M2, M3, M4, M5}
2. **foreach** $S \in \{-3\sigma, -2\sigma, -1\sigma, 0\sigma, 1\sigma, 2\sigma, 3\sigma\}$
3. resize $layer_{mask1}$ by $+S/2$
4. shift $layer_{mask1}$ by $+S/4$
5. resize $layer_{mask2}$ by $+S/2$
6. shift $layer_{mask2}$ by $-S/4$
7. merge $layer_{mask1}$ and $layer_{mask2}$ with remaining layers
8. RC parasitic extraction and timing analysis

With the output RC parasitic files, we analyze timing and capacitance variations for individual nets, and the timing of the whole design. Detailed analysis will be discussed in Section V.

V. EXPERIMENTAL RESULTS

A. Interconnect Analysis Setup

We use a FEOL and BEOL layer stack and design rules that reflect a representative $45nm$ technology, based on the ITRS [1], as shown in Table II. We use 20% of nominal interconnect width as the 3σ variation of overlay,[10] and use 3.3 as the effective dielectric constant for all dielectric materials.

[10]The value of 20% is taken from the ITRS 2008 update [1]. The 2009 ITRS edition is being released just as this paper is being finalized. We will be updating our studies based on the new estimates.

TABLE II
TECHNOLOGY STACK PARAMETERS.

Layer	W_{nom}	H_{nom}	D_{nom}
poly	$45nm$	$80nm$	$160nm$
M1	$52nm$	$94nm$	$94nm$
M2	$52nm$	$94nm$	$94nm$
M3$\sim$M5	$68nm$	$122nm$	$122nm$
M6, M7	$104nm$	$188nm$	$188nm$
3σ variation	$W_{3\sigma}$	$H_{3\sigma}$	$D_{3\sigma}$
M2$\sim$M5	$13.6nm$	$24.4nm$	$24.4nm$

B. Interconnect Capacitance Tables

We conduct experiments across various DPL options to be able to compare these options in terms of capacitance values. We also compare the impact of overlay with that of width variation, which is one of the traditional variation sources.

In Table III, the only variation source is the overlay. Similarly, in different rows, we compare width only, height only, or all variation sources including dielectric thickness. C^{down}, C^{top}, and C^{intra} are the capacitances to the lower, upper, and intralayer interconnects, respectively. C^{total} is the total capacitance. Subscripts *min*, *nom*, and *max* indicate minimum, nominal and maximum cases, respectively. Since each value is found as a maximum value among all the DOE results, the summation of partial coupling capacitance may not match with the total capacitance.

We observe that positive photoresist process with direct alignment (*DA*) results in similar capacitance impact due to overlay or width variations. We also observe *IA* results in larger capacitance changes as compared to *DA* cases for positive photoresist case.

We conduct 3-dimensional TCAD field solver analysis using the setup in Figure 4. Upper and lower layers contain orthogonal interconnects with same width and spacing and no overlay. We use 500,000 grid points, and use the same technology and dimensions with $1\mu m$ lines. In Figure 4(a), coupling between the middle interconnect and one of its immediate neighbors increases by only 0.3% due to rotational overlay. Figure 4(b) provides the worst case, where the impact rises to 2.82%. We conclude that rotational overlay is not as significant, as one section of a line would get closer to, while the remaining section would move away from, an intralayer neighbor. The magnification component is similar to width variations; hence, we focus on the translational component of overlay.

Intralayer coupling capacitance correlates quite well to noise or coupling-induced delay at the circuit level. Total capacitances, on the other hand, correlate well with circuit delay.

C. Chip-Level Analysis Setup

Traditional parasitic extraction tools directly read a design database (e.g., design exchange format (DEF), GDS, etc.), and use capacitance tables that contain width or height variations of metal or dielectric layers. To account for overlay in extraction, we present a new RC extraction flow for double patterning lithography as shown in Figure 6. Details of the flow are as follows.[11]

1. Initial GDS. We stream out GDS from a routed design.

[11]Although we perform exhaustive analysis for the purpose of technology selection, use of our framework for DPL variability analysis targets worst-case corners only, thereby reducing the number of simulations.

TABLE III
CAPACITANCE ($aF/\mu m$) RESULTS.

Configuration	C_{min}^{down}	C_{nom}^{down}	C_{max}^{down}	C_{min}^{top}	C_{nom}^{top}	C_{max}^{top}	C_{min}^{intra}	C_{nom}^{intra}	C_{max}^{intra}	C_{min}^{total}	C_{nom}^{total}	C_{max}^{total}
P-DE/DP, *DA*, Overlay Only	31	31	31	31	31	31	56	68	85	200	200	205
P-DE/DP, *DA*, Width Only	30	31	31	31	31	32	56	68	86	174	200	222
P-DE/DP, *DA*, All Variations	25	31	39	26	31	40	36	68	135	152	200	283
P-DE/DP, *IA*, Overlay Only	31	31	31	31	31	31	52	68	95	200	200	210
P-DE/DP, *IA*, Width Only	30	31	31	31	31	32	56	68	86	174	200	222
P-SDP, Spacer Thickness Only	29	31	31	30	31	31	61	68	76	189	200	200
P-SDP, All Variations	25	31	40	25	31	41	49	68	90	165	200	236
N-DE/DP, *DA*, Overlay Only	27	31	33	28	31	34	68	68	68	192	200	204
N-DE/DP, *DA*, Height Only	31	31	31	31	31	32	57	68	79	178	200	214
N-DE/DP, *DA*, All Variations	22	31	43	23	31	44	44	68	102	145	200	271
N-DE/DP, *IA*, Overlay Only	26	31	34	27	31	35	68	68	68	189	200	206
N-DE/DP, *IA*, Height Only	31	31	31	31	31	32	57	68	79	178	200	214
N-SDP, Spacer Thickness Only	30	31	31	31	31	31	56	68	68	187	200	200
N-SDP, All Variations	26	31	38	26	31	39	44	68	99	163	200	242

2. Split GDS. We generate a base GDS that only has all front-end-of-line (FEOL) layers, i.e., n-well, active, p-implant, along with larger-dimension interconnect layers that do not use double patterning lithography, and sub-GDS files for double patterning-applied layers. We assume that double patterning lithography is applied to local interconnect layers which use stricter design rules.

3. Pattern decomposition for double patterning lithography. For local interconnect layers, we generate two sub-GDS files from a decomposition of the original layout using integer linear programming-based min-cost coloring [10]. Finally, patterns in each local layer are split into two masks, $layer_{mask1}$ and $layer_{mask2}$.

4. Shift and merge. To model interconnect parameter variations due to overlay, each sub-GDS in each layer is overlaid with a different origin point on top of the base GDS. For instance, to model a $-10nm$ translational overlay for M2 layer's first double patterning mask ($M2_{mask1}$), we locate the sub-GDS containing the $M2_{mask1}$ at ($-10nm$, $0nm$) in the coordinate system of the base GDS. To shift and merge GDS files, we use SKILL scripts with the *Cadence Virtuoso Layout Design Environment IC6.1.0.243* [37].

5. Resize and extraction. We use the *SIZE* command in *Synopsys Hercules(v2006.12-8)* to expand or shrink original patterns to account for width variation from overlay. After width change, the *BOOLEAN OR* command is used to merge two double patterning mask layers. Finally, we use *Synopsys STAR-RCXT v2007.06* [33] for RC extraction.

We implement from RTL the open-source core *AES*, obtained from *opencores.org* [32]. With $4ns$ clock cycle time, we synthesize, place and route the testcase with *Nangate* $45nm$ open cell library [31] using *Cadence RTL Compiler v5.2* [36] and *Cadence SOC Encounter v7.2* [38]. The final implemented *AES* has 86% placement utilization with 26,069 standard cell instances, and average 10% (maximum 14%) metal density with no metal fill insertion.[12] We also implement another testcase with floating track-type dummy fill to observe the impact of overlay in a manufacturing-ready design. Average and maximum metal density with metal fill are 37% and 46% for all routing layers, respectively.

[12]Metal density is calculated for only signal routing layers. The maximum metal density value for signal nets is 50%, when all routing tracks are occupied.

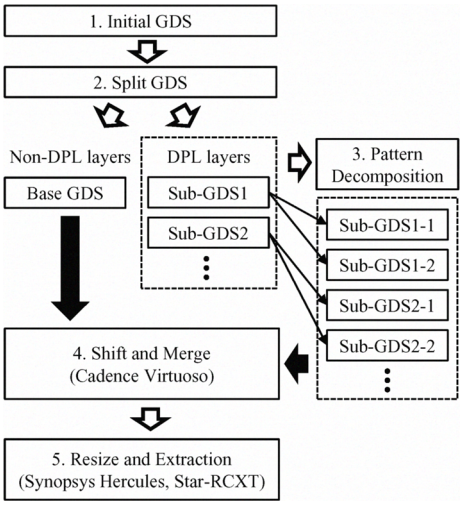

Fig. 6. Extraction flow for double patterning lithography considering overlay.

For the BEOL stack of the chip-level design, we use five small-dimension metal layers (M1-M5), and two large-dimension metal layers (M6 and M7) as shown in Table II. We do not include the variation in FEOL, since the impact of overlay in FEOL needs to be included in cell characterization and library generation. Due to the minimum precision of $1nm$ for the layout editor, we use $12nm$ for 3σ of overlay or spacer thickness variability S for design-level analysis, instead of the $10.4nm$ that is 20% of M1 width.

D. Chip-Level Analysis Results

Our first analysis compares the coupling-induced delay variation due to overlay. We use *Synopsys PrimeTime-SI vB-2008.12-SP2* [35] as a standard coupling-aware delay calculator which takes into account the amount of cross-coupled capacitance and relative arrival times. This tool also considers slew rates of all signal transitions, switching directions, and combined effects of all aggressors on a victim net. After logical and electrical filtering using functional checking and timing window comparisons, coupling capacitances greater than a specific threshold value are considered during the coupling noise analysis.

We identify the net with largest coupling-induced delay in the nominal design. This net consists of three interconnect segments: $1.604\mu m$ of M2, $0.78\mu m$ of M3 and $14.788\mu m$ of M4 segments. The M2 segment has a same-layer neighbor

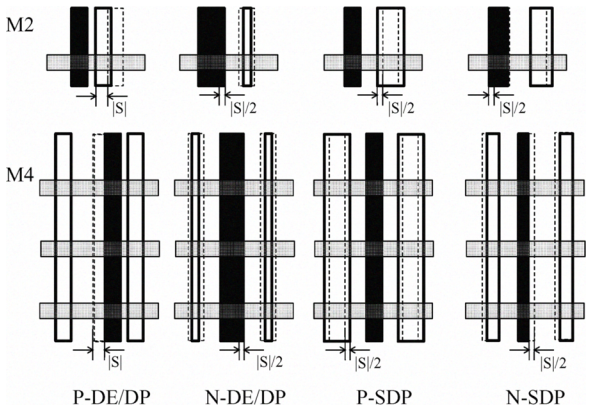

Fig. 7. Simplified configurations of a net having the largest coupling-induced delay variation in the testcase before metal fill.

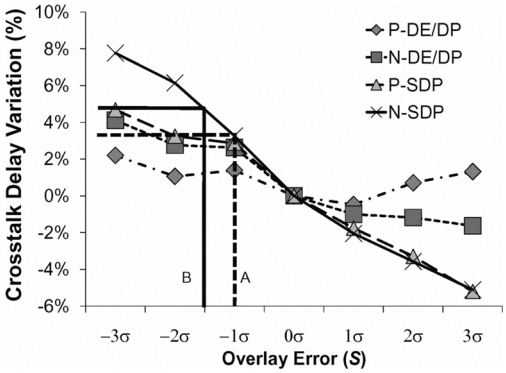

Fig. 8. Coupling-induced delay variation (%) in y-axis due to M4 overlay in x-axis.

with minimum spacing on the right-hand side. Two M1 nets and three M3 nets cross the M2 segments. The M3 segment does not have any neighbor with minimum spacing. The M4 segment has neighbors at minimum spacing on both sides. 26 M5 nets and 31 M3 nets cross the M4 segment. Figure 7 illustrates simplified configurations of the selected nets, with negative variation of S, for each DPL technique. Black boxes and white boxes with solid boundaries denote the selected net (victim) and neighbors (aggressors) in the same layer, respectively. The boxes with dotted boundaries represent the original patterns without variations, and the orthogonal gray boxes represent the aggressors in upper or lower layers. From the layout configurations, we expect that intralayer coupling will dominate for the M2 segment, and that both interlayer and intralayer coupling will affect coupling-induced delay variation.

The number of aggressors after filtering is five, and the aggressors are connected to the victim net via 27 coupling capacitances. Coupling-induced delay change without metal fill ('w/o metal fill') and with metal fill ('w/ metal fill') at the nominal corner ($S = 0$) is $364ps$ and $292ps$, respectively. After metal fill insertion, total capacitance of the net increases from $2.946fF$ to $3.023fF$. However, in 'w/ metal fill', ground capacitance increases from $1.087fF$ to $1.385fF$, but coupling capacitance decreases.

We now discuss in detail, by way of example, the coupling-induced delay variation with M4 overlay error.[13] Figure 8 shows the coupling-induced delay variation with different M4 overlay bounds.

- **P-DE/DP.** For the selected victim net, linewidth does not change but the space between aggressors and the victim changes. For M4 overlay, with both negative and positive S, the coupling-induced delay increases. This is because the capacitance increase due to neighbor nets on one side is larger than the capacitance decrease with neighbors on both sides.
- **N-DE/DP.** Since the space between intralayer aggressors and the victim does not change, coupling capacitance variation with respect to intralayer aggressors is small. However, linewidth increase (decrease) of the victim net amplifies (decreases) ground capacitance and interlayer coupling. For the M4 segment, negative (positive) S results in linewidth increase (decrease) of the victim net as shown in Figure 7. Coupling-induced delay due to the large number of neighbors on upper and lower layers, increases (decreases) with linewidth increase (decrease).
- **P-SDP.** For this specific victim net, the M4 segment consists of the patterns underlying the primary patterns in the first litho-etch step of the SDP process. Negative (positive) S leads to smaller (larger) spacer thickness which results in smaller (larger) space between the victim and aggressors. Therefore, coupling-induced delay increases with negative S and decreases with positive S. Since the spaces on both sides of the M4 segment are increased or decreased at the same time, the impact of overlay in P-SDP is larger than that of DE or DP.
- **N-SDP.** The space on one side of the M4 segment changes, causing intralayer coupling variation. The width of the victim also changes, causing interlayer coupling variation. Positive S leads to linewidth increase and spacing decrease, so that the coupling-induced delay increases. Negative S leads to linewidth decrease as well as spacing increase as shown in Figure 7, so that the coupling-induced delay variation decreases. Note that in Figure 8, we inversely plot N-SDP results against S, to juxtapose delay variations against those of other options. Since intralayer and interlayer couplings vary together in the same direction, overlay impact in N-SDP can be larger than in P-SDP.

From Figure 8, we can observe the relative significance of the overlay control requirement for each option.

1) P-DE/DP has the smallest variation from overlay. With the same 3σ overlay control, the variations in P-DE/DP, N-DE/DP, P-SDP and N-SDP are 2.20%, 4.11%, 4.68% and 7.77%, respectively. This implies that the overlay control requirement for P-DE/DP can be relaxed compared to the other technology options.
2) If overlay control in N-SDP is relatively easy, such that

[13] Coupling-induced delay variation due to M2 overlay is smaller than that due to M4 overlay, and the impact of overlay in M3 and M5 layers contributed by interlayer coupling variation is around ±1%.

it can be controlled within 1σ,[14] then the overlay control requirement for P-SDP and N-DE/DP must be within 2σ to have a similar level of variation in N-SDP, e.g., 3.26% variation, as indicated by the dotted line 'A'.

3) The overlay control requirement for N-SDP should be twice as tight as for the others. For instance, if we target 3σ overlay for N-DE/DP or P-SDP, the overlay control for N-SDP must be within 1.5σ to have variation similar to N-DE/DP or P-SDP, as indicated by the solid line 'B'.

Our second analysis compares capacitance variation due to overlay. Figure 9 shows interconnect capacitance changes of the top 5,307 high-capacitance nets ($\geq 2fF$) of the 'w/o metal fill' testcase. We measure maximum increase, maximum decrease and mean variation, by comparing extracted parasitic files. In most cases, we observe more than 10% increase or decrease of capacitances from the nominal capacitance values. Such increases and decreases of capacitances will contribute to larger on-chip variations in timing analysis.

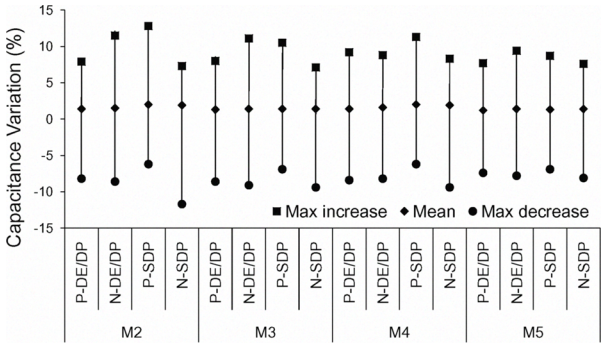

Fig. 9. Capacitance changes (%) of high-capacitance nets ($\geq 2fF$) from 3σ overlay.

Our third analysis compares the impact of overlay on design timing. We use total negative slack (TNS), which is the sum of timing slack values at all endpoints in static timing analysis, as a metric to quantify design timing. Figure 10 shows the normalized TNS of the worst-case corner ($S = \pm 3\sigma$) with respect to the TNS of the nominal corner ($S = 0$). Values on the y-axis give the relative variation from the TNS value of the nominal corner (1.0). The total negative slack in the nominal corner is -63*ns* without metal fill and -83*ns* with metal fill.

From the TNS variation analysis, we observe that P-SDP and N-SDP options have greater sensitivity to the overlay than DE/DP, since both linewidths and spaces are varied in P-SDP and N-SDP. Figure 11 shows the relative sensitivity of double patterning lithography options with respect to overlay. We observe that both P-SDP and N-SDP are more sensitive than DE/DP with the same overlay, and that the lower layer (M2), which uses smaller-dimension design rules, is more sensitive than higher layers with larger-dimension design rules.

VI. CONCLUSIONS

We have provided a variational interconnect analysis framework for double patterning lithography, taking overlay into account. We have applied our framework to testcases ranging from a small representative interconnect structure to chip-level designs based on a 45*nm* technology, with golden extraction and timing analysis tools.

We obtain the following conclusions, which may help process technology developers to assess double patterning lithography options in terms of chip-level performance and variability.

1) Overlay with indirect alignment (IA) results in higher capacitance variations than direct alignment (DA) in DE or DP.
2) For all DPL techniques, more than 10% interconnect capacitance variation can occur due to overlay or spacer thickness variation.
3) Design timing can be significantly degraded due to the large capacitance variation, e.g., up to 13% worse total negative slack in N-SDP with 3σ of spacer thickness variation.
4) SDP may require track fills for metal fills for chemical-mechanical polishing constraints. Hence, performance degradation due to fill may be larger for SDP in production designs. Furthermore, mask coloring and design will be difficult. SDP has tighter variability control, but

[14]Spacer thickness variation in SDP can be much less than overlay in DE/DP, e.g., 1/3 of the overlay control spec in DE/DP, since spacer thickness is controlled by well-controlled oxide growth, deposition and thinning rates.

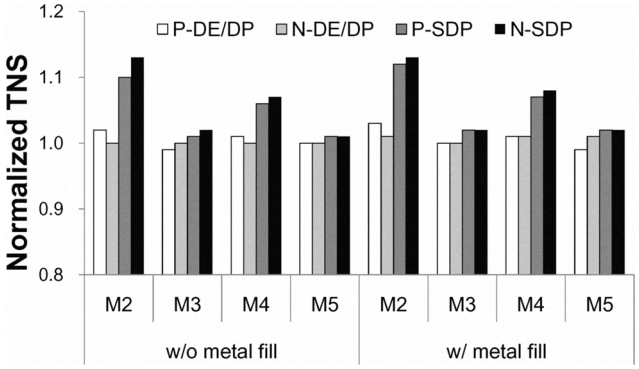

Fig. 10. Normalized total negative slack in y-axis due to 3σ overlay in each layer in x-axis for each double patterning lithography option.

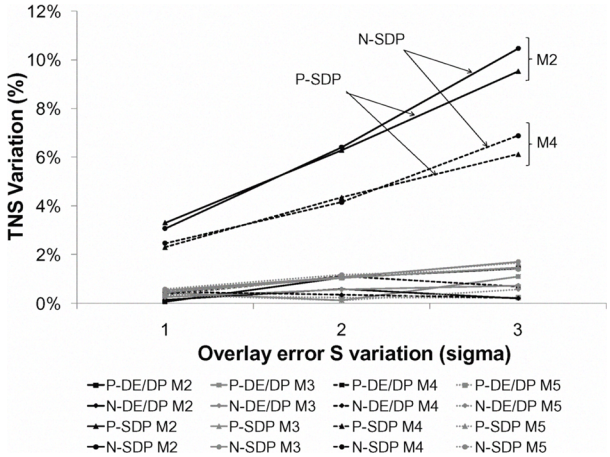

Fig. 11. Total negative slack variation (%) from the nominal value in each double patterning lithography option with respect to overlay *S* variation.

is an expensive option in terms of design rules and restrictions.

5) Given the potential disadvantages of SDP, P-DE/DP may be the most favorable option for BEOL double patterning lithography based on performance. With the same 3σ variation control ($12nm$), the coupling-induced delay variation in P-DE/DP is half that of N-DE/DP.
6) When variation specifications differ, e.g., 3σ for DE/DP and 1σ for SDP, the amounts of coupling-induced delay variation can be similar. Designers and lithographers must then consider design cost and cost of ownership associated with these technology options.

Our study of overlay impacts may shed light onto which technology should be preferred, at least from a performance-oriented perspective. Furthermore, the framework we provide for DPL variability analysis can be used in the analysis and optimization of interconnects once a particular DPL method is chosen as a technology.

VII. ACKNOWLEDGMENTS

The authors thank Dr. Harry J. Levinson, Dr. Jongwook Kye and Dr. Yuansheng Ma of GLOBALFOUNDRIES for discussions on double patterning lithography, and Prof. Puneet Gupta and Mr. Rani S. Ghaida of UCLA for discussions on overlay.

REFERENCES

[1] *International Technology Roadmap for Semiconductors 2008 Update*, 2008.
[2] K.-J. R. Chen, W.-S. Huang, W.-K. Li and P. R. Varanasi, "Resist Freezing Process for Double-Exposure Lithography", *Proc. SPIE Advances in Resist Materials and Processing Technology XXV*, Vol. 6923, 2008, pp. 69230G-1–69230G-10.
[3] T.-B. Chiou, R. Socha, H.-Y. Kang, A. C. Chen, S. Hsu, H. Chen and L. Chen, "Full-Chip Pitch/Pattern Splitting for Lithography and Spacer Double Patterning Technologies", *Proc. SPIE Lithography Asia*, Vol. 7140, 2008, 71401Z-1–71401Z-12.
[4] R. S. Ghaida and P. Gupta, "Design-Overlay Interactions in Metal Double Patterning", *Proc. SPIE Design for Manufacturability through Design-Process Integration III*, Vol. 7275, 2009, pp. 727514-1–727514-10.
[5] J. N. Helbert, *Handbook of VLSI Microlithography: Principles, Technology, and Applications*, 2nd ed., Park Ridge, N.J., Noyes Publications; Norwich, N.Y., William Andrew Publishing, 2001.
[6] M. Hori, T. Nagai, A. Nanamura, T. Abe, G. Wakamatsu, T. Kakizawa, Y, Anno, M. Sugiura, S. Kusumoto, Y. Yamaguchi and T. Shimokawa, "Sub-40-nm Half-Pitch Double Patterning with Resist Freezing Process", *Proc. SPIE Advances in Resist Materials and Processing Technology XXV*, Vol. 6923, 2008, pp. 69230H-1–69230H-8.
[7] B. Hwang, N. Lim, J.-H. Park, S. Jin, M. Kim, J. Jung, B, Kwon, J. Hong, J. Han, D. Kwak, J. Park, J. Choi and W.-S. Lee, "Development of 38nm Bit-Lines using Copper Damascene Process for 64-Giga bits NAND Flash", *Proc. Advanced Semiconductor Manufacturing Conference*, 2008, pp. 49–51.
[8] K. Jeong and A. B. Kahng, "Timing Analysis and Optimization Implications of Bimodal CD Distribution in Double Patterning Lithography", *Proc. Asia South Pacific Design Automation Conference*, 2009, pp. 486–491.
[9] K. Jeong, A. B. Kahng and R. O. Topaloglu, "Is Overlay Error More Important Than Interconnect Variations in Double Patterning?", *Proc. Workshop on System-Level Interconnect Prediction*, 2009, pp. 3–10.
[10] A. B. Kahng, C.-H. Park, X. Xu and H. Yao, "Layout Decomposition for Double Patterning Lithography", *Proc. International Conference on Computer-Aided Design*, 2008, pp. 465–472.
[11] A. B. Kahng and R. O. Topaloglu, "Generation of Design Rule Guarantees for Interconnect Matching", *Proc. Workshop on System-Level Interconnect Prediction*, 2006, pp. 29–34.
[12] D. Laidler, "Identifying Sources of Overlay Error in FinFET Technology", *Proc. SPIE Metrology, Inspection, and Process Control for Microlithography XIX*, Vol. 5752, 2005, pp. 80–90.
[13] D. Laidler, P. Leray, K. D'Have and S. Cheng, "Sources of Overlay Error in Double Patterning Integration Schemes", *Proc. SPIE Metrology, Inspection, and Process Control for Microlithography XXII*, Vol. 6922, 2008, pp. 69221E.1–69221E.11.
[14] H. J. Levinson, *Principles of Lithography*, 2nd ed., Bellingham, WA, SPIE, 2005.
[15] Z. J. Lin and C. J. Spanos, "Sensitivity Study of Interconnect Variation Using Statistical Experimental Design", *Proc. Workshop on Statistical Metrology*, 1998, pp. 68–71.
[16] Y. Liu, L. T. Pileggi and A. J. Strojwas, "Model Order-Reduction of RC(L) Interconnect Including Variational Analysis", *Proc. Design Automation Conference*, 1999, pp. 201–206.
[17] N. Lu, "Statistical and Corner Modeling of Interconnect Resistance and Capacitance", *Proc. Custom Integrated Circuits Conference*, 2006, pp. 853–856.
[18] V. Mehrotra, S. Nassif, D. Boning and J. Chung, "Modeling the Effects of Manufacturing Variation on High-Speed Microprocessor Interconnect Performance", *Proc. International Electron Devices Meeting*, 1998, pp. 767–770.
[19] U. Narasimha, B. Abraham and N. S. Nagaraj, "Statistical Analysis of Capacitance Coupling Effects on Delay and Noise", *Proc. International Symposium on Quality Electronic Design*, 2006, pp. 795-800.
[20] P. Rigolli, C. Turco, U. Iessi, G. Capetti and P. Canestrari, "Double Patterning Overlay Budget for 45nm Technology Node Single and Double Mask Approach", *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer structures* 25(6) (2007), pp. 2461-2465.
[21] SEMI P18-92 (Reapproved 1104), "Specification for Overlay Capabilities of Wafer Steppers", http://www.semi.org/.
[22] SEMI P19-92 (Reapproved 0707), "Specification for Metrology Pattern Cells for Integrated Circuit Manufacture", http://www.semi.org/.
[23] A. Sezginer, B. Yenikaya and W. Staud, "Double Patterning Technology: Process-Window Analysis in a Many-Dimensional Space", *Proc. SPIE Photomask and Next-Generation Lithography Mask Technology XIV*, Vol. 6607, 2007, pp. 66072S-1–66072S-9.
[24] N. Shigyo, "Variations of Interconnect Capacitance and RC Delay Induced by Process Fluctuations", *Proc. Workshop on Statistical Metrology*, 2000, pp. 68-71.
[25] W. Shiu, W. Ma, H. W. Lee, J. S. Wu, Y. M. Tseng, K. Tsai, C. T. Liao, A. Wang, A. Yau, Y. R. Lin, Y. L. Chen, T. Wang, W. B. Wu and C. L. Chiang, "Spacer Double Patterning Technique for Sub-40nm DRAM Manufacturing Process Development", *Proc. SPIE Lithography Asia*, Vol. 7140, 2008, pp. 71403Y-1–71403Y-8.
[26] B. E. Stine, V. Mehrotra, D. S. Boning, J. E. Chung and D. J. Ciplickas, "A Simulation Methodology for Assessing the Impact of Spatial/Pattern Dependent Interconnect Parameter Variation on Circuit Performance" *Proc. International Electron Devices Meeting*, 1997, pp. 133–136.
[27] R. O. Topaloglu, "Variational Interconnect Analysis for Double Patterning Lithography", *Proc. International VLSI Multilevel Interconnection Conference*, 2008, pp. 267–270.
[28] V. Venkatraman and W. Burleson, "Impact of Process Variations on Multi-Level Signaling for On-Chip Interconnects", *Proc. International Conference on VLSI Design*, 2005, pp. 362–367.
[29] Y. Yamamoto, R. Rigby and J. Sweis, "Multi-Layer Reticle (MLR) Strategy Application to Double-Patterning/ Double-Exposure for Better Overlay Error Control and Mask Cost Reduction", *Proc. SPIE Photomask Technology*, Vol. 6730, 2007, 67302X-1–67302X-12.
[30] J.-S. Yang and D. Z. Pan, "Overlay Aware Interconnect and Timing Variation Modeling for Double Patterning Technology", *Proc. International Conference on Computer-Aided Design*, 2008, pp. 488–493.
[31] *NANGATE*, http://www.nangate.com/.
[32] *OPENCORES.ORG*, http://www.opencores.org/.
[33] *Synopsys STAR-RCXT User's Manual.* http://www.synopsys.com/Tools/Implementation/SignOff/Pages/Star-RCXT.aspx.
[34] *Synopsys Hercules User's Manual.* http://www.synopsys.com/Tools/ Implementation/PhysicalVerification/Pages/Hercules.aspx.
[35] *Synopsys PrimeTime User's Manual.* http://www.synopsys.com/Tools/Implementation/SignOff/Pages/PrimeTime.aspx.
[36] *Cadence RTL Compiler User's Manual.* http://www.cadence.com/eu/Pages/rtl_compiler.aspx.
[37] *Cadence Virtuoso Layout Design Environment User's Manual.* http://www.cadence.com/ products/cic/pages/.
[38] *Cadence SOC Encounter User's Manual.* http://www.cadence.com/products/di/soc_encounter/Pages/.