Predictive Modeling of Lithography-Induced Linewidth Variation

Andrew B. Kahng† and Swamy V. Muddu‡
† CSE and ‡† ECE Departments, UCSD, La Jolla, CA 92093
abk@cs.ucsd.edu, swamy@vlsicad.ucsd.edu

ABSTRACT

Despite advanced resolution enhancement techniques (RET) and illumination techniques, several sources of variation in the pattern transfer process manifest as variations in chip-level performance and power. At 45nm and below, accurate design-level performance and power analyses must consider litho-simulated non-idealities. However, lithography simulation is computationally expensive to perform at chip-scale, and essentially infeasible during iterative design optimization. In this work, we develop a predictive model of device linewidths after optical proximity correction (OPC) across the process window. The predictive model is fast, accurate and highly scalable, enabling its use in the design phase at full-chip scale without actually performing OPC and litho simulation.

To model litho effects on 2D poly geometries in standard cell layouts, we rigorously identify layout parameters that affect the litho contour. We classify gate poly (devices) into different categories based on their geometric parameters as well as those of neighboring field poly shapes. To create a model, we create a design of experiments (DOE) for all device categories and perform OPC followed by through-process window litho simulation. To limit the runtime of OPC and litho simulation for the DOE, we reduce the layout parameter space with a rigorously qualified methodology for filtering out unimportant parameters. To allow prediction of the device contour, we model the device edge placement error (EPE) using a response surface methodology followed by polynomial regression. We have implemented our predictive linewidth modeling with foundry 90*nm* and 65*nm* technology, along with industry-strength OPC models and recipes. Using the regression models, we have performed prediction on standard-cell blocks and achieved a 3σ prediction accuracy of 2*nm* across the process window.

1. INTRODUCTION

To evaluate linewidth variation of design geometries prior to manufacturing and to calibrate exposure, resist and etch processes, *lithography simulation* is used extensively by lithographers and process engineers. Lithography simulation (litho sim) is a computational procedure that evaluates silicon dimensions of layout geometries using a model of wafer exposure and processing steps. In sub-100*nm* technologies, accurate design-level performance and power analysis must consider litho-simulated design geometries to account for the impact of non-uniformities in the pattern transfer process [8]. Simulation of exposure, resist and etch processing steps in lithography at the design level is computationally expensive. The objective of this work is to construct a predictive model of post-OPC device linewidth without actually performing OPC and litho sim.

This paper is organized as follows. In Section 1.1, we present the background of our work and motivate the need for predictive modeling of device linewidth. In Section 1.2 we introduce our proposed approach. In Section 2, we discuss abstraction of layout shapes using parameters. We give formal definitions of parameters and discuss techniques for reducing the dimensionality of the parameter space. In Section 3, we give an overview of our design of experiments (DOE) and process modeling, and present our proposed methodology in detail. In Section 4, we discuss our experimental setup and give details of our flow for constructing the predictive model. We summarize the contributions of this work and present future directions in Section 5.

1.1. Motivation

OPC is typically performed using a litho model generated at the best defocus condition. Any deviation of focus or dose from the OPC conditions results in linewidth variation. Although the extent of variation is tolerable within the process window, the linewidth deviation can translate to performance and power variations at the design level. The use of defocus models (e.g., by Sturtevant et al. [2]) instead of the best focus model improves the linewidth response after OPC. However, post-OPC linewidths still vary with focus since the OPC is valid only at a *single* focus condition. Although the use of defocus and variational OPC models improve linewidth control, they do not guarantee a flat linewidth response within the process window.

Design Impact of Post-OPC Linewidth Variation. Linewidth variation has a direct impact on timing and leakage of designs. Timing analysis based on circuit delay models constructed from post-lithography critical dimensions enable designers to perform robust optimizations that are tolerant to variation [8]. Analysis of post-OPC residual CD error across the process window at the design-level is necessary to enable such flows.

Full-chip Lithography Simulation. Litho simulation across the process window at the design level is computationally expensive (even if the post-OPC layout is available). For standard cell-based layouts, full-chip post-litho linewidth evaluation can be sped up by running litho simulation on individual standard cells and then accounting for the variation in linewidth due to the presence of other cells in a layout placement context. This technique, referred to as library-based litho simulation, has been reported in [3]. However, library-based litho sim suffers from two basic drawbacks. (1) *Scaling with proximity effects.* Library-based litho sim and post-litho analyses perform OPC on individual standard cells followed by litho sim across the process window. Design-level litho sim output is then generated by substituting individual cell results into the full-chip layout. The full-chip litho contours obtained by this approach are invalid because OPC and litho sim do not comprehend inter-cell interactions. (2) *Incremental litho sim.* Conventional litho sim does not allow designers to evaluate litho contours after any engineering change order (ECO). Any layout ECO must be followed by full-chip OPC and litho sim across the process window to evaluate poly litho contours. This process is computationally prohibitive even if such an incremental litho sim flow is feasible.

To overcome these drawbacks and to enable fast, design-level *device* litho contour evaluation, we propose a predictive model of device litho contours. We next give an overview of our proposed methodology.

1.2. Proposed Methodology

To construct a predictive model of device litho contours in a layout, we model device contours of devices in poly test patterns as a function of geometric parameters (also referred to as "parameters") of each pattern across the process window. The geometric parameters of test patterns include poly width, spacing, line end extension, etc. We give formal definitions of layout (test pattern) parameters in Section 2.

To perform predictive modeling of litho contours, we first identify parameters of layout patterns that contribute to CD variation across the process window. The parameters that characterize device and poly shapes can be selected directly from design rules or from existing poly layouts in standard cells. We create a design of experiments (DOE) for different combinations of parameters within the optical proximity radius (OPR) surrounding the device; the values assumed by layout parameters in the DOE are bounded by design rule constraints. We discuss issues related to DOE parameter selection, parameter domain selection and their implications on model accuracy in Section 3.1. After selecting DOE parameter values, we perform OPC on the test pattern mask at the nominal defocus and exposure conditions. We then perform litho sim across all defocus and exposure doses. For each DOE configuration in the layout, we extract device litho contours along the direction of the device width, for modeling. To extract the contour of a device edge, we sample its litho print image uniformly along its width. The accuracy of contour reconstruction (i.e., "prediction") depends on the number of samples used for model generation. We construct a predictive model of device litho contours using contours of devices in test patterns. The predictive model of litho contour can be used in conjunction with layout analysis to obtain device edge placement error (EPE) values without running OPC and litho sim.

2. CAPTURING THE LAYOUT PARAMETER SPACE

In this section, we discuss the prediction and modeling phases of our methodology. For clarity, we give definitions of commonly used terms in Table 1. Figure 1 shows the overall flow of the proposed methodology. One of the most important steps of the flow is identification of layout parameters that affect device contours across the process window. This step is analogous to abstraction of layout geometries that affect the contour during litho sim. We formally define parameters of devices and their neighborhoods in Section 2.1. To identify and analyze the interactions between layout features, we propose to construct a DOE for all identified layout parameters.

The number of layout parameters in the neighborhood of a device can be in the range $10-20$. It is computationally infeasible to create and analyze a DOE in such high-dimensional space. To reduce the dimensionality of the parameter space and enable an exhaustive DOE and response surface modeling (RSM), we analyze the impact of individual parameters. We filter out parameters that contribute to less than $1nm$ variation in EPE across the process window. The methodology for filtering layout parameters to reduce the parameter space is discussed in Section 2.2. The reduced set of layout parameters is then used for exhaustive DOE generation, as discussed in Section 3. The filtering step also directs the mapping of a device layout (represented by the device and its neighborhood parameters) to its low-dimensional equivalent. This is an important step and is required to construct the device contour using the predictive model.

Table 1: Definitions of terms.

Notation	Description
Poly	Poly refers to the polysilicon geometry in a standard cell or a full-chip layout.
Layout polygon	Polygon representation of layout geometry.
Device	The region of the layout formed by intersection of poly and diffusion (active region). This is also referred to as gate poly.
Device edge	An edge of the polygon represented by the device. In this work, device edge refers to the (left or right) edge along the (vertical) device width.
Device parent poly	The poly feature of which the device under study is a part.
Layout parameter	A variable that captures the physical span of layout polygons or the separation between edges of layout polygons (these polygons can belong to the same layer or to different layers).
Device neighborhood	The region of the layout surrounding the device within a distance equal to the OPR in all directions. In L_∞ norm, this region is defined by a square that encloses the device. The side of the square is $2 \times OPR$.
Isolated device	If the device under study has no neighbors within its OPR, then it is isolated.
Dense device	If the device under study has at least one neighbor within the OPR of its edges, then it is dense.

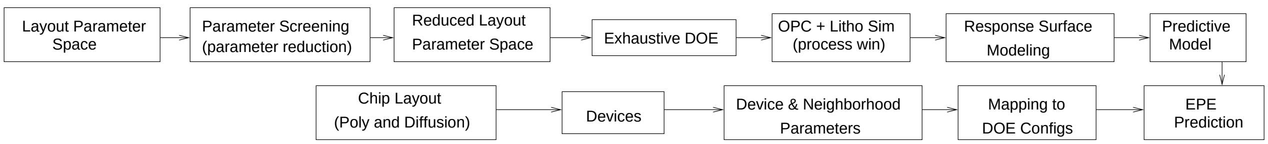


Figure 1: Overall methodology for predictive litho modeling.

2.1. Layout Parameters

To capture the variation in device contour across the process window as a function of layout parameters, we abstract the geometry of the device and its neighborhood in terms of a set of layout parameters. To identify layout parameters of the device parent poly and those of its neighbors, we formally define poly geometry. Any basic device in Manhattan geometry is characterized by the device body (i.e., region of intersection of poly and diffusion regions) and terminations. Poly terminations at device ends are a part of "field" poly and do not form devices. In the case of devices with vertical orientation, the terminations are present on the top and bottom of the device and in the case of horizontal orientation, terminations are present on the left and right of the device. In any given layout, devices are present either in vertical (V) or horizontal (H) orientation only (orientation of devices is constrained due to a systematic H-V bias in lithography [4]).

In a Manhattan layout, the terminations are determined by the direction of edges corresponding to the field poly beyond the edges of gate poly. To define device terminations and to classify devices into different categories, we use the following rules.
(1) Any given poly geometry in a layout can be defined as a sequence (or array) of points in the *x*-*y* plane.
(2) The sequence of points in the *point array* may follow a clockwise or counterclockwise ordering.
(3) Any two consecutive points in the point array define an *edge*.
(4) Any polygon edge (i.e., the vector connecting any two points in the point array of the polygon) can take one of four possible directions: right (0°), left (180°), top (90°) or bottom (270°).

Figure 2 shows a schematic of gate poly edges connected through a sequence of points in counterclockwise order. P_1, P_2, P_3, P_4 form the four points that define left and right edges of the device. Points D_1, D_2, D_3, and D_4 are points of intersection of gate poly edges with diffusion. $\overrightarrow{D_1D_2}$ defines the right edge of gate poly and is coincident with poly edge $\overrightarrow{P_1P_2}$ (includes field and gate poly). $\overrightarrow{D_3D_4}$ defines the left edge of gate poly and is coincident with the poly edge $\overrightarrow{P_3P_4}$. The direction of arrows from or to each of the points P_1, P_2, P_3, and P_4 indicates the direction of the poly edge incident to, or emanating from that point; these define the geometry of the parent poly of a device. Depending on the direction of vectors $\overrightarrow{BP_1\,P_1}$, $\overrightarrow{P_2\,AP_2}$, $\overrightarrow{BP_3\,P_3}$ and $\overrightarrow{P_4\,AP_4}$, and the relative locations of points P_1, P_4, P_2 and P_3, the geometry of the poly around the device is determined. Based on the classification of poly geometry towards device terminations, we categorize any given device in the layout into one of several configurations.

For a given device layout, three cases of relative locations of P_2 and P_3 are possible. Note that according to the convention of Figure 2, P_2 is always to the right of P_3, i.e., $P_2.x > P_3.x$, and P_1 is always to the right of P_4, i.e., $P_1.x > P_4.x$ (given any point P in a layout, $P.x$ denotes its x-coordinate and $P.y$ denotes its y-coordinate). The total number of valid device configurations possible at the top termination of a device is 6. Since the top and bottom terminations of a device can vary independently of each other, the total number of device configurations (based on edge classification beyond edges of gate poly) is 36.

2.1.1. Device Classification

The total number of (top or bottom) device terminations identified in Section 2.1 are generalizations of three simplified termination types: *line end, line corner* and *line taper*. These types are defined in the following.

(1) **Line end.** A device termination is a *line end* if the two points represented by ends of the gate poly edge (towards top or bottom) occur next to each other in the point array represented by the parent poly of the device. A device has a top line end extension if $AP_2 = BP_3$ and has a bottom line end extension if $AP_4 = BP_1$. The layout of a line end termination is shown in Figure 3.

(2) **Line corner.** A device termination is a *line corner* if the vectors emanating from or incident to the two points represented by ends of gate poly edge (towards top or bottom) are parallel to each other in opposite directions. Note that depending on the direction of the vectors, a termination can be a *left* line corner or a *right* line corner (see Figure 4).

(3) **Line taper.** A device termination is a line taper if the vectors emanating from or incident to the two points represented by ends of gate poly edge (towards top or bottom) are parallel to each other in the same direction. The layout of a top taper as defined above is shown in Figure 5. Note that the edges $\overrightarrow{BP_3\,P_3}$ and $\overrightarrow{P2\,AP_2}$ connected to the left and right gate poly edges are at equal spacing from the boundary between diffusion and gate poly. However, these edges are not constrained to be at equal distances from the diffusion boundary, and they can move independently of each other. Depending on the separation between horizontal diffusion edge and edges $\overrightarrow{BP_3\,P_3}$ and $\overrightarrow{P2\,AP_2}$, the taper configuration shown in Figure 5 can have two variants. These variants, called *left-proximal taper* and *right-proximal taper*, are shown in Figure 6(a) and Figure 6(b) respectively. In the left-proximal taper, the left edge beyond the gate poly edge is closer to the diffusion and gate poly boundary; in the right-proximal taper, the right edge is closer to the diffusion and gate poly boundary. A taper with constant left and right edge distance is referred to as a *uniform taper*. We denote line end, line corner and line taper as E^{end}, $C^{end}_{direction}$ and $T^{end}_{taper\_type}$, respectively, where $end = t$ (top) or b (bottom), $direction = l$ (left) or r (right) and $taper\_type = l$ (left-proximal) or r (right-proximal) or u (uniform). Using this notation, any of the 36 device types in the layout can be described by composing top and bottom termination types, in that order. For instance, the device shown in Figure 6(a) is denoted as $T^t_l E^b$.

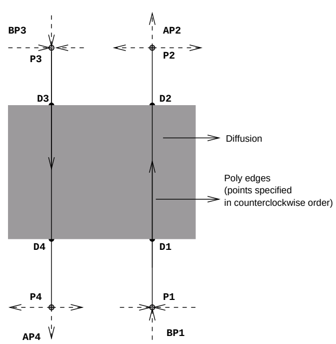


Figure 2. Points and edges of the poly geometry corresponding to a device.

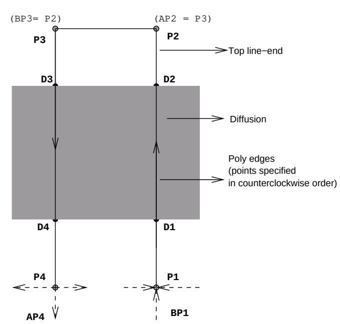


Figure 3. Line end at device top termination.

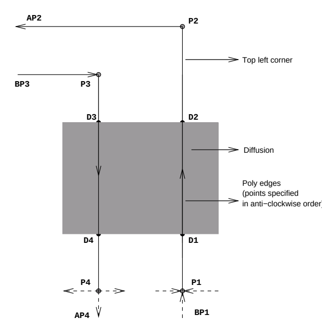


Figure 4. Left corner at device top termination.

2.1.2. Parameter Definitions

In the following, we define parameters of different types of devices. The number of parameters of an isolated device depends on the type of the device (i.e., its terminations). For a line end termination, the geometry is defined by *line end extension* or *end cap* (EC). For a corner termination, the geometry is defined by four parameters – two parameters each for the edges corresponding to each side of gate poly. Figure 7 shows the layout of a top right corner termination and its associated layout parameters. The length of the edge beyond the gate poly edge determines the extent of the corner, and the distance from the diffusion and gate poly boundary to the edge beyond gate poly determines the spacing to the corner.

Layout parameters of taper are similar to those of line corner. For a taper, the geometry is defined by four parameters – two parameters each for the edges corresponding to each side of gate poly. Figure 8 shows the layout of a top left-proximal taper termination and its associated layout parameters. The width of the left edge beyond the gate poly edge determines the extent of the left taper, and the distance from the diffusion and gate poly boundary to the edge beyond gate

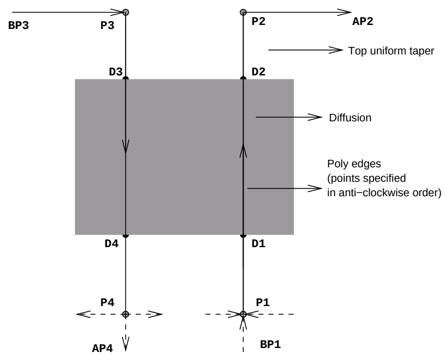


Figure 5: Uniform taper at device top termination.

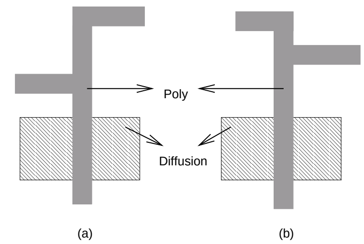


Figure 6. (a) Left-proximal and (b) right-proximal non-uniform taper at device top termination.

poly determines the spacing to the left taper. Table 2 gives the notations of layout parameters for basic device types. These parameters, combined with the device width (W), completely define an isolated device in the layout. Thus, the minimum number of parameters that define a device geometry is 3 (in the case of line end terminations at both ends of a device) and the maximum number is 9 (in the case of line corner or line taper at both ends of a device).

Table 2. Layout parameter notations ($end = t(op)$ or $b(ottom)$). Definitions of left corners and tapers extend toward right corners and tapers.

Termination type	Parameter	Notation	Computation
Line end	line end extension	EC^{end}	$EC^t = \lvert\overrightarrow{D_2\,P_2}\rvert$ $EC^b = \lvert\overrightarrow{BP_1\,P_1}\rvert$
Line corner	left corner spacing left corner extent	LCS^{end} LCE^{end}	$LCS^t = \lvert\overrightarrow{P_3\,D_2}\rvert$ $LCE^t = \lvert\overrightarrow{BP_3\,P_3}\rvert$
Line taper	left taper spacing left taper width	LTS^{end}; LTW^{end}	$LTS^t = \lvert\overrightarrow{P_3\,D_2}\rvert$ $LTW^t = \lvert\overrightarrow{BP_3\,P_3}\rvert$

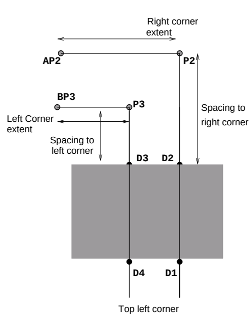


Figure 7. Corner termination parameters.

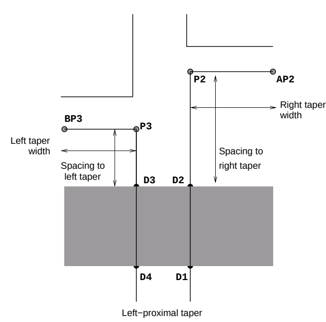


Figure 8. Taper termination parameters.

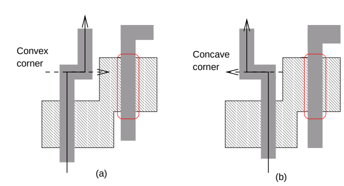


Figure 9. Layout of convex and concave corners in device neighborhood.

The set of parameters that describe a device in a layout environment depends on the device type and the poly layout within the OPR surrounding the device. Thus, the number of layout parameters depends on the minimum spacing between poly and the proximity range. To define layout parameters of a device and its neighborhood, we label poly shapes to the left of the device with prefix "L_{i}_" and those to the right with prefix "R_{i}_", where $i \geq 1$ and increases moving outward from the device under study. The layout of poly in the neighborhood of a device may not fall in to the device categories identified in Section 2.1.1. However, only the layout of neighboring poly that horizontally overlaps the device affects the post-OPC device contour. We refer to these regions as *edge interaction regions* (refer to Section 2.2).

Poly lines in a device neighborhood within the edge interaction regions can be one-dimensional (1D) (i.e., vertical or horizontal) or two-dimensional (2D) (i.e., poly with both vertical and horizontal shapes). 2D poly features refer to jogs, corners and contact landing pads. The incidence of 2D neighboring poly shapes on a device edge affects its contour and is well-known for creating litho hotspots. Poly "corner incidence" on a device edge refers to the projection of a poly bend onto the device edge. Figures 9(a) and (b) show the two possible projections - convex and concave - of a poly corner on to the edge of another device. A corner of poly that projects towards the device edge is called a *convex corner*, and one which projects away from the device edge is called a *concave corner*. This definition applies to counterclockwise ordering of the poly point array. We now discuss different types of poly shapes in a device neighborhood and define their layout parameters. To denote the layout of neighboring poly, we follow a simple convention. Vertical lines, i.e., 1D features, are denoted using a single letter 'V' with a $L_i\_$ or $R_i\_$ prefix. 2D features, that are a combination of vertical and horizontal lines are denoted using a sequence of 'H' and 'V' with a $L_i\_$ or $R_i\_$ prefix. Vertical and horizontal poly and the symbols 'H' and 'V' are annotated according to their projection direction.

Vertical (1D) Poly. A simple 1D vertical poly in the interaction region of an edge is shown in Figure 10. The vertical poly line can span, completely or partially, the entire width of the overlap region corresponding to a device. Poly lines 'a' and 'c' in Figure 10 show vertically-incident lines from the bottom and from the top, respectively, that partially span the interaction region. Poly line 'b' shows a vertical poly spanning the interaction region completely. Vertical poly lines can

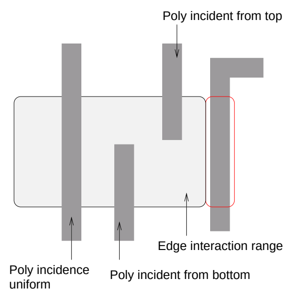


Figure 10. One-dimensional poly line layouts in the device interaction regions.

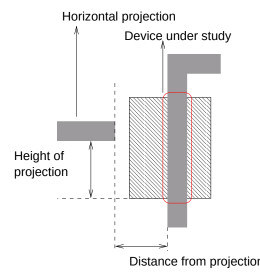


Figure 11. Horizontal projection of neighbor poly on the device under study.

project from top (t) or bottom (b), or can be incident uniformly (u) to the edge interaction region. We represent a vertical poly line with V^{end} where $end \in \{t, b, u\}$. Finally, the geometry of vertical poly can be represented by two parameters in the case of partial projection and by one parameter in the case of complete (uniform) projection. These parameters are as follows.

(1) **Spacing** of the (right or left) edge of the poly to the (left or right) edge of the device, respectively. The spacing parameter is common for both partial and uniform projections. The spacing is represented by S^{L_i} or S^{R_i}, where $i \geq 1$ is the index of the neighbor poly.

(2) **Extension** of the poly projection beyond the bottom (or top) edge of the interaction region (for bottom and top poly projections, respectively). The extension value for top (t) and bottom (b) poly projections is represented by $E^{L_i}_{end}$ or $E^{R_i}_{end}$, where $end = t$ or b and $i \geq 1$ is the index of the neighbor poly.

2D Poly. A 2D poly configuration has both horizontal and vertical segments in the edge interaction region and the corner defined by them can be convex or concave. To represent a 2D geometry, we decompose the polygon in to horizontal and vertical segments. The number of parameters of 2D poly configuration is the sum of number of parameters corresponding to vertical and horizontal segments. Due to space constraints, we do not discuss 2D poly configurations in detail here.

The number of layout parameters that are representative of the layout surrounding a device depend on the layout and the OPR. The maximum number of poly shapes within the OPR of a device edge depends on the poly-to-poly spacing specified by the design rules. If the number of poly to the left and right edge of a device is n, then the maximum number of layout parameters possible within the OPR of the device is $5 \times 2 \times n + 9$. The factor of 5 corresponds to the maximum number of parameters of a 2D poly in the neighborhood of a device edge, and the factor of 2 corresponds to device edges (left and right). The constant term in the expression corresponds to the maximum number of parameters of the device itself. It is clear that even with $n = 1$ (i.e., one left poly and one right poly), the number of parameters is greater than 20. To screen parameters from such a high-dimensional space, a modest three-level full-factorial DOE needs 3^{20} device configurations, which is clearly intractable. To reduce the dimensionality of the parameter space and to allow compact model construction, we prune the parameter space by filtering out unimportant parameters.

2.2. Pruning Layout Parameter Space

The construction of DOE in high-dimensional layout parameter space is infeasible due to OPC and litho simulation runtimes. To reduce the number of DOE parameters, we analyze the impact of neighbor poly parameters on device contours across the process window and filter out parameters that do not cause EPE magnitude change greater than $1nm$ in the aerial image*. Since OPC and litho simulation are iterative computational approaches, it is not possible to perform formal analyses of the impact of different layout parameters on device EPE. To determine the impact of parameters of neighbors on device EPE, we observe experimental data from OPC and process window litho sim. In the rest of this section, we discuss observations from EPE analysis. To prevent inferences from experimental artifacts, we analyze trends across multiple technologies, for different OPC and litho sim settings.

Observation #1. Poly geometries outside the device edge interaction region do not affect device contour.

For any layout, the aerial image is comprised of regions of varying light intensities. Regions of the image corresponding to opaque regions on the mask have higher contrast compared to those of clear regions. The change in image contrast of a layout feature depends on the presence of other features within the proximity range, and also on the direction of change in contrast corresponding to all features. For any given layout shape, the direction of change in image contrast is along the normal to edges of the shape. Hence, feature edges whose normals intersect edges of other features have optical interactions (only if they are within the OPR). This concept is illustrated in Figure 12.

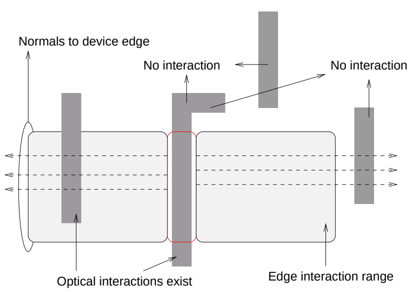


Figure 12. . Interactions between edges of poly features. Optical interactions are predominant only between edges whose normals intersect each other within the optical radius.

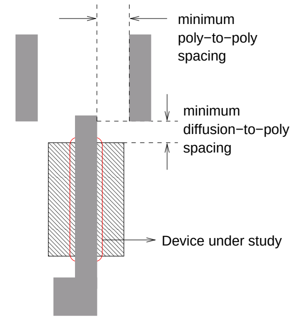


Figure 13. Test pattern used to evaluate the impact of poly outside the optical radius on device EPE across the process window.

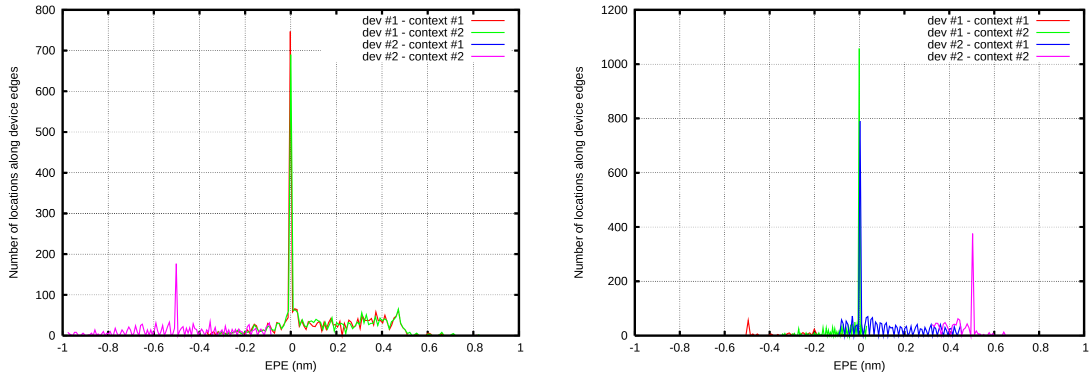
To validate this observation, we analyze device EPE with different poly contexts *outside* the edge interaction region. The poly and device configurations used for this experiment are shown in Figure 13. Poly features representing the Figure 14(a) and Figure 14(b) show the post-OPC EPE distributions of two devices across the process window, for two different neighbor poly contexts outside the interaction region, in $90nm$ and $65nm$ technology respectively. We sample EPE at 40 locations along each device edge to obtain EPE distributions. From the figures, we can observe that the mean change in EPE is $0nm$ for both devices in $90nm$ and $65nm$. The spread in EPE is in the range $(-1,\ 0.8)nm$ and $(-0.6,\ 0.6)nm$ for $90nm$ and $65nm$ respectively.

Observation #2. Only convex-incident corners of the first neighbor poly affect the device contour.

Convex corners next to a device edge within the poly interaction region ($L_1\_H^{cx}\_V^t$, $L_1\_H^{cx}\_V^b$, $R_1\_H^{cx}\_V^t$ and $R_1\_H^{cx}\_V^b$) project two bends onto the edge. However, a concave corner projects only a single bend. As a result, the impact of a convex corner on image contrast is greater than that of a concave corner. Since a concave corner projects its edges "away" from a device edge, it is equivalent to a poly with a line end. For this observation, we construct convex and concave corners adjacent to a device edge and compare the resulting EPE across process window with that of a line end.

Figure 15(a) and Figure 15(b) show comparisons of post-OPC EPE distributions of (1) $EPE_{lineend} - EPE_{convex}$ and (2) $EPE_{lineend} - EPE_{concave}$ for a single device across the process window. The terms $EPE_{lineend}$, EPE_{convex} and $EPE_{concave}$ denote the EPE at multiple locations along device edges when the device neighbor is a line end, convex corner and concave corner, respectively. From the figures we can observe that for both $90nm$ and $65nm$ technology, $EPE_{lineend} - EPE_{concave}$ has a tighter distribution than $EPE_{lineend} - EPE_{convex}$. The number of sample points at which $EPE = 0nm$ is greater for the case of concave corner compared to that of convex corner. This suggests that concave corners are equivalent to line

*Sub-nanometer EPE variations are typically neglected even in lithography simulation [5].

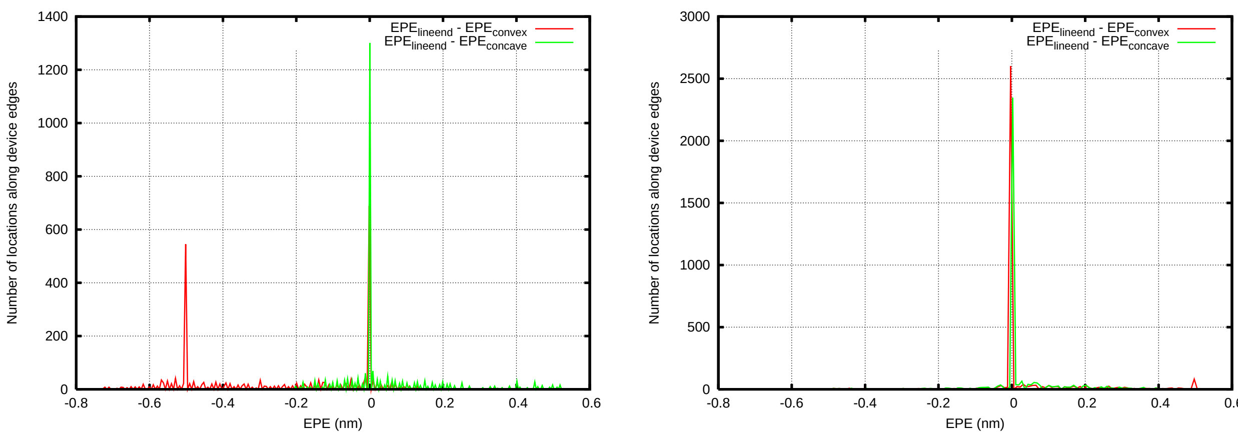


(a) EPE distributions for the 90nm technology.

(b) EPE distributions for the 65nm technology.

Figure 14. EPE distributions of two devices (dev #1 and dev #2) in two different layout contexts of poly outside the edge interaction region. The distributions are generated from litho sims across the process window in 90nm and 65nm technologies.

end in terms of EPE impact. As the distance of the corner from the device edge increases, even convex corners can be approximated as line ends.



(a) Difference distributions for the 90nm technology.

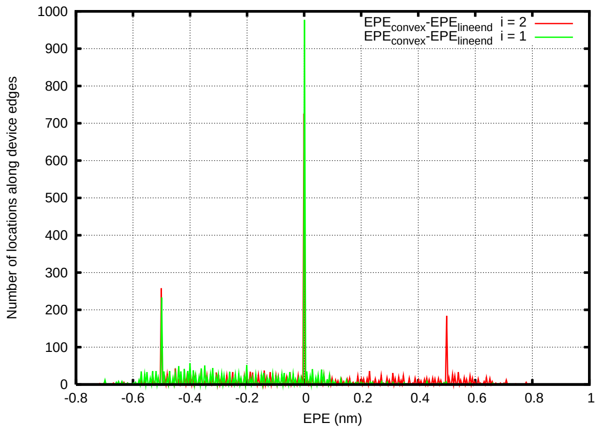
(b) Difference distributions for the 65nm technology.

Figure 15. Distributions of the difference between EPE of a device when the neighbor is (1) a line end, and (2) a convex or a concave corner. Results are generated from litho sims across the process window.

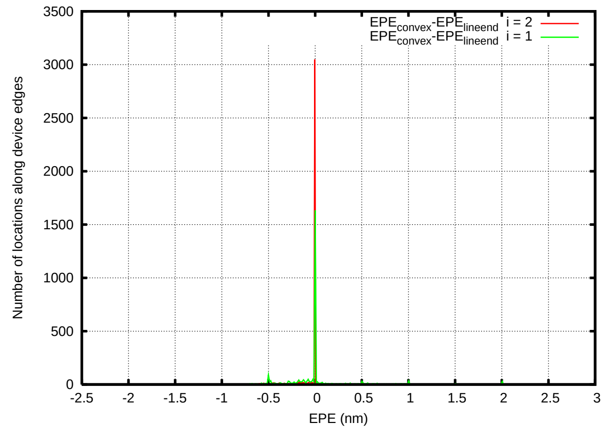
Observation #3. Convex and concave corners of poly beyond the first neighbor poly can be ignored.

Observation #3 extends Observation #2 for the case of poly beyond first neighbor. Poly with convex corners beyond the first neighbor ($L_1\_H^{cx}\_V^t$ and $L_1\_H^{cx}\_V^b$, where $i > 1$) are "shielded" by the first poly. As a result, the impact of a convex corner on EPE diminishes beyond the first poly, and it can be considered equivalent to a line end ($L_i\_H^{cx}\_V^t \equiv L\_V^t$). The same is the case with concave corners, which have a smaller impact on EPE compared to convex corners (from Observation #2). To demonstrate the decreasing influence of corners and line bends on poly EPE beyond the first neighbor, we compare the EPE of a device in two neighborhoods: (1) corner ($L_2\_H^{cx}\_V^b$) and (2) line end ($L_2\_V^b$), across the process window.

Figure 16(a) and Figure 16(b) show post-OPC EPE distributions of $EPE_{convex} - EPE_{lineend}$ for the cases of $i = 1$ and $i = 2$, for a single device, across the process window. The terms $EPE_{lineend}$ and EPE_{convex} respectively denote the EPE at multiple locations along device edges when the device neighbor is a line end and convex corner. From the figures we can observe that the distribution of $EPE_{convex} - EPE_{lineend}$ is skewed toward positive EPE when the poly with the corner is the first neighbor (i.e., $i = 1$). The distribution sharpens toward the center and is skewed toward negative EPE when the poly with the corner is the second neighbor. This demonstrates that influence of corners beyond the first poly diminishes and that the poly can be considered equivalent to a line end.



(a) Difference distributions for the 90*nm* technology.



(b) Difference distributions for the 65*nm* technology.

Figure 16. Distributions of the difference between EPE of a device when the neighbor is (1) a line end, and (2) a convex corner. Results are generated from litho sims across the process window.

Observation #4. Beyond the first neighbor, poly in the edge interaction region affect EPE only if the normal to the device edge at that location intersects the neighbor.

To study the EPE impact of change in vertical separation of the second neighbor, we vary the vertical poly spacing relative to the bottom edge of the device under study. We simulated the change in EPE at the lower left corner of a device at the worst defocus condition for the 90*nm* and 65*nm* technologies. We observed that when the second left neighbor "moves out" of the interaction region (i.e., when the normal from the bottom left of the device does not intersect the vertically-shifted poly), there is a sudden drop in the EPE and it remains constant for other values of vertical shift.

To reduce the dimensionality of the parameter space, we use Observations #1, #2, #3 and #4 to filter out poly parameters that do not cause EPE variation $> 1nm$ across the process window. From Observation #1, we can infer that poly geometries outside the edge interaction region can be neglected in modeling EPE of devices. From Observations #2 and #3, we can infer that only convex-incident poly in the edge interaction region affects device contour shape. Following these observations, we can reduce the number of parameters of poly beyond the first neighbor from 3 (in the case of poly with convex/concave corner) to 2 (in the case of poly with line end). From Observation #4, we can infer that beyond the first neighbor, poly vertical separation relative to the device does not have any affect on EPE. Based on all the four observations, we can reduce the number of parameters of the neighbor poly in the edge interaction region.

3. DESIGN OF EXPERIMENTS AND PROCESS MODELING

In this section, we discuss design of experiments and predictive model construction (process modeling) for edge placement error (EPE) of layout devices. In Section 3.1, we present our proposed DOE methodology. In Section 3.2, we present our predictive modeling approach.

3.1. DOE Methodology

The classical design and analysis of DOE focus on optimal design of 2 or 3 level experiments and analysis of variance of experimental data for screening and calibration experiments. These DOE frameworks cannot be extended toward collection and analysis of experimental data with several factors, each with arbitrary number of levels. In this section, we discuss our proposed methodology for collection of EPE data for all device types.

To construct a predictive model of EPE across the process window at the design-level, we require models of EPE for all device types in the layout. The number and type of parameters are different for each device type. To collect EPE data for modeling, we generate DOE for each of the 36 device types in isolated and dense layout contexts. The number of layout parameters for each isolated device configuration may vary from 3 to 9. The choice of layout parameter values (i.e., sampling of layout parameter space) can be determined from design rules or from existing standard cell libraries for which the EPE model is generated. In the rest of this section, we discuss a layout analysis methodology to extract parameter distributions and propose a sampling scheme for DOE construction.

3.1.1. Extraction and Sampling of Layout Parameter Distributions

To obtain layout parameter distributions, we extract all poly parameters corresponding to all devices, either from the entire standard cell library or a design layout in a given technology. For each parameter type, we count the number of devices with a specific value of that parameter. Layout parameter distributions are discrete and are characterized by peaks. The sampling strategy for choosing layout parameter values for the DOE must consider model accuracy and DOE size. If the distribution is uniformly and sparsely sampled, then it may not capture the "peaks" in the non-periodic distribution of layout parameters. On the other hand, an uniform dense sampling that includes all the peaks leads to a large DOE size. To maintain a balance between accuracy and DOE size, we apply the following general guidelines for sampling parameter distributions.
(1) Any sampling of the parameter distribution must include the peaks. The peaks in the parameter distribution represent a significant number of devices having a value corresponding to that peak in the layout. If the value corresponding to the peak is included in the sampling, then the modeling error corresponding to that data point can be minimized.
(2) Include samples from the regions of the distribution which contribute to most of the variation in EPE. Although layout parameters assume a wide range of values in the layout, only a specific set of values contribute to most of the variation in EPE. The sampling scheme must consider more samples in the regions of high variability.
(3) Utilize the knowledge about any trend in the response with respect to a given parameter while sampling its distribution. If the trend in the response (i.e., EPE) with respect to a variable is known *a priori*, then it must be used to guide the sampling scheme.

We construct a full factorial DOE for each of the 36 device configurations, by varying each of the layout parameters in the configuration through all the levels obtained from sampling its corresponding distribution. We discuss details of test pattern layout, OPC, lithography simulation and EPE data collection in Section 4.

3.2. Predictive Modeling of EPE

In this section, we discuss model section, model fitting and validation in detail.

Model selection. Process window typically corresponds to the depth of focus and exposure latitude space that results in a CD variation of 10% of drawn CD. Within the process window, CD response to focus and exposure dose can be modeled using low-order polynomials [6]. Outside the process window, the behavior of post-litho CD across different levels of defocus and exposure dose can be discontinuous. To model EPE response within the process window, we use polynomial regression to fit a model of layout parameters, defocus and exposure dose. We choose to use polynomial regression as the layout and litho parameters exhibit behavior that can be approximated by quadratic or cubic polynomials.

Model fit. Model fitting is an iterative process that involves selecting variables and their interactions, fitting the model, and checking the quality of fit. To construct our EPE model, we explore the multidimensional response surface of each device EPE and obtain the main effects and interaction effects of parameters. To observe trends in higher dimensions, cross-sections of the response surface data can be used to obtain main effects. The data set can be *sliced* along each dimension, for a fixed setting of variables in all remaining dimensions, to obtain the trend of the response along that dimension. To generate our EPE model, we first identify main effects of model variables. We explore the response surface of the EPE data using online analytical tools such as *rstool* in MATLAB statistics toolbox [7]. The main effects of variables can be linear, quadratic or cubic. Due to the nature of the EPE response within the process window, layout and litho parameters do not exhibit higher-order trends. After accounting for main effects, we explore interactions between parameters by varying the level of each parameter and capturing the *change* in the trend in response to other variables. This analysis is repeated for all the model variables. After the determination of main and interaction effects, we specify a *model form* of the regressor and perform linear least-squares regression to obtain parameters of the model.

Model validation. To determine the quality of our linear model, we evaluate R^2 of the fit. We use fit descriptions such as residual plots, normal probability plots and quantile-quantile (Q-Q) plots to determine the fit quality and improve it. We also perform lack-of-fit test to check if the fit is missing any significant terms. To check for over fitting, we use Student's t-test to determine the relevance of each term in the model fit from linear regression. To test the validity of the model across all device EPE, we perform predictions at the design layout level across the process window and compare them against EPE values from lithography simulation. We analyze the distributions of EPE prediction error (i.e., difference between predicted EPE and actual EPE) and improve the model.

4. EXPERIMENTS: METHODOLOGY AND RESULTS

In this section, we discuss our experimental setup for model construction and results in detail. The flow discussed in this section is not specific to a technology node. In Section 4.2 we discuss the results of model construction and the predictive power of the EPE model in the 90*nm* and 65*nm* technology nodes.

4.1. Flow Setup

In this section, we discuss each step of the flow for EPE prediction in detail.

Layout parameter extraction. We extract layout parameters corresponding to each device configuration and obtain their distributions for sampling. To extract layout parameters of a device, we analyze the shape of its poly parent and measure distances to corners and other poly lines with in the optical vicinity of the device edge.

Layout parameter sampling and DOE Construction. To construct DOE for OPC and litho sim, we sample parameter distributions from the parameter extraction step. Sampling of distribution determines the maximum order of the polynomial corresponding to that parameter in the final EPE model. For instance, to discover any quadratic dependency between a layout parameter and the output, there must be at least three samples from its corresponding parameter distribution. We use the sampling guidelines discussed in Section 3.1.1 to obtain layout parameter values for DOE construction.

For the predictive modeling flow, we use 50 standard cells in the 90*nm* and 65*nm* technology. We sample the distributions of parameters across all device configurations and construct test pattern masks. We construct a separate mask for each device configuration to perform OPC and litho simulation. The values of layout parameters for each configuration are taken from the distributions obtained by parameter extraction on the standard cell library. Table 3 shows the device configuration and the number of corresponding test patterns for EPE data collection. We use *Calibre Workbench v2007.1_24.22* to create test pattern masks.

Table 3. Number of DOE patterns in the 90*nm* and 65*nm* test masks corresponding to different device configurations.

Config of device under study	No. of test patterns (90nm)	No. of test patterns (65nm)
$E^tC_l^b$	11664	17496
$E^tC_r^b$	13122	17496
$E^tT_u^b$	17496	23328
$C_l^tE^b$	10848	17496
$C_r^tE^b$	12222	17496
$T_u^tE^b$	19200	23329

Table 4: OPC model parameters.

OPC model parameter	90*nm*	65*nm*
NA	0.75	0.85
Illumination	Annular	Annular
σ_1, σ_2	0.75, 0.5	0.9, 0.6
Defocus range	$[-100, 100]nm$	$[-75, 75]nm$
Resist threshold (Exposure dose)	$0.24, 0.25, 0.26$	$0.28, 0.3, 0.32$

OPC and Litho Simulation. To obtain EPE data for modeling, we perform OPC at the nominal defocus and exposure condition, followed by lithography simulation across all defocus and exposure dose combinations. For our OPC and litho sim setup, we use industry-strength recipes that give 0*nm* EPE at the nominal focus and dose conditions. OPC parameters such as fragmentation length, corner correction distances and site choices are optimized to minimize EPE across the process window. For both 90*nm* and 65*nm* technologies, we use a threshold-based resist model for OPC and litho sim. Table 4 gives the NA, partial coherence factors and illumination settings used for generation of optical models. We use *Mentor Calibre v2007.1_24.22* for all OPC and litho sim runs. To obtain EPE data for test patterns, we run litho sim at 27 points across the process window in both 90*nm* and 65*nm* technologies. We vary exposure dose by changing the threshold of the resist. We extract device EPE from litho contours at five locations along the width of the device (spaced uniformly). We use shape analysis routines in Calibre design rule engine to obtain device EPE values.

Data Preparation and Polynomial Regression. To create data decks for regression, we combine layout parameter data from test mask generation step and EPE data from litho contour analysis. We use these data decks to run polynomial regression in R (version 2.1) [1]. Since EPE at different locations along the device edge exhibits different sensitivities to different layout parameters, we perform modeling at each location separately. In our current setup, we create 10 EPE models corresponding to five locations each on the left and right edges. We choose these locations at distances 0%, 25%, 50%, 75% and 100% of the width of the device. The number of EPE sampling locations can be increased for greater accuracy. To analyze the response surface for model construction, we use *rstool* in MATLAB statistical toolbox to analyze main and interaction effects between layout parameters. The online analysis feature in *rstool* allows users to interact with the data sets and observe changes in variable levels on the output response. We use observations from *rstool* to guide regression in R. We use the linear least squares regression package *lm* in R to fit EPE models. We fit the model by specifying the main and interaction effects of the model, and *not* the exact polynomial fit. We iteratively improve the model fit by adding or dropping variables and their interactions, while checking for its quality using residual, Q-Q plots and Student's t-test. We stop model improvement when the root mean squared (RMS) error is $\leq 1nm$. The final model is saved in internal R format for prediction.

EPE Prediction. To predict EPE, we first extract layout parameters corresponding to all devices in a design layout. We classify each device into one of the 36 types based on its terminations. We then construct extraction decks that pass device parameters, focus and exposure dose to the model corresponding to the device type. We compare the predicted EPE results against those obtained from litho sim at the design layout level to validate the models. In our prediction flow, we use the layouts of three ISCAS benchmark designs, synthesized using 50 cells with a placement utilization of 75% in the TSMC 90*nm* library. We export the standard-cell layout in GDSII stream format for OPC and litho sim. We also perform layout parameter extraction to obtain the parameters of all devices in the design layout for EPE prediction.

4.2. Predictive EPE Model: Results

In this subsection, we discuss the results of EPE modeling and validation. Table 5 gives the R^2 and RMSE of fit for $E^tC_l^b$, $E^tC_r^b$ and $E^tT_u^b$ at all EPE sampling locations in the and 65*nm* technology (90nm results are not included due to page limit constraints). From the table we can observe that the quality of fit improves significantly at sampling locations away from a corner. Corners and jogs in the poly that are proximal to the device edge are highly susceptible to variation due to focus and dose variation. The EPE at the sampling location next to a corner vertex is cubic in the distance of the sampling location to the corner vertex. Further, the extent of the corner (LCE or RCE) also affects the curvature of the contour in EPE sampling locations that are proximal to the corner. As a result, the spacing to corner and the extent of the corner have significant correlated impact on the device EPE near a corner. This effect is prominent along the edge that has a corner in the same direction as the edge i.e., left edge is affected more due to the presence of a left corner than due to a right corner and vice-versa. Away from the corner, defocus and exposure dose are the most predominant contributors to EPE variation.

Table 5. Statistics of fit for 65*nm* device configurations. Columns 3 through 12 correspond to the bottom (b), first quarter (fq), center (c), third quarter (tq) and top (t) EPEs of the left (l) and right (r) edges, respectively. The value of RMSE is given in nm.

Device Config	Fit Metric	b_l	fq_l	cl	tq_l	t_l	b_r	fq_r	c_r	tq_r	t_r
$E^tC_l^b$	R^2	0.90	0.90	0.90	0.92	0.93	0.89	0.90	0.87	0.91	0.89
	RMSE	0.70	0.45	0.45	0.40	0.41	0.55	0.46	0.51	0.42	0.54
$E^tC_r^b$	R^2	0.93	0.90	0.91	0.93	0.94	0.93	0.92	0.91	0.92	0.94
	RMSE	0.61	0.44	0.41	0.37	0.39	0.45	0.42	0.42	0.39	0.39
$E^tT_u^b$	R^2	0.84	0.88	0.91	0.92	0.94	0.85	0.88	0.91	0.92	0.94
	RMSE	0.88	0.52	0.43	0.39	0.40	0.85	0.51	0.43	0.39	0.39

Figure 17 shows the trend in EPE at the center of left edge of the $E^tC_r^b$ configuration as a function of spacing to two left neighbors and two right neighbors. From the figure we can observe that the EPE at the center of the left edge is linear in the spacing to the first left and first right neighbors. We can also observe that left neighbor spacing has a more significant impact than the right neighbor spacing. The spacing to neighbors beyond the first neighbor decreases progressively and the trend is weakly quadratic. This result is in line with Observation #3 discussed in Section 2.2. To demonstrate the effectiveness of the predictive model at the design level, we run prediction on three testcases: c432, c880 and c3540, with 710, 1152 and 3464 devices respectively. We run prediction using EPE models at 10 locations along each device edge, across 27 defocus and exposure dose conditions. We compare 270 predicted EPE values for each device against actual EPE from litho simulation. Figures 18 and 19 show the distribution of the EPE prediction error (difference between actual EPE and predicted EPE) and the scatter plot of actual versus predicted EPE for c432 testcase across the process window. From the distributions, we can observe that the mean prediction error is 0*nm* and a significant fraction of errors are within 1*nm*. Table 6 gives the mean error and standard deviation of prediction error distribution (across process window) for each testcase in 90*nm* and 65*nm* technology.

5. CONCLUSIONS

Design analysis and optimization in future technology nodes (45*nm* and below) must consider silicon shapes to decrease pessimism in design that is present in existing corner based methodologies. Computationally intensive processes such as OPC and lithography simulation cannot be performed at the design-level since design phase cannot be provided with

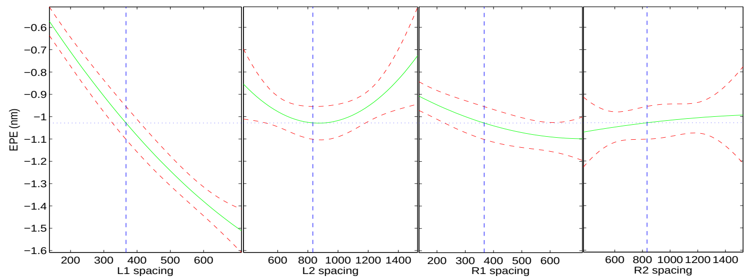


Figure 17: Trend in center EPE of left edge of the $E^tC_r^b$ configuration with left and right neighbor spacing (90*nm* technology).

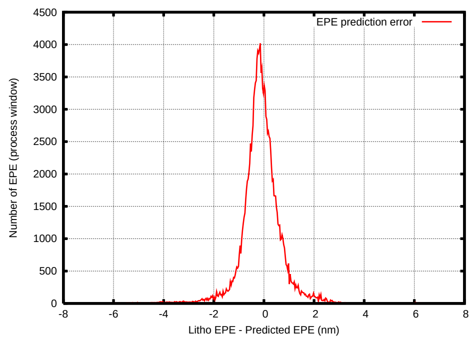


Figure 18. Distributions of error in EPE prediction from that of litho sim in the 90*nm* implementation for testcase c432.

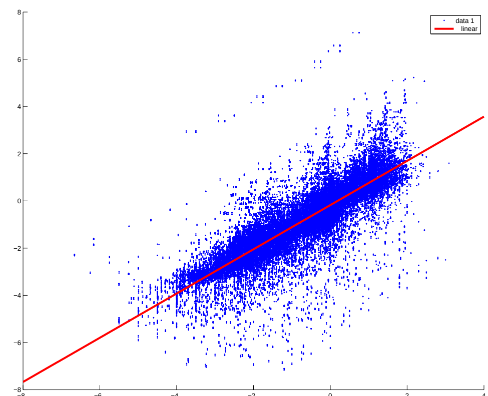


Figure 19. Scatter plot of actual EPE versus predicted EPE for c432 showing 145923 EPE points across the process window.

foundry models. Further, litho simulators cannot be used during *incremental* design analysis and optimization due to runtime considerations.

To provide design with *fast* and *accurate* models of post-lithography linewidth, we have proposed a novel methodology for modeling of device linewidths from litho sim. In this methodology, we construct test patterns representative of layout geometries and perform litho sim across the process window after OPC. We then capture the variation in device linewidth and perform regression in terms of layout parameters of poly, defocus and exposure dose. We have executed this methodology with leading-edge TSMC 90 and 65*nm* processes as a testbed, and have demonstrated the efficacy of our approach. The mean prediction error (difference between predicted EPE and actual EPE) across the process window is $<$ 0.2*nm* for both 90*nm* and 65*nm* technologies. The standard deviation of prediction error is in the range $0.8 - 1.2$*nm* for 90*nm* and 65*nm* technologies. This implies that our proposed methodology emulates the output of the litho sim tool within 2*nm* for 90% of EPE predictions. This accuracy is reasonable during incremental analysis of layout printability and resulting electrical impact during the design phase. Further, designers do not need to perform OPC and lithography simulation to analyze layout printability.

We note that the recipes used for OPC and lithography simulation by the foundry, prior to pattern transfer on the wafer, are considered "golden". A predictive model generated on the basis of these golden recipes can be used for analysis of any layout in the same technology. If the golden OPC and lithography simulation recipes are changed, then the models must be re-calibrated by performing lithography simulation on post-OPC test pattern layouts.

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Table 6: Statistics of EPE prediction error distributions for testcases in 90*nm* and 65*nm* technologies.

Testcases	Fit Metric	Value (90*nm*)	Value (65*nm*)
c432	μ (nm)	-0.11	0.04
	σ (nm)	0.80	1.17
c880	μ (nm)	-0.06	0.10
	σ (nm)	0.89	0.95
c3540	μ (nm)	-0.09	-0.12
	σ (nm)	0.88	1.05

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