Electrical Metrics for Lithographic Line-End Tapering

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ABSTRACT

A major source of patterning problems in low-k1 lithography is line-end pullback. Though geometric metrics such as CD at gate edge have served as good indicators, the ever-rising contribution of line-end extension to layout area necessitates reducing pessimism in qualifying line-end patterning. Electrically-aware metrics for line-ends can be helpful in this regard. In this work, we calculate the I_{on} and I_{off} impact of line-end taper shapes as well as line-end length. The proposed models are verified using TCAD simulation in a typical 65nm process. We observe that the device threshold voltage is a weak function of line-end pullback, and that the electrical impact of the taper can vary with overlay errors. We apply a non-uniform channel length model in addition to the proposed taper-dependent threshold voltage model to calculate ΔI_{on} and ΔI_{off}. Finally, the electrical metric for line-end printing is defined as *expected* change in I_{on} or I_{off} under a given overlay error distribution. We also propose a super-ellipse form to parameterize taper shapes, and then explore a large variety of taper shapes to characterize electrical impact.

1. INTRODUCTION

In the subwavelength lithography regime, gate shape is no longer a perfect rectangle given the low $k1$ patterning conditions ($k1 < 0.3$). Current circuit analysis tools assume that a transistor gate and diffusion are perfect rectangles. These tools are unable to handle complicated geometries. Large discrepancies can result between the simulated and observed values of circuit parameters such as current and threshold voltage. Moreover, the discrepancy is likely to become more significant as the misalignment becomes a more critical issue in future technologies.

There have been several approaches to electrically model non-rectilinear geometries [7–10, 12–14]. All of these works consider the threshold voltage and hence the current density to be uniform along the device width. As a result, variations along with gate length are treated the same, irrespective of the location of the variation. It is known that the fringing capacitance [4] due to line-end extension and dopant scattering significantly affect the device threshold voltage. These effects are more pronounced near the device edges and roll off sharply as we move toward the center of the device. Some previous work has accounted for this effect via non-rectangular gate models [5, 11]. Most of these works slice non-rectilinear gates along the device width at a certain level of granularity, then sum of I_{on} (or I_{off}) of each slice to model I_{on} (or I_{off}) of the non-rectilinear devices. For each rectangle, the current density model is used corresponding to its length. The total current of this rectangle is the integral of the current density over its width. The total current can be used to provide an equivalent rectangular length for the device, so that it can be modeled using SPICE-like tools. [6] has also investigated the impact of the non-rectilinear shape of diffusion on circuit performance using TCAD simulation. Source-side and drain-side rounding of diffusion behave differently from an electrical perspective, which suggests that diffusion rounding modeling must be design context-aware. Simple weighting function models for I_{on} and I_{off} are used to account for the diffusion rounding effects, by adjusting the gate width.

The primary concerns of lithographic patterning are line-end pullback and linewidth. Traditionally, lithographers have measured line-end printing quality by (1) line-end gap (space between two facing line-ends), (2) CD at the gate edge, and (3) non-existence of line-end shortening (i.e., poly not covering active completely). Though these geometric metrics have served as good indicators, the ever-rising contribution of line-end extension to layout area necessitates reducing pessimism in qualifying line-end patterning. The quality of line-end patterning depends on the rounded shape of the line-end, as well as on linewidth at device edge (and, to a negligible extent, on line-end gap). We use the word *"taper"* to describe the shape of a line-end. Line-end itself is defined as the extension of polysilicon shape beyond the active edge. We employ a 3D TCAD simulator [2] to investigate the changes of capacitance, I_{on} and I_{off} according to various tapers and line-end extensions. We observe that the current and leakage is a strong function of line-end pullback. For example, our experiments indicate that I_{on} can change by as much as 4.5% and I_{off} by as much as 30% as shown in Figure 1. Moreover, the electrical impact of the taper can vary significantly with overlay errors.

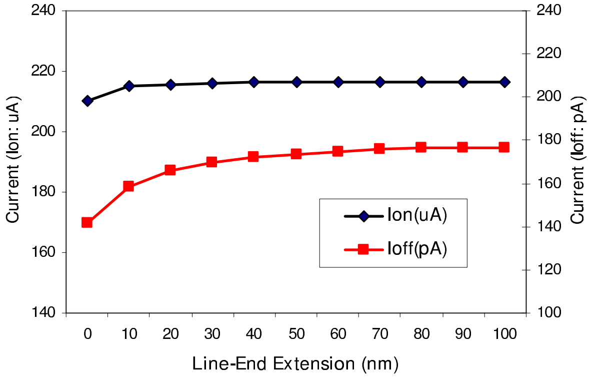


Figure 1: I_{on} and I_{off} change with varying line-end extension.

In this paper, we propose a novel modeling framework which includes (1) capacitance modeling of taper and consequent V_{th} change in channel, and (2) I_{on} and I_{off} modeling from the new capacitance model. Finally, the electrical metric for line-end printing is defined as *expected* change in I_{on} or I_{off} under a given overlay error distribution. We use a super-ellipse form to parameterize taper shapes and then generate a large variety of taper shapes. We evaluate the electrical metric on these line-end taper shapes to come up with simple rules of thumb that the lithographer can use to quickly evaluate the quality of a lithography + OPC solution with respect to line-end patterning.

2. TAPER MODELING

Taper affects the fringe capacitance to the channel of the MOS gate, which in turn affects the threshold voltage of the gate. Hence, I_{on} and I_{off} models accounting for taper impact can be developed in terms of taper capacitance. Figure 2 shows the overall flow of taper modeling.

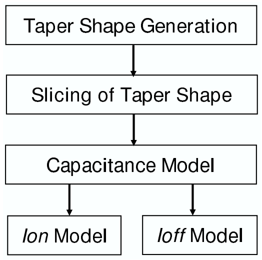


Figure 2: Taper modeling flow. I_{on} and I_{off} can be modeled as functions of taper capacitance.

2.1. Taper Shape Generation with Super-Ellipse

We propose a taper generation method using the $super-ellipse$ equation. A super-ellipse curve is defined as the set of all points (x,y) such that

$$\left|\frac{x}{a}\right|^n + \left|\frac{y-k}{b}\right|^n = 1, \qquad (1)$$

where $n > 0$ and a and b are semi-minor and semi-major axes of a super-ellipse, and k represents taper shift in the y-axis. For a given taper shape, a and b represent gate length and length of taper, respectively. n determines the slope, or corner routing, of the taper. For example, n = 2 yields an ordinary ellipse, and increasing n beyond 2 yields shapes that start to resemble a rectangle. The center of a super-ellipse o represents a misalignment value where (3σ) is considered to be the worst-case misalignment.

For asymmetric taper shapes, the super-ellipse is rotated about its center with $x = x'cos\theta - y'sin\theta$ and $y = x'sin\theta + y'cos\theta$ (or $x = x'cos\theta + y'sin\theta$ and $y = -x'sin\theta + y'cos\theta$), where x' and y' are the original coordinates of the original super-ellipse shape. $b+k$ represents the new LEE (line-end extension) after taper shift. In this paper, we focus on symmetric taper shapes only.

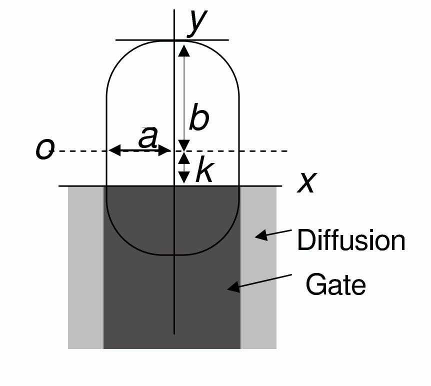


Figure 3: An example of Taper represented by super-ellipse equation.

3. NON-UNIFORM TAPER MODELING

An electrical model for the line-end taper must be representative of change in power or performance characteristics of a given device. For taper modeling, we convert a lithography contour into several sliced rectangles as shown in Figure 4. For each slice, we use the current density model corresponding to its length. The sum of the currents of all slices is the total current of the device. The total current can be used to provide an equivalent rectangular length for the device, so that it can be modeled by SPICE-like tools. The taper model, along with the non-uniform channel length model [5], is used to model the device under misalignment. We calculate the probability of occurrence of each slice at a given location from the misalignment distribution. Using location-dependent weights in taper and channel, we can predict the change in I_{on} or I_{off} under a given misalignment error.

3.1. Capacitance Modeling

Gate capacitance is a sum of capacitance of channel ($C_{channel}$) and capacitance of the line-end extension (C_{taper}). C_{taper} is a fringe capacitance between gate extension and the channel. Due to the large difference in electric field between the gate edge and the gate extension, we can simply model the capacitance of gate extension as a sum of fringe capacitance of each segment and the capacitance of the gate edge which is the fringe capacitance without line-end extension, illustrated in Figure 4.

$$C_{taper} = C_{edge} + \sum_{i=1}^{N} C_{taper_i} \tag{2}$$

where
$$C_{taper_i} = l_i^{\alpha}\left(\frac{t_i}{h_i + t_i/2 + t_{ox}}\right)^{\beta}, \; C_{edge} = \lambda \cdot \frac{l_0}{L_{nom}} \tag{3}$$

Capacitance of each taper slice or segment can be modeled as a function of the length (l_i), thickness (t_i), the distance from the gate edge (h_i) and oxide thickness (t_{ox}). Intuitively, this fringe capacitance effect increases with larger length, larger thickness and smaller height. C_{edge} is simply modeled in terms of the ratio of the linewidth of the gate edge (l_0) to the nominal gate length (L_{nom}).

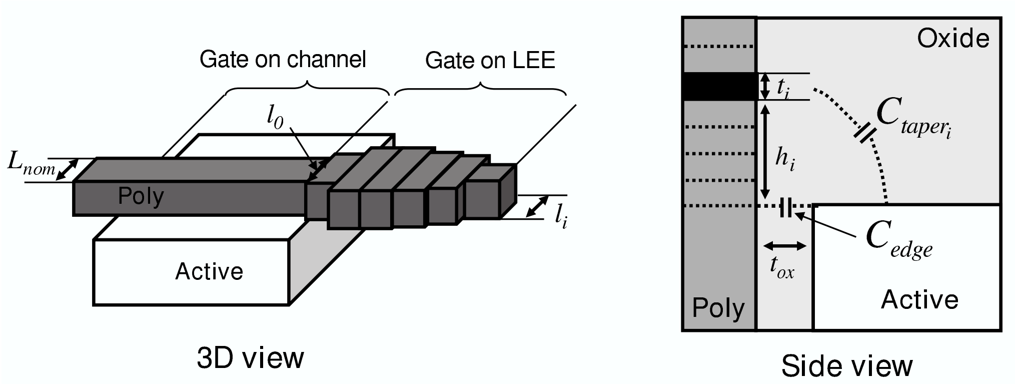

Gate on channel
Gate on LEE
l_0
L_{nom}
Poly
l_i
Active
3D view
Oxide
t_i
C_{taper_i}
h_i
C_{edge}
t_{ox}
Poly
Active
Side view

Figure 4: Modeling line-end capacitance.

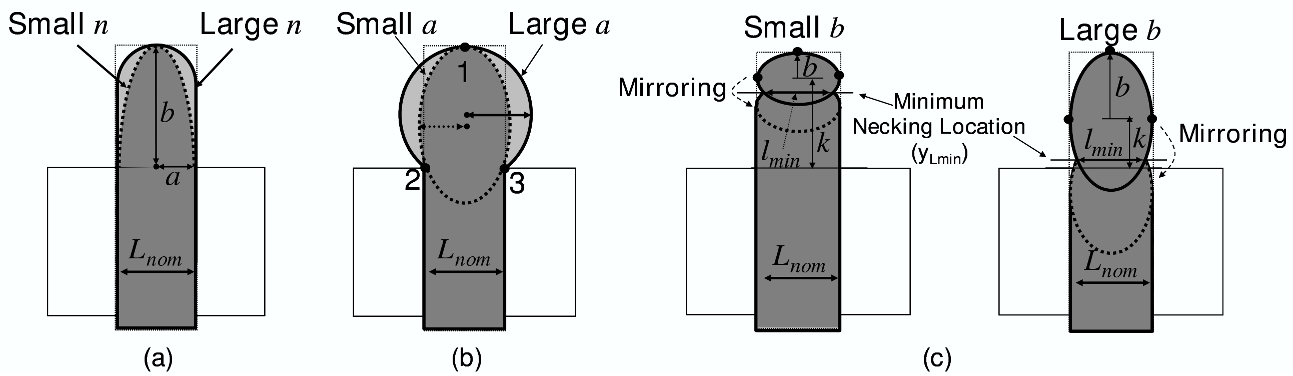

Small n
Large n
b
a
L_{nom}
Small a
Large a
1
2
3
L_{nom}
Small b
Mirroring
b
Minimum
Necking Location
(y_{Lmin})
l_{min}
k
L_{nom}
Large b
b
Mirroring
l_{min}
k
L_{nom}
(a)
(b)
(c)

Figure 5: Line-end shapes represented by the super-ellipse equation.

Figure 5 shows three representative shapes of the line-end; l_i (calculated directly from the super-ellipse parameters), a, b, k, and n. For different shapes of line-end, l_i can be expressed as follows.

Tapering: Figure 5 (a) is the case of tapering, in which the center of the super-ellipse is on the gate edge. l_i can be calculated as

$$l_i = 2a\left(1 - \left|\frac{h_i - k}{b}\right|^n\right)^{\frac{1}{n}}, \tag{4}$$

Bulge: Figure 5 (b) represents a bulge line-end shape, in which the minor axis is greater than L_{nom} and the minimum linewidth between the center of the super-ellipse and the gate edge is greater than or equal to the nominal linewidth (L_{nom}). The corresponding y-coordinate, when the linewidth is L_{nom}, is calculated by

$$y_{L_{nom}} = k - b\left(1 - \left|\frac{L_{nom}/2}{a}\right|^n\right)^{\frac{1}{n}}, \tag{5}$$

The value of l_i for the bulge shape is then computed as

$$l_i = 2a\left(1 - \left|\tfrac{h_i - k}{b}\right|^n\right)^{\frac{1}{n}}, \quad h_i \le y_{L_{nom}} \tag{6}$$

$$l_i = L_{nom}, \qquad 0 \le h_i \le y_{L_{nom}} \tag{7}$$

Necking: Figure 5 (c) gives two examples of necking shapes. It is difficult to ensure smooth changes in linewidth for necking cases by using one super-ellipse. Therefore, we use a simple mirror transform where the mirroring axis is the minimum linewidth (l_{min}) within the fitting range. Corresponding y-coordinate of the mirroring axis $y_{l_{min}}$ is calculated by

$$y_{l_{min}} = k - b\left(1 - \left|\frac{l_{min}/2}{a}\right|^n\right)^{\frac{1}{n}}, \tag{8}$$

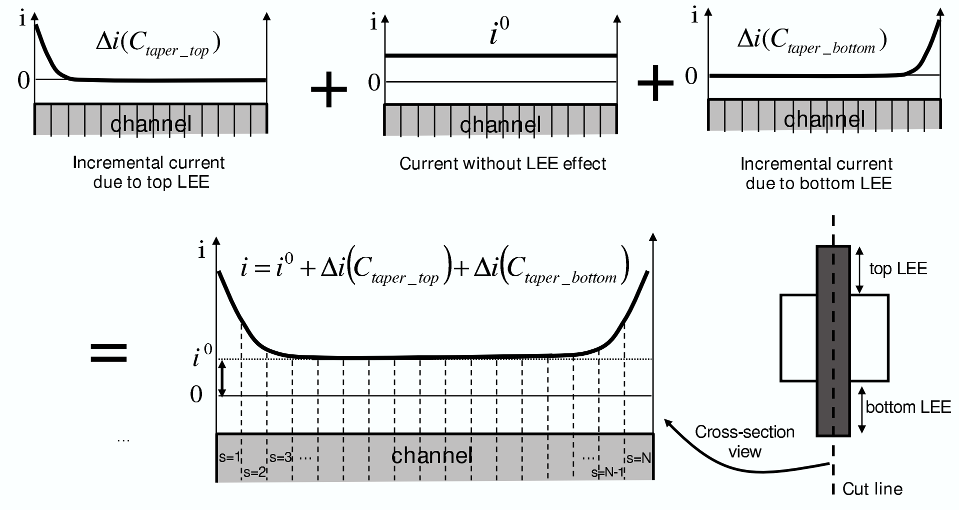
The value of l_i for the necking shape is then

$$l_i = 2a\left(1 - \left|\frac{h_i - k}{b}\right|^n\right)^{\frac{1}{n}}, \qquad h_i \le y_{l_{min}} \tag{9}$$

$$l_i = 2a\left(1 - \left|\frac{y_{l_{min}} - h_i - k}{b}\right|^n\right)^{\frac{1}{n}}, \quad 2y_{l_{min}} - k \le h_i \le y_{l_{min}} \tag{10}$$

$$l_i = L_{nom}, \qquad 0 \le h_i \le 2y_{l_{min}} - k \tag{11}$$

In our modeling, minimum length of the segment (l_{min}) is $60nm$. The super-ellipse model can automatically calculate capacitance from the taper shape. α, β and γ in Eq. 3 are 0.1290, 0.6593 and 3.3990, respectively, obtained from Matlab [3] nonlinear curve fitting. The capacitance unit in our model is $10^{-18}F$. The fitted model shows 2.4% average absolute error with respect to TCAD [2] simulations over 145 different taper shapes.



i
$\Delta i(C_{taper\_top})$
0
channel
Incremental current due to top LEE
+
i
i^0
0
channel
Current without LEE effect
+
i
$\Delta i(C_{taper\_bottom})$
0
channel
Incremental current due to bottom LEE
=
i
$i = i^0 + \Delta i(C_{taper\_top}) + \Delta i(C_{taper\_bottom})$
i^0
0
...
channel
s=1
s=2
s=3
...
...
s=N-1
s=N
top LEE
bottom LEE
Cross-section view
Cut line

Figure 6: Non-uniform channel modeling procedure.

3.2. I_{on} Modeling

Using the capacitance model for taper, we propose a new model for I_{on}. Gate segments near the gate edge are affected more by the taper capacitance as shown in Figure 6. Taper effect exponentially decreases when the distance from the gate edge increases.

The i_{on} of an individual gate segment s is a function of capacitance of the line-end extension. I_{on} is the sum of all segments. s is the segment index that accounts for the distance from the gate edge. C_{taper_top} and C_{taper_bottom} represent taper capacitances at top and bottom gate edges respectively. Thus, total I_{on} current is expressed as

$$I_{on} = \sum_{s=1}^{N} i_{on}(C_{taper\_top}, C_{taper\_bottom}, s, L) \tag{12}$$

$$i_{on}(C_{taper\_top}, C_{taper\_bottom}, s, L) = i^0_{on}(L_s) + \Delta i_{on}(C_{taper\_top}, s, L_s) + \Delta i_{on}(C_{taper\_bottom}, N - s + 1, L_s) \tag{13}$$

Here, $i^0_{on}(L_s)$ is the base current of the gate segment, as measured from a large-width device which is not affected by line-end extension. The additive current (Δi_{on}) for each segment of the gate is modeled as a function of the line-end capacitance (C_{taper}), segment index (s) and linewidth of the segment (L_s). Both $i^0_{on}(L_s)$ and Δi_{on} are defined as follows.

$$\begin{aligned} i^0_{on}(L_s) \quad & = h(L_s) \cdot i^0_{on\_nom} && (14)\\ \Delta i_{on}(C_{taper}, s, L_s) \quad & = f(C_{taper}) \cdot g(s) \cdot h(L_s) && (15)\\ \text{where} \quad & f(C_{taper}) = (C_{taper})^{\alpha} && (16)\\ & g(s) = \gamma e^{-\beta(s-1)} && (17)\\ & h(L_s) = (\frac{L_{nom}}{L_s})^k && (18)\\ & i^0_{on\_nom} \text{ is the base current of a segment with nominal gate length } L_{nom}. && (19) \end{aligned}$$

Our fitting accuracy using Matlab is 0.47% average absolute error for $60nm \le L_s \le 80nm$. Here, α, β and γ are 0.3491, 0.1248 and 0.5197, respectively, and k is 1.2814. I_{on} unit is uA.

3.3. I_{off} Modeling

I_{off} is modeled similarly. However, I_{off} has exponential relationship with the gate length L; we adopt an exponential function to model the I_{off} change with gate length. I_{off} of a gate segment s is a function of capacitance of the line-end extension and is the sum of all segments. C_{taper_top} and C_{taper_bottom} represent taper capacitances at top and bottom gate edges respectively. Thus, total I_{off} current is expressed as

$$I_{off} = \sum_{s=1}^{N} i_{off}(C_{taper\_top}, C_{taper\_bottom}, s, L_s) \tag{20}$$

$$i_{off}(C_{taper\_top}, C_{taper\_bottom}, s, L_s) = i^0_{off}(L_s) + \Delta i_{off}(C_{taper\_top}, s, L_s) + \Delta i_{off}(C_{taper\_bottom}, N-s+1, L_s) \tag{21}$$

$i^0_{off}(L_s)$ is the base current of the gate segment, as measured from a large-width device which is not affected by line-end extension. The additive current (Δi_{off}) for each segment of the gate is modeled as a function of the line-end capacitance (C_{taper}), segment index (s) and linewidth of the segment (L_s). Both $i^0_{off}(L_s)$ and Δi_{off} are defined as follows.

$$\begin{aligned} i^0_{off}(L_s) \quad & = h_1(L_s) \cdot i^0_{off\_nom} && (22)\\ \Delta i_{off}(C_{taper}, s, L_s) \quad & = f(C_{taper}) \cdot g(s) \cdot h_2(L_s) && (23)\\ \text{where} \quad & f(C_{taper}) = (C_{taper})^{\alpha} && (24)\\ & g(s) = \gamma e^{-\beta(s-1)} && (25)\\ & h_1(L_s) = e^{k_1(e^{-k_2 L_s} - e^{-k_2 L_{nom}})} && (26)\\ & h_2(L_s) = e^{k_3(e^{-k_4 L_s} - e^{-k_4 L_{nom}})} && (27)\\ & i^0_{off\_nom} \text{ is the base current of a segment with nominal gate length } L_{nom}. && (28) \end{aligned}$$

We find the coefficients by numerical fitting. Here, α, β and γ are 0.4455, 0.5337 and 11.5533, respectively, and k_1, k_2, k_3 and k_4 are 1036.46, 0.071953, 4864.38 and 0.10468, respectively. The model shows 1.28% average absolute error compared to TCAD simulation for $64nm \le L_s \le 76nm$. I_{off} unit is pA.

3.4. Misalignment model

With misalignment, the lengths of segments near the channel edge change. Since segments in the channel affect I_{on} and I_{off} differently compared to the segments in the taper, we first determine whether the segment belongs to channel or taper. Misalignment error is a vector component quantity in X and Y directions. We assume that the minimum poly-to-diffusion spacing is larger than the misalignment error, so that misalignment errors do not cause any spurious transistor channels.

Therefore, X-directional misalignment is neglected. Given a misalignment condition, we can calculate the I_{on} and I_{off} of the entire gate by summing up the segments' current values (i_{on} and i_{off}). Let the number of possible sites of poly placement due to misalignment be N_{sites}, [*] the probability of the corresponding m misalignment be $P(m)$, and the current under such misalignment be $I(m)$. We can calculate the expected current I_{exp} by integrating the product of $P(m)$ and $I(m)$ over the misalignment range.

$$I_{exp} = \sum_{m=1}^{N_{sites}} P(m)I(m) \tag{29}$$

4. EXPERIMENTS AND DISCUSSION

4.1. Model Accuracy

We apply our proposed model to the ideal rectangular line-end. Table 1 shows the comparisons of our model results and the TCAD results. We measure I_{on} and I_{off} changing the line-end length. Column 1 shows the drawn line-end length. Columns 2 and 3 show the I_{on} and I_{off} values without considering the line-end effects. Comparing column 4 with 6 and 5 with 7 shows the accuracy of our model. In columns 8 and 9, we show the impact of misalignment errors.

When we reduce the line-end extension, we can see the decreasing trends of I_{on} and I_{off}, since small line-end extension results in small gate capacitance and hence higher threshold voltage. This result implies that an unnecessarily large line-end rule is not desirable from the electrical point of view. Note that in this case, since the shape is perfect rectangular, misalignment errors do not cause linewidth variation in the channel, so that the impact of misalignment is negligibly small.

LEE (nm)	Drawn		Model w/o misalignment		DaVinci		Model w/ misalignment	
	I_{on} (μA)	I_{off} (pA)	I_{on} (μA)	I_{off} (pA)	I_{on} (μA)	I_{off} (pA)	I_{on} (μA)	I_{off} (pA)
100	120.156	128.283	120.940	130.474	120.156	128.283	120.934	130.458
80			120.677	127.041	120.109	127.506	120.671	127.020
40			119.918	117.510	119.651	120.519	119.908	117.455
20			119.172	109.625	118.886	110.881	119.165	109.461
10			118.686	103.358	117.902	100.865	118.627	102.856

Table 1: Model accuracy and impact of misalignment on rectangular line-end.

4.2. Evaluation of the line-end shapes

We also evaluate the line-end shapes generated by the proposed super-ellipse model. Tapering is a typical shape in post-OPC silicon image. Corner rounding is represented by the super-ellipse parameter n. Larger n results in less corner rounding, but increases mask cost in terms of mask writing time and mask inspection since aggressive OPC needs to be applied. Bulge may be caused by inaccurate OPC and may be amplified under defocus. The degree of bulge shape is determined by a and having positive k. Necking is a reduction in linewidth that is caused by an excessive OPC hammerhead, i.e., the hammerhead results in narrow linewidth under defocus at the channel edge even if the hammerhead can compensate for corner rounding error under best focus condition.

For each shape generated from a super-ellipse, in Figure 5, we change the line-end length by shifting the entire poly shape and calculate I_{off} for each.[†] When we reduce the line-end length, since the line-end part of the poly gate becomes enclosed by the diffusion, gate segments in the line-end turn into gate segments in the channel.

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[*] Since 3σ misalignment error for 65nm technology is 11nm [1] and our segmentation size is 5nm, we assumed N_{sites} to be 5. The third site represents no misalignment error and the others represent movement of poly segments within the maximum misalignment bound.

[†] We limit the minimum line-end length to $20nm$, to avoid line-end shortening by overlay error.

Table 2 shows the dependence of I_{on} and I_{off} on the super-ellipse exponent and the line-end extension, i.e., on the *sharpness* of the line-end. In this case, the super-ellipse semi-minor and semi-major axes are fixed at 35nm and 100nm, respectively. As we increase n, the tapering becomes more rectangular and the I_{off} variation is reduced. However, as noted above, increased n requires more complex OPC and can increase OPC and mask costs. Note that in the table, some cases are out of the boundary of our model, but it is obvious that those cases must be avoided in design, so as to not increase leakage current too much.[‡]

	Super-ellipse exponent (n)											
	2.5		3.0		3.5		4.0		4.5		5.0	
LEE (nm)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)
100	122.0	149	122.0	149	122.0	149	122.0	149	122.0	149	122.0	149
90	121.9	149	121.9	148	121.9	148	121.9	149	121.9	149	121.9	149
80	121.9	150	121.9	148	121.9	148	121.9	148	121.9	148	121.9	148
70	121.9	158	121.8	151	121.8	148	121.8	147	121.8	147	121.8	147
60	122.0	184	121.8	159	121.7	152	121.7	149	121.7	147	121.7	147
50	122.3	291	121.9	187	121.7	163	121.7	154	121.6	150	121.6	147
40	122.9	-	122.2	-	121.9	199	121.7	170	121.6	158	121.5	152
30	-	-	-	-	122.2	-	121.9	236	121.7	188	121.5	168
20	-	-	-	-	-	-	-	-	121.9	-	121.7	263

Table 2: I_{on} and I_{off} changes with line-end extension and *sharpness* for 200 nm NMOS.

Table 3 shows the I_{on} and I_{off} dependence on the $fatness$ of bulge shape and the line-end length. Super-ellipse exponent is fixed at $n = 3.0$. Since we use a contour that passes through three points in Figure 5 (b), if we change the semi-minor axis a, the other parameters b and k are determined automatically by solving the super-ellipse equation. Column 2 is the same configuration as column 3 in the Table 2. For the bulge shape line-ends, I_{off} variation is small compared to the tapering (sharpness) case.

	Super-ellipse semi-minor axis (a) (nm)											
	35		36		37		38		39		40	
LEE (nm)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)
100	122.0	149	122.0	149	122.0	149	122.0	149	122.0	149	122.0	149
90	121.9	148	121.9	144	121.8	141	121.8	139	121.8	138	121.7	137
80	121.9	148	121.6	134	121.5	127	121.3	123	121.1	120	121.0	119
70	121.8	151	121.3	127	121.0	118	120.6	113	120.3	110	120.0	109
60	121.8	159	121.0	123	120.4	113	119.9	108	119.4	105	118.9	103
50	121.9	187	120.7	121	119.9	110	119.2	104	118.5	101	117.8	99
40	122.2	-	120.5	123	119.4	108	118.5	101	117.6	98	116.8	96
30	122.8	-	120.4	142	119.1	112	117.9	101	116.8	96	115.8	94
20	-	-	-	-	119.0	-	117.6	130	116.3	104	115.1	95

Table 3: I_{on} and I_{off} changes on line-end length and $fatness$ for 200 nm NMOS.

Table 4 shows the I_{off} dependence on the location of necking and the line-end extension. For this simulation, we use a super-ellipse with 100nm line-end. By changing the semi-major axis, we control the necking location where the linewidth is minimized. After that, we shift the entire poly shape downward to model the reduction of the line-end design rule. The table shows that necking makes the device leaky, and that leakage current increases or decreases with line-end length. Especially, in case that the necking occurs near the channel edge (for large semi-major axis b), I_{off} increases substantially for all line-end lengths. This is because the minimum linewidth of the necking is enclosed by the channel due to existence of misalignment. This result implies that if we can not avoid necking shapes, necking location must be placed at least as far as the maximum misalignment error from the channel edge. However, this may require a longer line-end.

[‡] For the cases of small n, there still exists excessive leakage increase due to the small line-width (about 60nm), near the end of the line-end.

From all the experiments we observe that as line-end extension becomes smaller, I_{on} and I_{off} are reduced, due to the reduced line-end capacitance. However with tapering effects, if the small linewidth of the line-end segments get into the channel area due to overlay issues, I_{off} increases greatly. We also observe that the impact of line-end itself is negligibly small due to the electrical characteristics, but combined with line-end pull-back and misalignment, non-rectangular and small linewidth of the line-end segments leads to large variation in I_{on} and I_{off}.

	Super-ellipse semi-major axis (b) (nm)									
	60		50		40		30		20	
	Necking location ($y_{l_{min}}$ in Eq. 8) from gate edge (nm) for 100nm LEE									
	5		20		40		55		70	
	Minimum linewidth (l_{min} in Eq. 8) (nm) at necking location									
	65.0		64.5		67.0		67.0		67.0	
LEE (nm)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)	I_{on} (uA)	I_{off} (pA)
100	122.2	182	122.0	150	122.0	149	122.0	149	122.0	149
90	122.6	310	122.0	157	121.9	149	121.9	149	121.9	149
80	122.8	288	122.2	244	121.9	148	121.9	148	121.9	148
70	122.8	230	122.6	352	121.8	148	121.8	147	121.8	147
60	122.7	203	122.7	267	121.8	165	121.7	146	121.7	146
50	122.6	192	122.5	220	121.9	186	121.6	148	121.6	145
40	122.4	191	122.4	203	121.8	167	121.6	177	121.4	143
30	122.4	211	123.3	202	121.6	156	121.6	167	121.3	153
20	122.7	-	123.3	325	121.5	172	121.4	155	121.3	168

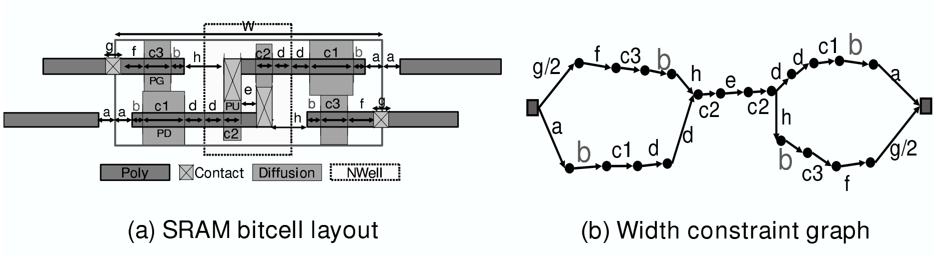
Table 4: I_{on} and I_{off} change with line-end extension and *necking* for 200 *nm* NMOS.

4.3. Application to Design

We now analyze how the line-end rule affects design area and leakage current.

SRAM bitcell. Figure 7 (a) shows an example of bitcell layout, while (b) shows the corresponding layout constraint graph that defines the width of the bitcell. In the figure, a is half of the line-end gap, b is the length of the line-end extension, $c1$, $c2$ and $c3$ are the respective widths of pull-down (PD), pull-up (PU) and pass-gate (PG) transistors. Also, d is the space rule between diffusion layer and N-well, e is the space between diffusion layers, f is the space between contact and diffusion, and g is the width of the contact shape. Since the line-end extension (b) occurs twice in the critical path of the width constraint graph, when we reduce the length of line-end by x, the bitcell width decreases by $2x$ and this will reduce the bitcell size.

We evaluate the area and the leakage current of the bitcell by changing the sharpness of the tapering line-end as well as the length of the line-end. Figure 8 shows the tradeoff curve under given design rules for 65nm technology. The I_{off} value in the figure is total leakage current of all transistors, i.e., two PD, two PG and two PU, in the bitcell. To calculate PU (PMOS) leakage current, we assume that unit width leakage of the PMOS is half of that of NMOS. We also assume that the line-end length of PUs is fixed, since it is determined by other fixed design rules, i.e., e and d, and cannot be reduced further without disconnecting from electrodes. Table 5 shows how much SRAM bitcell area can be reduced by line-end extension reduction under given leakage power constraints. Note that if we permit about a factor of 2 leakage increase, we can reduce the line-end design rule to about 50nm $\sim$ 20nm, and reduce the bitcell size by about 7.69% $\sim$ 12.31%, depending on the super-ellipse exponent.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c1
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(a) SRAM bitcell layout (b) Width constraint graph

Figure 7: SRAM layout and width constraint graph.

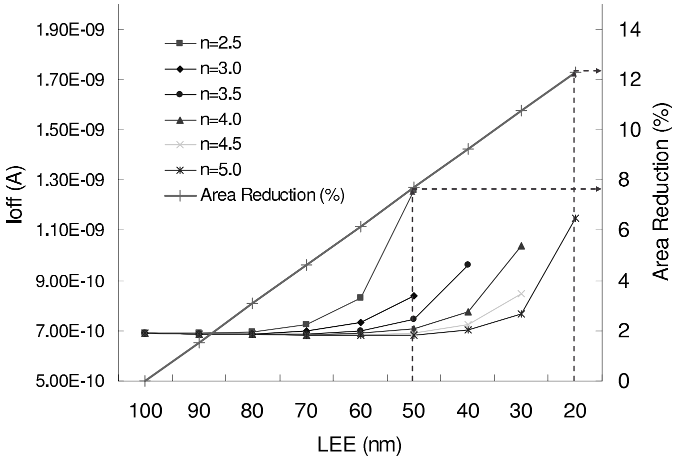
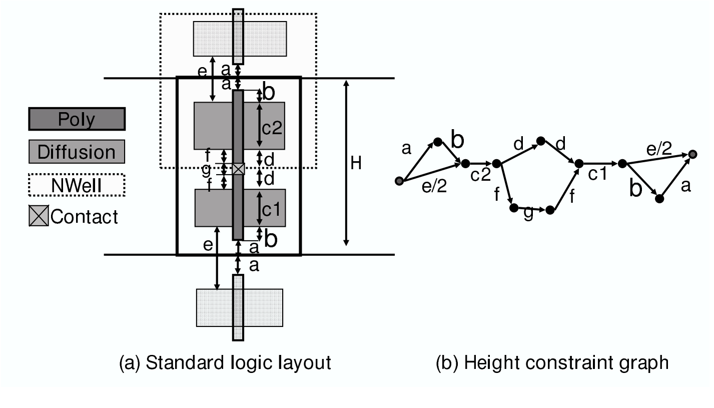


Figure 8: Area-leakage tradeoff for an SRAM bitcell.

Standard Cell Logic. Similar to the SRAM bitcell, we analyze the standard cell logic area and leakage current based on the line-end design rule and the sharpness of tapering. Figure 9 (a) shows a basic layout structure of a standard inverter cell; (b) shows the corresponding height constraint graph. Notation is same as that given for the SRAM bitcell except that $c1$ and $c2$ are the gate widths of NMOS and PMOS transistors, respectively. Figure 10 shows the tradeoff curve under given design rules for 65nm technology. We assume NMOS and PMOS width to be 400 *nm* and 800 *nm*, respectively, and unit width leakage current of the PMOS is half of that of NMOS. Unlike the SRAM case, line-end length of PMOSs also can be reduced. Table 6 shows how much standard cell area can be reduced by line-end length reduction under given leakage power constraints. From Figure 10 and Table 6, if a factor of 2 leakage increase is allowed, 5.52% $\sim$ 8.84% of logic area can be reduced by line-end design rule relaxation.


Poly
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(a) Standard logic layout (b) Height constraint graph

Figure 9: Inverter cell layout and height constraint graph.

n	Allowed leakage increase (%)					
	0	30	60	100	200	300
2.5	1.54	6.15	6.15	6.15	7.69	7.69
3.0	3.08	7.69	7.69	7.69	9.23	9.23
3.5	4.62	7.69	9.23	9.23	9.23	10.77
4.0	6.15	9.23	9.23	10.77	10.77	10.77
4.5	7.69	10.77	10.77	10.77	10.77	12.31
5.0	7.69	10.77	10.77	12.31	12.31	12.31

Table 5: SRAM bitcell area reduction (%) under allowed leakage increase (%).

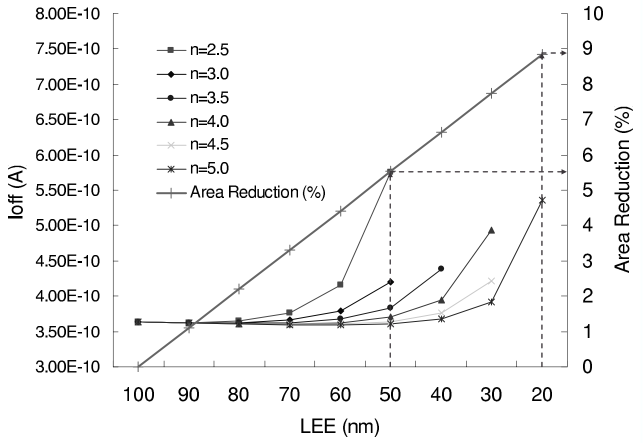

Figure 10: Area-leakage tradeoff for standard logic.

5. CONCLUSIONS AND ONGOING WORK

In this paper, we have proposed a novel modeling framework to model the electrical impact of line-end shapes. We model the line-end shape by a general super-ellipse equation. We model the capacitance between line-end and the gate channel, and derive I_{on} and I_{off} models from it, considering misalignment errors in the manufacturing process. Our model accuracy is within 0.47% and 1.28% for I_{on} and I_{off}, respectively, compared to 3-D TCAD simulation. Our results show that different line-end lengths can affect I_{on} and I_{off} by 4.5% and 30%, respectively, and that different line-end shapes, combined with misalignment, can increase I_{off} by several times compared to the ideal line-end shape. Applying the model to SRAM bitcell and inverter cell layout, we observe that the traditional line-end extension design rule can be reduced further without affecting electrical characteristics of the circuits. Our next goal is to provide rules of thumb by which OPC engineers can optimize line-end shapes, and finally suggest electrically safe, lithographically robust yet cost-effective, area-conserving line-end design rules.

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n	Allowed leakage increase (%)					
	0	30	60	100	200	300
2.5	2.21	4.42	4.42	5.52	5.52	5.52
3.0	2.21	5.52	5.52	6.63	6.63	6.63
3.5	3.31	6.63	6.63	6.63	7.73	7.73
4.0	4.42	6.63	7.73	7.73	7.73	7.73
4.5	5.52	7.73	7.73	7.73	8.84	8.84
5.0	5.52	7.73	8.84	8.84	8.84	8.84

Table 6: Logic area reduction (%) under allowed leakage increase (%).

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