Investigation of Diffusion Rounding for Post-Lithography Analysis

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Abstract – Due to aggressive scaling of device feature size to improve circuit performance in the sub-wavelength lithography regime, both diffusion and poly gate shapes are no longer rectilinear. Diffusion rounding occurs most notably where the diffusion shapes are not perfectly rectangular, including common L and T-shaped diffusion layouts to connect to power rails. This paper investigates the impact of the non-rectilinear shape of diffusion (i.e., sloped diffusion or diffusion rounding) on circuit performance (delay and leakage). Simple weighting function models for I_{on} and I_{off} to account for the diffusion rounding effects are proposed, and compared with TCAD simulation. Our experiments show that diffusion rounding has an asymmetric characteristic for I_{off} due to the differing significance of source/drain junctions on device threshold voltage. Therefore, we can model I_{on} and I_{off} as a function of slope angle and direction. The proposed models match well with TCAD simulation results, with less than 2% and 6% error in I_{on} and I_{off}, respectively.

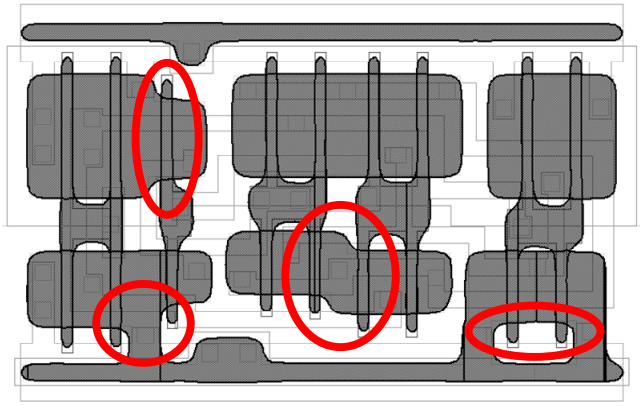

Figure 1. Lithography simulation contour showing diffusion rounding in a layout at the 90nm technology node.

I. Introduction

In modern CMOS technologies, minimum-sized devices are commonplace – particularly in low-power designs. In such gates, transistor width is only a few times larger than the minimum feature size and hence an understanding of gate width variation is important for accurate modeling of device characteristics (namely, delay and power). With the use of various resolution enhancement techniques (RETs) and design for manufacturability (DFM) methodologies, sub-wavelength lithography remains possible below the 65nm technology node [1]. However, new manufacturing problems due to the imperfect printing of gate length and width affecting parametric yield have become a major issue in post-lithography analysis [2],[3]. Many works have investigated the non-rectilinear poly gate shape and sought to model performance (I_{on} and I_{off}) to account for the irregularity of the poly gate [4]-[10]. Most of these works slice non-rectilinear gates along the device width at a certain level of granularity, followed by a summation of I_{on} (or I_{off}) of each slice to model I_{on} (or I_{off}) of the non-rectilinear devices. More recent work has been proposed to include the edge effect in post-lithography simulation with the STI process [5],[17]. References [11],[12],[13] discuss edge effects, which are manifested as an unequal distribution of drive and leakage current densities across the width of the channel. In the Berkeley Short-Channel IGFET Model (BSIM) [14], this effect is modeled using the narrow-width component of the threshold voltage model [13]. The observation that the threshold voltage of modern MOSFETs is much lower near the edges than the center of the channel is central to the method proposed in this paper. With edge effects, we observe inverse narrow width effect (i.e., V_{th} decreases as channel width decreases).

Most previous work assumes that the diffusion shape under the poly gate region is perfectly rectangular. However the diffusion shape is not actually rectilinear, because L and T-shaped diffusion regions often lead to a rounded diffusion under the poly gate. Figure 1 shows the lithography simulation contour of poly and diffusion in a 90nm standard cell using Calibre [15]. As can be seen from the figure, diffusion rounding happens in various locations with different forms.

In the sub-wavelength lithography regime, both gate width variation and diffusion rounding should be included in device analysis and characterization for accurate device modeling. Diffusion rounding is defined as occurring when source and drain diffusion areas do not form a perfect rectilinear shape under the poly gate region due to a 2D diffusion layout. These

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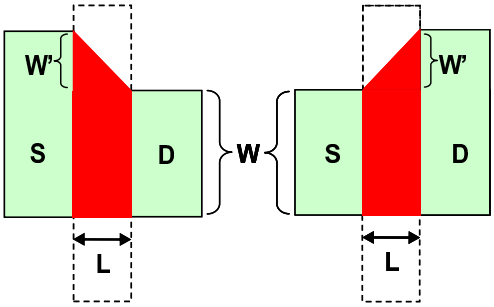
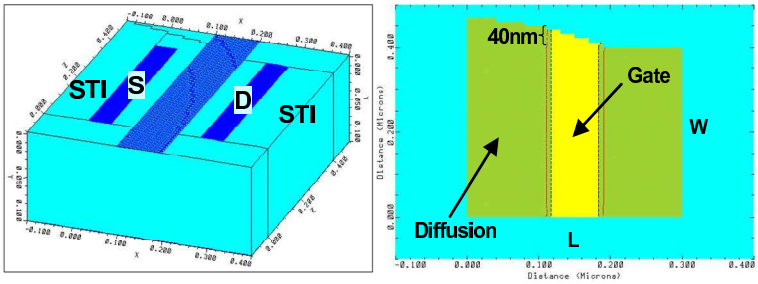


(a)



(b)

Figure 2. (a) Test patterns for diffusion rounding analysis; source-side (left) and drain-side (right) diffusion rounding. (b) TCAD profiles; 3D view (left) and top view (right) showing 40nm source-side diffusion rounding under the gate area.

Table 1. TCAD Model Parameters.

Parameters	Value
L_physical	70nm
Width	400nm
Vdd	1.2V
T_{ox}	2nm
Channel doping	3.0e+18 cm^{-3}
NSUB	3.0e+15 cm^{-3}
Junction depth	14nm
Line-end extension	100nm
S/D electrode length	50nm
S/D electrode width	400nm
S/D region to gate poly	50nm
STI width	100nm
STI depth	100nm

Table 2. I_{on} and I_{off} with diffusion rounding at source side (a) and drain side (b).

(a)

Source side		nominal	5nm	10nm	20nm	30nm	40nm	20nm both	40nm both
NMOS	I_{on} (μA)	232	235	236	237	238	241	245	255
	I_{off} (pA)	249	241	232	217	206	198	259	269
	I_{on_norm}	1.00	1.01	1.01	1.02	1.03	1.04	1.06	1.10
	I_{off_norm}	1.00	0.96	0.93	0.87	0.83	0.79	1.04	1.08
PMOS	I_{on} (μA)	125	127	127	128	129	130	133	138
	I_{off} (pA)	63.5	58.3	59.8	56.8	54.4	52.6	66.2	68.9
	I_{on_norm}	1.00	1.01	1.01	1.02	1.03	1.03	1.06	1.10
	I_{off_norm}	1.00	0.92	0.94	0.89	0.86	0.83	1.04	1.09

(b)

Drain side		nominal	5nm	10nm	20nm	30nm	40nm
NMOS	I_{on} (μA)	232	234	235	237	239	240
	I_{off} (pA)	249	289	279	254	255	245
	I_{on_norm}	1.00	1.01	1.01	1.02	1.03	1.04
	I_{off_norm}	1.00	1.16	1.12	1.02	1.02	0.98
PMOS	I_{on} (μA)	125	127	127	128	129	130
	I_{off} (pA)	63.5	62.0	69.5	65.5	65.7	63.4
	I_{on_norm}	1.00	1.01	1.01	1.02	1.03	1.03
	I_{off_norm}	1.00	0.98	1.09	1.03	1.04	1.00

bent diffusion layouts in L or T shapes often exist to connect source or drain to power supply (VDD or VSS) as shown in Figure 1. The extent of diffusion rounding mainly depends on the minimum distance from gate poly to the bent diffusion region. In 90nm and below, the minimum distance is about half of the minimum gate length. Thus the diffusion rounding size under the gate region is not negligible and we now see several 10s of nm of rounding in 90nm technology based on technology CAD (TCAD) simulation [15].

In this paper, we investigate the impact of diffusion rounding on device performance using a 3D TCAD simulator [16]. Simple weighting function models for both I_{on} and I_{off} are proposed to include this effect in post-lithography analysis. The rest of the paper is organized as follows. The 3D TCAD simulation setup for investigation of diffusion rounding effects is explained in detail in Section II. Section III describes how to calculate and verify weighted I_{on} and I_{off} models that can capture this effect. Section IV discusses results of diffusion rounding on a typical D flip-flop cell from a 90nm library in terms of leakage and delay. Section V concludes the paper.

II. TCAD Simulation of Diffusion Rounding

To understand the impact of diffusion rounding on device performance in terms of delay and leakage, we employ a 3D TCAD simulator [16] to generate the diffusion rounding shapes, and then measure I_{on} and I_{off}.†

Figure 2(a) shows two test patterns for diffusion rounding analysis in TCAD simulation; one includes diffusion rounding on the source side (left) and the other on the drain

† I_{off} in this paper refers only to subthreshold leakage; gate leakage is considered negligible.

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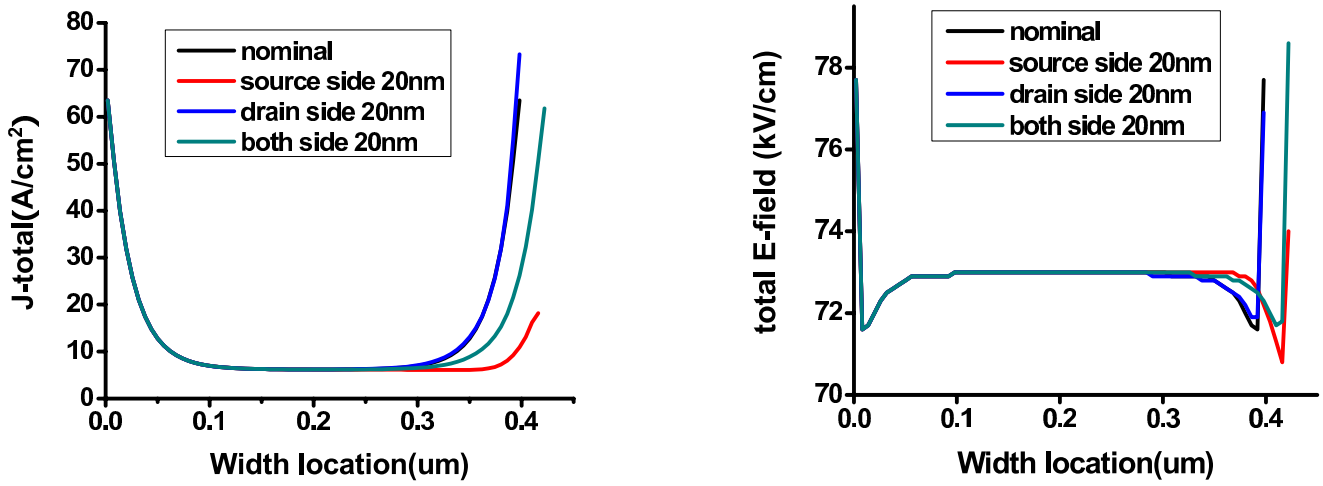

(a) (b)

Figure 3. (a) Total current density and (b) total electric field along device width for several diffusion rounding cases.

side (right). Both 3D and top views of TCAD profiles with 40nm diffusion rounding are shown in Figure 2(b). We use nominal NMOS and PMOS devices with effective length 70nm and width of 400nm. Slope size, *w'*, is swept from 5nm to 40nm. TCAD model parameters used to generate the test device are shown in Table 1. TCAD simulation results are shown in Table 2 for the two test patterns. Results of "20nm both" and "40nm both" cases in which both source and drain side increase by 20nm and 40nm respectively are shown for comparison. As can be seen from the table, there are small changes in I_{on} both for source-side and drain-side diffusion rounding. However, it is interesting to see that I_{off} results are rather asymmetric; I_{off} decreases due to source-side diffusion rounding (which is the common case in actual layouts) up to 20% in NMOS (17% in PMOS). On the other hand, for drain-side diffusion rounding I_{off} increases then saturates as slope size increases.

The impact of diffusion rounding on I_{on} can be explained by effective gate area change without any dependency on the rounded diffusion direction. For I_{off}, the leakage current reduction by source-side diffusion rounding is justified because in that case the rounded diffusion increases the effective device width (at source side) and slightly reduces the narrow-width effect (i.e., increases V_{th} of the device) [13],[17]. The increased V_{th} at the edge will reduce the leakage current exponentially. Therefore, we see smaller leakage than nominal due to source-side diffusion rounding. The narrow-width effect and corresponding V_{th} change are only relevant for source-side rounding since V_{th} is defined at the source rather than the drain. In summary, both I_{on} and I_{off} variations by the diffusion rounding can be explained by its size (*w'*) and location (source or drain).

Another factor contributing to this phenomenon is that VDD is applied at the drain; therefore source-side diffusion rounding decreases E-field at the source junction by increasing the effective channel length. On the other hand,

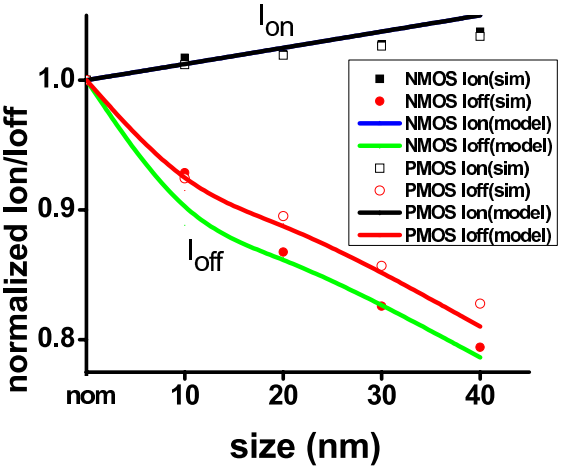

Figure 4. Comparison of TCAD simulation results with proposed models for I_{on} and I_{off}.

drain-side diffusion rounding does not increase the effective channel length anywhere along the source junction. Total current density and E-field plots along the device width of nominal, nominal+20nm, and the two test patterns of slope size (*w'*) 20nm are shown in Figure 3 (a) and (b) respectively. As can be seen from the figures, diffusion rounding at source-side (red line) presents smaller current density and E-field at the device edge thus we expect smaller edge effect. 20nm drain-side diffusion rounding (blue line) shows current density and E-field values similar to the nominal device (black line). Again, these results indicate reduced I_{off} by source-side diffusion rounding and small change in I_{off} by drain-side diffusion rounded devices from a nominal device.

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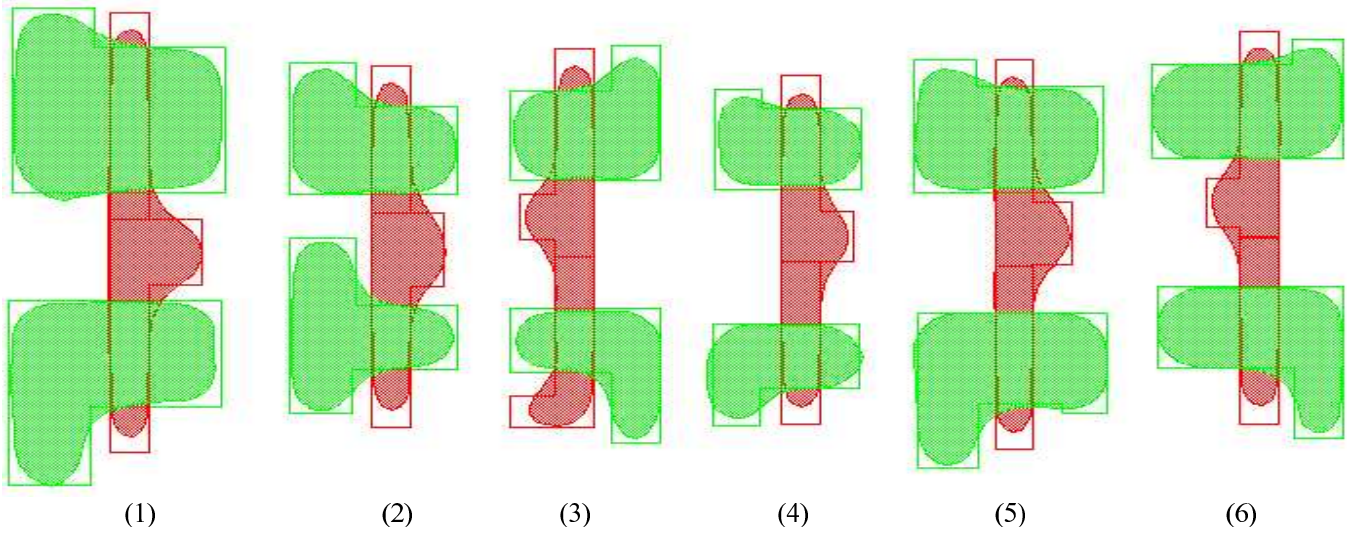

Figure 5. Lithography simulation contour of test patterns. (only NMOS device # 1 ~ 6)

Table 3. TCAD simulation results and comparison of test pattern post-lithography contours to proposed models.

NMOS device #	W_{drawn} (nm)	nominal		litho-contour		contour2nom (%)		model			*model2contour (%)*	
		I_{on} (μA)	I_{off} (pA)	I_{on} (μA)	I_{off} (pA)	I_{on}	I_{off}	w' (nm)	I_{on} (μA)	I_{off} (pA)	I_{on}	I_{off}
1	274	136.15	6.53	137.48	4.88	0.98	-25.24	15	139.88	4.95	***1.74***	***1.41***
2	164	85.33	5.87	90.63	3.59	6.21	-38.85	20,15	91.40	3.71	***0.85***	***3.50***
3	164	85.33	5.87	87.81	5.20	2.91	-11.36	19	88.62	5.12	***0.93***	***-1.51***
4	164	85.33	5.87	88.96	5.43	4.25	-7.41	11	87.23	5.22	***-1.94***	***-4.02***
5	234	117.66	6.29	120.09	5.43	2.07	-13.71	15	120.17	5.55	***0.07***	***2.18***
6	209	106.11	6.14	108.64	5.70	2.38	-7.19	19	109.33	5.36	***0.63***	***-5.92***

III. Modeling and Verification

As explained in the previous section, the impact of diffusion rounding on device saturation current (I_{on}) can be explained by an effective gate area change without consideration of location dependency. Thus, the effect of diffusion rounding on I_{on} can be modeled as

$$I_{on} = I_{on_nom} * \left[1 + \frac{(w'/2)}{W}\right] \quad (1)$$

Here I_{on_nom} is the on-current of the nominal rectangular device and w' is the height of diffusion rounding. W is the width of the nominal device (i.e., W_{drawn}). In reality, diffusion rounding is not strictly a straight line. However we make this approximation as shown in Figure 2(a).

On the other hand, leakage current exhibits a location dependency. There is only a small change due to drain-side diffusion rounding while source-side diffusion rounding reduces leakage by a more significant factor. We focus on modeling I_{off} for source-side rounding since most layouts show primarily source-side diffusion rounding to connect to power lines (VDD and VSS) and to share the source. We model I_{off} due to source-side diffusion rounding as an exponential function of effective channel length at the edge:

$$I_{off} = I_{off_nom} * K_1 * \exp\left(\frac{L_{nom}}{L'}\right) \quad (2)$$

Here I_{off_nom} is the off current of the nominal rectangular device, K_1 is a fitting parameter (0.33 for NMOS and 0.34 for PMOS in this analysis), L_{nom} is nominal channel length, and L' is the effective channel length at the edge of diffusion rounding. L' can be calculated from the square root of $(w'^2 + L_{nom}^2)$. The fitting parameter K_1 is constant for a technology. For different technology nodes this parameter is empirically fit to observed data.

Figure 4 shows the accuracy of the proposed models for different slope sizes from 10nm to 40nm. As can be seen, the proposed models capture the effect of diffusion rounding well in both I_{on} and I_{off} across different slope sizes.

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Table 4. Comparison of leakage, delay, and setup time for DFFX1 between nominal and w/ diffusion rounding effect. CLK→ Q and setup time are taken at 90ps input transition time and 6.52fF output load (from the 7x7 LUT).

		nominal (w/o diffusion rounding)	w/ diffusion rounding	*delta (%)*
leakage (nW)		138.69	83.49	*39.8*
CLK→Q (ps)	fall	70.57	68.54	*2.9*
	rise	76.07	74.07	*2.6*
setup time (ps)	fall	20.43	18.08	*11.5*
	rise	42.71	35.01	*18.0*

To verify the proposed models with actual device lithography contours, we perform lithography simulations on six common device patterns that form different diffusion rounding shapes under the gate area. We then generate device structures based on these contours in TCAD simulations to measure I_{on} and I_{off}.

Figure 5 shows the lithography contours for the six test inverter patterns. Empty solid lines are for drawn poly and diffusion and filled contours are for simulated poly and diffusion obtained using Calibre Workbench [15]. In this study we only generate NMOS devices (bottom devices) with the TCAD simulator. Devices 1, 3, 4, 5, 6 have diffusion rounding at either the top edge or bottom edge while Device 2 exhibits diffusion rounding at both edges. In these test patterns, the slope size varies from 11nm (Device 4) to 20nm (Device 2). Table 3 presents the I_{on} and I_{off} simulation results for the nominal drawn poly/diffusion and litho-contour based poly/diffusion. As shown in the contour2nom column, I_{on} changes by up to 7% and I_{off} differs by up to 40% (Device 2) due to diffusion rounding. The proposed models accurately capture I_{on} and I_{off} with diffusion rounding, with less than 2% and 6% error in I_{on} and I_{off}, respectively (*model2contour* column). In Device 1, the model for I_{on} overestimates the diffusion rounding impact because the proposed model cannot capture the poly flaring effects occurring in that device. In Devices 4 and 6, the model for I_{off} underestimates the diffusion rounding impact because the model ignores the line edge roughness (LER) effects along the width. The remaining errors likely arise from the rectangular approximation of diffusion rounding geometry in the proposed models.

IV. D Flip-Flop Case Study

To quantify the performance impact of diffusion rounding on actual standard cells, we examine the heavily-used DFFX1 (size 1 D-flip-flop) layout from a 90nm library and perform lithography simulation. The lithography simulated contour is then analyzed to determine the size and location of the diffusion rounding cases. In the DFFX1, 11 PMOS (out of 14 total) and 5 NMOS (out of 14 total) devices exhibit appreciable diffusion rounding. The extent of diffusion rounding varies from 13nm to 26nm (*w'*) using a 90nm lithography recipe.

Based on these results we calculate I_{on} and I_{off} using our proposed models. Finally, we incorporate diffusion rounding effects in the SPICE netlist by modifying the mobility values of the devices containing diffusion rounding. In this analysis we ignore the minor capacitance impact due to diffusion rounding. The comparison of leakage power, CLK→Q delay and setup time for DFFX1 between the nominal and diffusion rounding cases is shown in Table 4. Diffusion rounding reduces leakage power by about 40%, CLK→Q delay by about 3%, and setup time by 12-18 %.

V. Conclusions and Future Work

We investigate the impact of the non-rectilinear shape of diffusion on device on- and off-currents. We observe that diffusion rounding on the source side leads to a fairly appreciable reduction in subthreshold current, while at the same time providing a small boost in on-current. We propose simple models to capture the diffusion rounding effects in post-lithography analysis. The test patterns studied, taken from a 90nm library, show that neglecting diffusion rounding can lead to 7% (40%) error in predicting I_{on} (I_{off}). The proposed models show good match to simulation results and are within 2% in I_{on} and 6% in I_{off}. A layout analysis of a commonly used sequential cell shows that diffusion rounding potentially reduces leakage, CLK→Q delay, and setup time. In our analysis we assume that there is no line edge roughness effect or poly flaring at the edge of the gate. Combining LER with diffusion rounding to create general models that account for various types of device shape irregularities is worthy of further investigation.

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