

A DOE Set for Normalization-Based Extraction of Fill Impact on Capacitances

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Abstract—Metal fills, which are used to reduce metal thickness variations due to chemical-mechanical polishing (CMP), increase the capacitances in a circuit. Although current extraction tools are accurate in handling grounded fills and regular interconnects, for floating fills, these tools are based on certain approximations, such as assuming that floating fills are grounded or each fill is merged with neighboring ones. To reduce such inaccuracies, we provide a design of experiments (DOE), which will be used in addition to what is available in the extraction tools for regular interconnects. Through the proposed DOE set, a design or mask house can generate normalized fill tables to remove the inaccuracies of the extraction tools in the presence of floating fills. The capacitance values are updated using these normalized fill tables. The proposed DOE enables extensive analyses of the fill impacts on coupling capacitances. We show through extensive 3D field solver simulations that the assumptions used in extractors result in significant inaccuracies. We present analyses of fill impacts for an example technology, and also provide analyses using the normalized fill tables to be used in the extraction flow for three different standard fill algorithms.

I. INTRODUCTION

In order to reduce the metal height variations within a die, (dummy) fills are added to the layout of metal layers. Addition of fills can be either handled by the design house, mask house, or the foundry. As fills are inserted to reduce the thickness variations caused by chemical-mechanical polishing, ideally, they should not alter the capacitances of and between interconnects. Although design rules help reduce the increase in capacitances, these rules are by no means sufficient to eliminate the impact of fills on capacitances. For example, second neighboring layer coupling can be significant, yet there are no explicit design rules to restrict such coupling. Furthermore, current extraction tools are not very accurate in providing the impact of fills on capacitances.

The industry needs a way to incorporate the impact of fills during extraction. In this paper, we show a parameterized DOE-based method to increase the accuracy of extraction in the presence of fills. Following a motivation section, where we identify the inaccuracies introduced by current extraction tools, we present the proposed flow in the methodology section. In Section V, we provide the basic structure for our DOE and show how the DOE is implemented. In Section VI, we provide an insight on the keep-off design rule, which is a very important design rule related to fills. We then provide a means to include the height variations due to CMP. In the experimental results section, we provide exhaustive simulation results for our experiments for three types of fill algorithms:

standard (traditional), staggered and 2-pass. We show how much inaccuracy we would have observed, had we used approximations such as merged fills or grounded fills.

II. PREVIOUS WORK

[1] has proposed a field solver which can take into account floating fills by using floating fill conditions in the direct boundary element equations. [2] has proposed an extraction method, where fills are eliminated one by one using a graph-based random walk algorithm while updating the coupling capacitances. [3] has shown that inter-layer coupling can be more important than intra-layer coupling. [4] has analyzed the impact of intra-layer fills on capacitances. [5] has provided design guidelines to reduce coupling. [6] has provided fill patterns to reduce interconnect coupling. [7] has presented an exhaustive method to generate capacitance tables for fills. [8] has presented a charge-based capacitance measurement method to analyze the impact of fills. [9] has analyzed the impacts of fills using an effective permittivity model. There is still a need for public algorithms for analyzing fills, generating efficient DOE's and incorporating the resultant data into extraction. In this paper, we try to achieve this and provide practical methods and parameterized DOE's for any design house or foundry to use on their technology to understand, analyze and characterize the impact of fills in their flow.

III. MOTIVATION

Current extraction tools have known inaccuracies for inclusion of floating fill impact on final coupling and total capacitances.¹ Most tools use simplifications to account for effects of fills. Below, we present simplifications used by extraction tools. Along with each simplification, we also underline how much error can be introduced for a typical structure.

Assuming Floating Fills as Grounded: Some extractors assume that the floating fills are grounded. These extractors use the same capacitance tables, which are also used to extract the regular interconnect capacitances. This assumption introduces results in up to 2x and 10x underestimation for first and second neighboring layer coupling capacitances, respectively, as well as almost eliminating the intra-layer coupling capacitances.

Merging the Fills: A popular method is to merge all the neighboring fills within a layer into one large fill. This results in up to 23x average overestimation of the intra-layer for small

¹The type of fill of interest to this paper is floating fill, since grounded fills are not versatile due to routing and increased total capacitances, extraction is not a concern to current extraction tools.

keep-off distances and underestimation of second neighboring-layer coupling capacitances up to 4x depending on the fill algorithm. First neighboring-layer coupling capacitance can be over or underestimated up to 2x. Another extension of this assumption is accounting for fill density only. Some extraction tools take density of fills as input to their models. In this case, different fill patterns yielding the same density are assumed to yield the same results. However, different patterns yielding the same fill density are known to yield different coupling capacitances.

Other Inaccuracies for Floating Fill Consideration of Extraction Tools: Another important inaccuracy is related to first and second neighboring inter-layer coupling, i.e., coupling between layers M and $M + 1$, and between $M - 1$ and $M + 1$, respectively. Patterns on M and $M + 1$ impact the coupling between the interconnects in these layers. As fills on layers M are introduced, the coupling between interconnects on layers $M - 1$ and $M + 1$ are impacted according to the pattern in M . So, assumptions such as merged or grounded fills will result in inaccuracies.

IV. METHODOLOGY

Current extraction tools do not contain accurate design of experiments for floating fills, although the DOE's for regular interconnects are sufficient. We provide an extensive DOE set for the floating fills. Our proposed method consists of a parameterized field solver DOE and normalization of results to enable a normalization-based extraction methodology for fills. To compare against the traditional flow, the traditional flow is presented in Figure 1. Essentially, after interconnects are designed and fills are automatically or manually inserted into the design, the extraction tool is run over the layout. As the extraction tools use one of the methods analyzed in the previous section, the results will not be much accurate.

The proposed flow, on the other hand, is illustrated in Figure 2. According to the proposed flow, the results are normalized to include the impact of fills. Furthermore, this flow makes it possible to compare impact of different fill algorithms using results of the same extraction for interconnects with no fills in between. Essentially, we propose to run an extraction tool over the interconnects with no fills first. This step is accurately handled by the current extraction tools. Then, using the fill DOE, we propose to update the impact of fills on coupling and total capacitances using a normalization step. The normalization is done with respect to the same structure and interconnect parameters without any fills in between interconnects. The capacitances with the fills are normalized with respect to capacitances without the fills. This results in normalized values close to and higher than 1, whenever the capacitance increases due to fills. The normalized couplings are all expected to be larger than 1, as fills increase coupling. The normalized data in the capacitance tables are then used to convert the result of extraction with no fills to accurate results accounting for the presence of floating fills. We use accurate 3D field solutions for our DOE and hence the results will be much more accurate than known approximations.

V. FILL DOE'S

Basic DOE structure: In this section, we propose our parame-

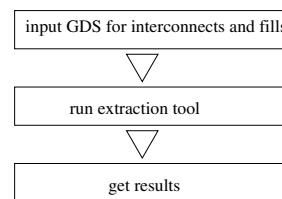


Fig. 1. Traditional flow

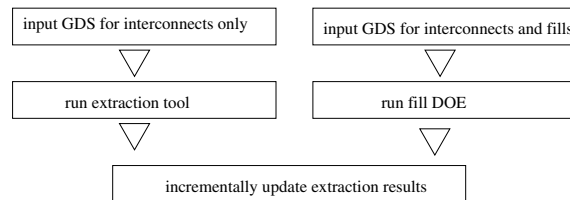


Fig. 2. Proposed flow to incorporate floating fill impact

terized DOE's. These DOE's can both be used for analysis and characterization of a process, as well as generating capacitance tables.

In order to reduce the run-time to a manageable amount, we have designed one structure for all DOE's, as shown in Figure 3, except the parallel neighboring layers DOE, which uses a version where interconnects are parallel in each layer instead of orthogonal. We propose a 5-layer structure, with top and bottom plates grounded. Each layer consists of two parallel interconnects facing each other. Parallel interconnects rotated 90 degrees to each other are used in layers $M - 1$, M and $M + 1$. Here, layer M refers to the layer in the middle. In layers $M - 1$, M and $M + 1$, two parallel interconnects are present, with fills in between placed according to parameters and a selected fill algorithm, the end results of which may look like the ones in Figure 1 of [3], i.e., standard, staggered, 2-pass, etc. Layers $M + 1$ and $M - 1$ include orthogonally oriented interconnects with respect to layer M . Interconnects on layers $M - 1$ and $M + 1$ overlap with each other, though an additional parameter can be used to introduce shifting of the overlapped interconnects. The simulated structures are parameterized according to the particular fill pattern (algorithm) of interest.

In the figure, interconnects on layer M are drawn vertically, whereas interconnects on layer $M + 1$ or $M - 1$ are drawn horizontally as dark rectangles. We have included in the simulation window, indicated by dashed lines, half width of each interconnect to account for the Neumann boundary conditions. These boundary conditions enable the mirroring of each structure along the dashed lines. Hence, essentially part of a large regular pattern is simulated.^{2,3}

The DOE structure is able to provide all the coupling capacitances of interest. For intra-layer coupling, capacitances between lines on layer M are used in the proposed structure. For neighboring-layer coupling, capacitances between one line

²While implementing the DOE structures, interconnect lengths are selected long enough to enable a repetitive pattern according to Neumann boundaries. The given parameters otherwise define the simulation structure unambiguously.

³While constructing the fill tables, the capacitances, are normalized with respect to the interconnect length if the coupling is between parallel interconnects. If orthogonal, we have recorded the capacitance without nor-

on layer M and $M + 1$ each are used in the proposed structure. For second neighboring-layer coupling, capacitances between lines on layers $M + 1$ and $M - 1$ are used in the proposed structure. For neighboring layer parallel line capacitances, the structure has been modified such that there are two parallel lines on neighboring three layers.

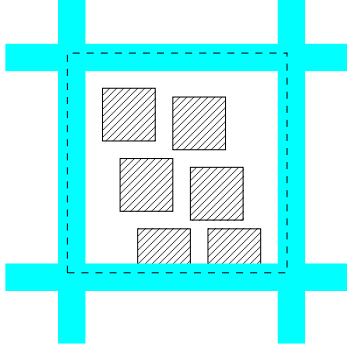


Fig. 3. **Basic DOE structure.** The structure consists of 5 layers. Top and bottom are ground planes. Three layers consist of parallel interconnects orthogonal to others across each layer. The structure enables observation of intra-layer, first and second neighboring layer couplings in one simulation.

A. Basic Fill Algorithm for Intra-Layer Coupling

Basic fill DOE algorithm is given below. Assuming there are four parameters of interest, the algorithm looks like the following:

1. **foreach** $w_f = w_f^{min} : w_f^{inc} : w_f^{max}$ {
2. **foreach** $w_s = w_s^{min} : w_s^{inc} : w_s^{max}$ {
3. **foreach** $c_f = c_f^{min} : c_f^{inc} : c_f^{max}$ {
4. **foreach** $w_m = w_m^{min} : w_m^{inc} : w_m^{max}$ {
5. *Run field solver over parameterized structure*
6. *and add result to a table}}}}}*

In this algorithm, w_f and w_s refer to fill width and spacing between fills, respectively. c_f is the number of fill columns between two parallel interconnects for each of the layers $M - 1$, M and $M + 1$.⁴ w_m refers to metal width. w_f^{inc} corresponds to the increment and is equal to $(w_f^{max} - w_f^{min}) / (\text{num. of data points})$. Usually, four data points is sufficient to come up with reasonable data tables or compact models. *min* and *max* for the fill parameters refer to the minimum and maximum values for a parameter, which usually can be decided using the design manual.

The proposed fill DOE uses 3D field solutions, and hence is accurate. The DOE above is given for a standard regular rectangular pattern. If a different fill algorithm is used, it may require different parameters as shown later in the paper.

In order to enable updating the coupling and total capacitances of interconnects with fills added, the fill capacitance models need to be normalized with respect to the same configuration including no fills. Hence, the same DOE structures are run with no fills present between the interconnects and the results with fills are normalized with respect to the results without fills. During extraction, when interconnects are seen

⁴An asymmetric DOE, where each layer could consist of different parameters, would be impractical in terms of simulation time. These kinds of asymmetries are secondary effects. If these effects need to be included, a statistical DOE needs to be considered.

in design, coupling capacitances between interconnects are multiplied with the normalized DOE results.

The run-time complexity of the algorithm is a function of the number of parameters and number of data points for each parameter. So, it is highly recommended to look for ways to reduce these. Herein, we provide a couple of guidelines. If a relationship between a parameter and the impact is known to be linear, then only two data points for that parameter should be selected, for example. Certain parameters change at the same time as other parameters. For example, dielectric height changes with the dielectric constant. These kinds of parameters need to be tied to each other so that only one loop is executed for both. If sensitivity of coupling to a parameter is known to be low, then this parameter can be thrown out by setting it to a constant. Similar to field solver setups with current extraction tools, a careful selection at this step will be highly rewarding in terms of run-time.

B. Fill DOE for Neighboring Layer

There are two types of inter-layer couplings. The first one is first neighboring layer coupling. For an interconnect on layer M , neighboring layer refers to interconnects on layers $M - 1$ and $M + 1$. On the other hand, second neighboring layer refers to coupling between interconnect on layer $M + 1$ and interconnects on layers $M - 1$. Neighboring coupling is mainly of fringing type, whereas second neighboring coupling is of area overlap type, as the interconnects surfaces face each other.

Neighboring layer interconnects are most of the time orthogonal to each other to reduce coupling. A cross-over structure in 3D simulation yields exact coupling between the interconnects. However, the addition of fills around the interconnects increases this coupling.

There are two extreme cases for the location of these fills. For worst-case coupling, the fill can be overlapping the next layer interconnect from top view. This situation is shown in Figure 4(b). In the figure, the shaded rectangles are the fills on layer M . The least coupling occurs when the fills on layer M are shifted. This is shown in Figure 4(a).⁵

Similarly, fills on layers $M + 1$ or $M - 1$ also have worst- and best-case coupling positions. This is illustrated in Figure 5(a) and (b). In this figure, this time, fills on layers $M + 1$ or $M - 1$ are shown as shaded from a top view.

The corresponding DOE consists of evaluating all incremental configurations between these worst and best cases for neighboring layers. Hence, one parameter is added to evaluate the fill shifts.

With respect to the original defined DOE, we can change the DOE by adding the following line.

5. **foreach** $shiftM = shiftM^{min} : shiftM^{inc} : shiftM^{max}$ {

Here, $shiftM$ is short for the amount of shift for layer M fills.

C. Fill DOE for Parallel Neighboring-Layer Coupling

It is possible that two consecutive layers have parallel lines. This condition is especially possible in lower layers as well

⁵The shifting will impact coupling even with staggered fill especially if fill widths are large.

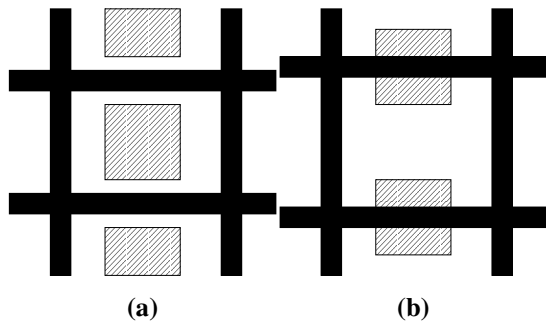


Fig. 4. **Inter-layer coupling for neighboring layers.** (a) Fills on layer M intersect minimally with interconnects on layers $M-1$ and $M+1$. (b) Fills on layer M shifted and intersect maximally with interconnects on layers $M-1$ and $M+1$.

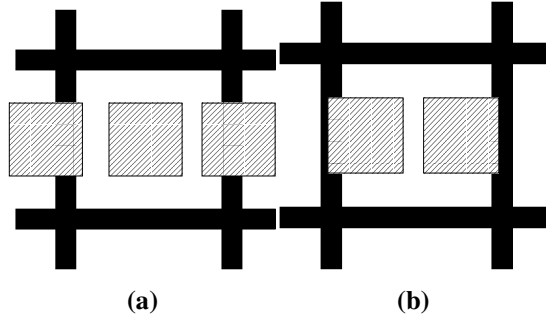


Fig. 5. **Inter-layer coupling for neighboring layers.** (a) Fills on layer $M+1$ intersect maximally with fills on layer M . (b) Fills on layer $M+1$ shifted and intersect minimally with interconnects on layers M .

as layers close to clock networks. In order to handle such a configuration, we have used a modified simulation structure as described above and illustrated in Figure 6 from a side view. Worst- and best-case shifts again need to be implemented. The same DOE algorithm presented in the previous section is used with the pattern in Figure 6.

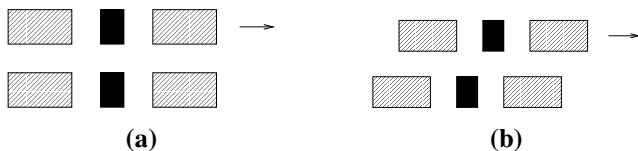


Fig. 6. **Inter-layer coupling for parallel neighboring lines.** (a) Layer M and $M+1$ interconnects intersect. (b) Layer $M+1$ shifted.

D. Fill DOE for Second Neighboring Layer Coupling

To analyze the layer M fill impact on $M-1$ and $M+1$ coupling capacitances, the structure shown in Figure 7 should be used. Practically, we have used the same structure from Figure 4 to reduce the number of simulations and hence handle both DOE's in one simulation. Similar to the previous DOE, positions for fills for best- and worst-case couplings should be identified.⁶ Also, lines in $M-1$ and $M+1$ may not be overlapping. To account for these shifts, $M+1$ lines should be shifted up to half the minimum spacing allowed between two interconnects as shown in Figure 8 from a side view. In our DOE's, we have only shifted the fills.

E. Implementation of Other Fill Patterns

The proposed DOE can be extended to other common fill patterns, such as staggered, two-pass or alternating rectangles.

⁶For staggered patterns, these shifts are only important for line lengths on the order of the fill width.

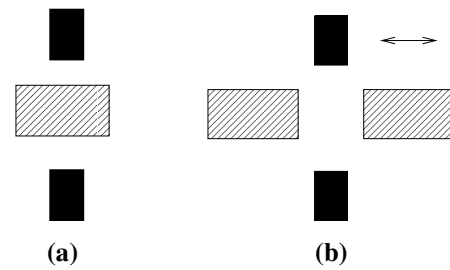


Fig. 7. **Inter-layer coupling for second neighboring layers.** (a) Fills on layer M intersect maximally with interconnects on layers $M-1$ and $M+1$. (b) Fills on layer M shifted and intersect minimally with interconnects on layers $M-1$ and $M+1$.

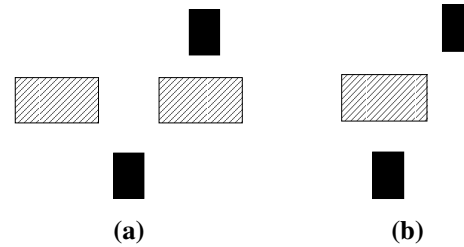


Fig. 8. **Inter-layer coupling for second neighboring layers.** (a) Layer M interconnect shifted to simulate for non-overlapping interconnects. (b) Fills on layer M and layer $M+1$ interconnect shifted.

In this section, we briefly describe how we have implemented the DOE for staggered and two-pass methods.

Staggered Fill Algorithm. Staggered fill algorithm produces a shape similar to the standard fill algorithm, except each row and column is *staggered* by a fixed amount.

Two-Pass Algorithm. Two or three-pass algorithms insert rectangles of two or three different sizes. Largest rectangles are inserted first, and are placed in the middle of two interconnects to reduce first neighboring layer coupling. Smaller fills are then inserted in the following steps.

VI. EXTENSIONS FOR KEEP-OFF RULE AND CMP IMPACTS

A. On the Keep-Off Design Rule

One of the design rules most relevant to floating fills is the keep-off, or exclusion, distance. This distance is defined as the minimum distance that a fill must be away from an interconnect. In this section, we provide some intuition about this design rule.

This design rule is usually selected such that the coupling capacitance to an intra-layer neighbor is negligible as compared to the total capacitance of a line. We have conducted an experiment on a layer with the values in Table I. We have changed the keep-off distance from $0.1\mu m$ to $0.9\mu m$ and observed the change in coupling capacitance over the total capacitance. This plot is shown in Figure 9.

The coupling over the total capacitance is crudely negligible (3%) around $0.5\mu m$, hence $0.5\mu m$ is likely to be selected as the keep-off distance for the layer for which this experiment has been conducted. As the fills are allowed to be closer to interconnects, corresponding to a lower keep-off distance, the coupling increases.

Having a large keep-off distance, although advantageous in terms of reducing intra-layer coupling, has other issues. It becomes difficult to insert fills into certain regions to

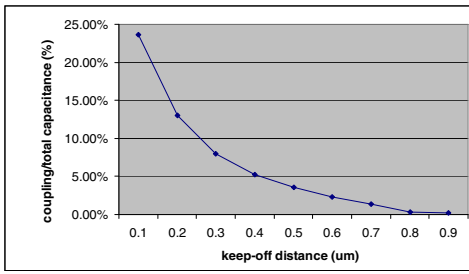


Fig. 9. Intra-layer impact of keep-off distance

TABLE I

PARAMETERS USED IN KEEP-OFF DISTANCE EXPERIMENTS

metal height	dielectric height	dielectric constant	
$0.3\mu m$	$0.3\mu m$	3.1	
keep-off distance	metal width	fill spacing	fill width
$0.1-0.9\mu m$	$0.1\mu m$	$0.1\mu m$	$0.5\mu m$

density constraint, as the distance between two parallel interconnects has to be larger than two times the keep-off distance. Consequently, CMP results in more variations. A second issue is increased coupling of interconnects to neighboring layers. As keep-off distance is increased, less electric flux is present between interconnects of the same layer. However, this flux is directed to interconnects on neighboring layers.

It is possible to have an edge over the design rule if accurate extraction is available. Historically, design rules appear before any analysis and optimization technique. Similar examples have been seen in lithography. With aggressive technologies, there is an unavoidable need to be able to analyze the effects of each interaction. In the context of the keep-off design rule, as accurate extraction has not been possible, the solution has been to restrict the proximity of fills to interconnects.

With the basic building blocks of an accurate extraction flow we are presenting in this paper, it will become possible to accurately analyze the impact of reduced keep-off distances on coupling and total capacitances as well. This will permit greater flexibility of fill algorithms in regions where coupling between lines is not critical. Reducing the keep-off distance enables tighter metal density uniformity, as well as reduced inter-layer coupling capacitances.

B. Incorporation of CMP Impacts

CMP is known to result in copper height and hence dielectric height variations. CMP models exist which give metal heights in a tile within a layer. It is then necessary to tie these heights to the final capacitance values. We have run a set of experiments to evaluate the effect of height variations on the coupling and total capacitances. The results are shown in Figure 10. The x axis gives the multiplication factor we have used for the height. Values on the y axis are normalized coupling capacitances. We have observed a linear relationship between height and both coupling and total capacitances. The implication is, by just running simulations for two different heights followed by linear interpolation or extrapolation; one can find the CMP-impacted capacitance. To incorporate the CMP impact, we have used two different heights per each simulation.

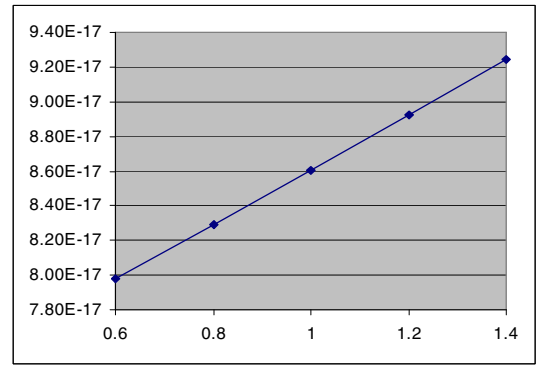


Fig. 10. CMP-induced height impact on coupling capacitance shows linear change.

VII. EXPERIMENTAL RESULTS: DOE ANALYSES

Using the proposed DOE, we provide an analysis of relationships we have observed. We have used three different fill algorithms. For each algorithm, we have repeated the simulations for merged fills and grounded assumptions for comparison. We have also simulated the structures with no fills for normalization. Each simulation takes between 10 to 120 seconds, depending on the selected parameter, and all the DOE's take roughly 24 hours to 48 hours on a 2.4GHz quad-core server with 2GB of memory using 3D field-solver Raphael. We have used a minimum grid size of 100,000 nodes per each structure. We have used up to 10 licenses and 5 machines to further reduce the simulation time. We have parameterized the standard fill algorithm using the values shown in Table II. Here, dielectric constant, metal and dielectric heights, changed at the same time, enable simulation of local, medium and global interconnects in the back-end stack. Parameter names prepended with a sign (star or plus) are changed at the same time to reduce the number of simulations as described above.

A. Analysis of Intra-Layer Coupling DOE for Standard Fills

Figures 11 and 12 show the intra-layer coupling capacitance as a function of fill width and spacing, respectively, for three different numbers of fill columns. We can observe that as fill width increases or fill spacing decreases, intra-layer coupling increases. The increase is more pronounced if there are more columns.

B. Analysis of First Neighboring Inter-Layer Coupling

To illustrate how much the shift can impact the coupling, we have used the representation as shown in Figure 13. In the figure, each sample corresponds to a set of six simulations, where the shift parameter is changed from 0 to 1 in increments of 0.2. These numbers are multiplicative constants, which are multiplied by half the pitch. 125 samples are shown, corresponding to 750 field solver simulations. The corresponding sample is computed as follows:

$$s_I = \max(v_i) / \min(v_j) - 1 : \forall v_{i,j} \in v_I \quad (1)$$

Here, I is a set of six experiments where the shift parameter is changed while keeping other parameters fixed; s

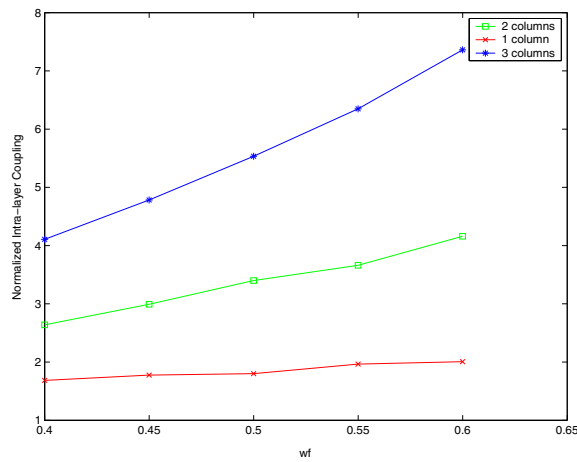


Fig. 11. Fill width dependency of intra-layer coupling for different number of fill columns.

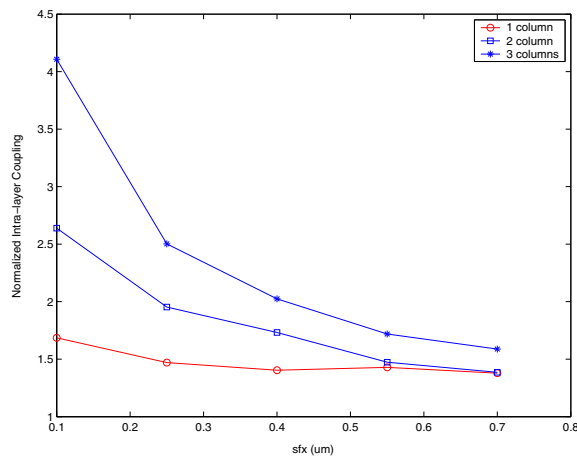


Fig. 12. Fill spacing dependency of intra-layer coupling for different number of fill columns.

corresponding sample value; and v_i and v_j are values of the experiments in set I . Essentially, the maximum over the minimum of the values of a set gives the maximal change due to the shift operation. A 1 is subtracted so that we can see the change more clearly when plotted. The y -axis values give the maximal change directly.

In Figure 13, we can see that the maximum of all the samples is 0.05, which corresponds to a 5% change due to the shift of fills on layer M only. We can say that this amount is negligible, considering the fact that we have used an almost best-case choice of $300nm$ keep-off distance for this plot. The data set with largest impact corresponds to fill width, fill spacing and metal widths of $0.6\mu m$, $0.4\mu m$ and $0.4\mu m$, respectively, in our technology.

C. Analysis of First Neighboring-Layer Parallel Line Coupling

A similar analysis has shown that the maximum of all the samples corresponds to 2.8% change due to parallel shifts of both interconnect and fills on layer $M+1$. We can say that this amount is negligible, considering the fact that we have used an almost best-case choice of $300nm$ keep-off distance. The data set with largest impact corresponds to fill width, fill spacing and metal widths of $0.4\mu m$, $0.55\mu m$ and $0.2\mu m$, respectively.

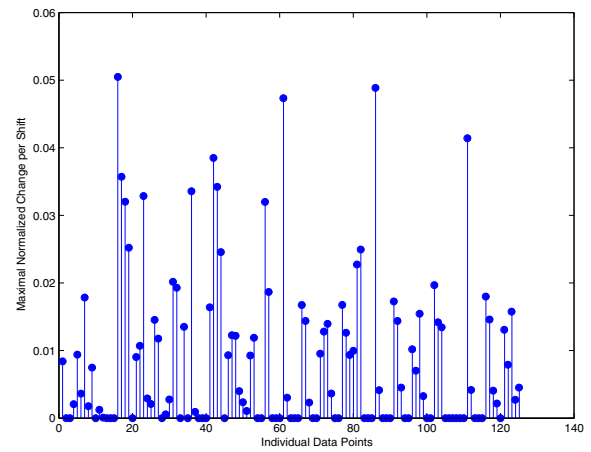


Fig. 13. Normalized Data showing maximal change in coupling of neighboring lines.

Figure 14 plots, for various interconnect widths, the neighboring layer coupling as a function of the shift parameter for this DOE. For small shifts, there is negligible impact. As shift is increased, field lines between interconnects on neighboring layers are blocked by a larger fill, which increases the coupling.

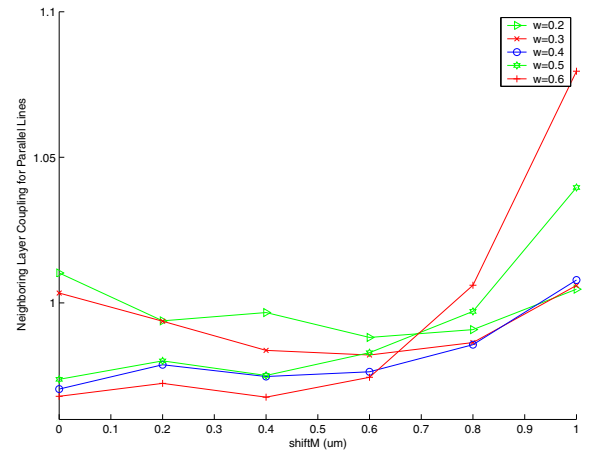


Fig. 14. Neighboring-layer parallel line coupling dependency on amount of M layer shift for various metal widths.

D. Analysis of Second Neighboring Inter-Layer Coupling

Figures 15 and 17 show fill shift dependency. In Figure 15, fill width and spacing are kept at $0.4\mu m$, which corresponds to around 25% density.⁷ At $shiftM = 0$, there is maximum overlap between interconnects of layers $M-1$ and $M+1$, and up to 1.55 times the coupling is seen with respect to no fills. Shifting the layer M fills by changing the $shiftM$ parameter reduces the coupling significantly. When fill width is small, there is not much change due to the shift of fills, as field lines between larger interconnects on layers $M+1$ and $M-1$ can find a direct path without going through the fills. In Figure 17, fill spacing is changed. Fill and metal widths are kept at $0.4\mu m$ and $0.2\mu m$, respectively. When the spacing between fills is small, the change in coupling due to the shift in layer M fills is negligible. On the other hand, increasing the spacing between fills (decreasing the metal density from 65% down to

⁷Exact density depends on the window in which the density is ρ

25%) on layer M results in a 35% change, which is significant and needs to be modeled.

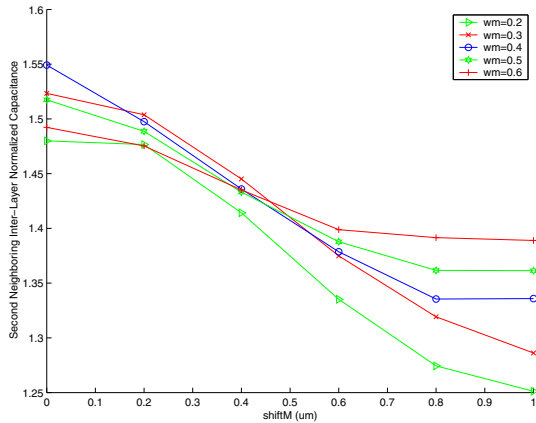


Fig. 15. Fill shift dependency of second neighboring layer coupling for different metal widths

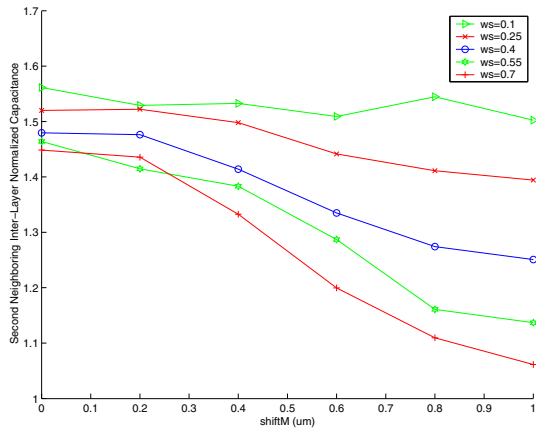


Fig. 16. Fill shift dependency of second neighboring layer coupling for different fill to fill spacings.

E. Analysis of Other Fill Patterns

We have parameterized the staggered fill algorithm using the variables in Table III. We have parameterized the 2-pass algorithm using the variables in Table IV. The two-pass ratio parameter is used to define the larger fill width in this algorithm with respect to the narrower width, which is inserted in the second step.

TABLE II
PARAMETERS FOR STANDARD FILL ALGORITHM

metal width	0.1, 0.2, 0.3, 0.4 (μm)
fill width	0.4, 0.45, 0.5, 0.55 (μm)
fill spacing	0.1, 0.25, 0.4, 0.55 (μm)
fill shift	0.25, 0.5, 0.75, 1 (x)
metal height*	0.3, 0.4 (μm)
dielectric height*	0.3, 0.4 (μm)
dielectric constant*	3.1, 2.8
number of fill columns	1, 2, 3
keepoff distance	0.3, 0.5, 0.7 (μm)

TABLE III
PARAMETERS FOR STAGGERED ALGORITHM

metal width	0.1, 0.2, 0.3, 0.4 (μm)
fill width+	0.4, 0.5, 0.55 (μm)
stagger amount+	0.2, 0.25, 0.275 (μm)
fill spacing	0.1, 0.25, 0.55 (μm)
fill shift	0.25, 0.5, 0.75, 1 (x)
metal height*	0.3, 0.4 (μm)
dielectric height*	0.3, 0.4 (μm)
dielectric constant*	3.1, 2.8
number of fill columns	2, 3, 4
keepoff distance	0.3, 0.5, 0.7 (μm)

TABLE IV
PARAMETERS FOR TWO-PASS ALGORITHM

metal width	0.1, 0.2, 0.3, 0.4 (μm)
fill width	0.4, 0.45, 0.4, 0.55 (μm)
fill spacing	0.1, 0.25, 0.4, 0.55 (μm)
fill shift	0.25, 0.5, 0.75, 1 (x)
metal height*	0.3, 0.4 (μm)
dielectric height*	0.3, 0.4 (μm)
dielectric constant*	3.1, 2.8
two pass ratio	2, 3
keepoff distance	0.3, 0.5, 0.7 (μm)

F. Comparison of DOE Results

Results for DOE, merged fill and grounded fill as metal width is changed are shown in Figure ?? for a particular subset of the 2-pass algorithm. DOE results sit in between the merged and grounded fill results. Grounded fills are almost negligible. Merged fills result in an overestimation, which is much more than this particular plot on the average. We next analyze this overestimation in detail.

Table V contains a summary of all the simulations for standard, staggered and 2-pass algorithms. In order to compare the proposed results, we have repeated the field solver simulations for the merged and grounded fills in addition to the proposed DOE. For merged fills, all same-layer neighboring fills are lumped into a single, using the convex hull of the fills. For the grounded fills, the same fill pattern as the DOE is used, except each floating fill is connected to ground. In the table, the columns from left to right are the means of normalized DOE, merged and grounded fill results. These columns indicate the normalized increase in coupling capacitances due to fills. The normalization is with respect to the original interconnect structure with no fills. The last two columns indicate the magnitude of each coupling term is as a percentage of the

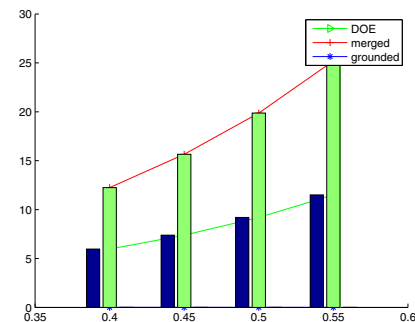


Fig. 17. Increase in coupling for DOE, merged and grounded range of metal widths.

TABLE V
COMPARISON OF DOE, MERGED AND GROUNDED EXTRACTION FOR STANDARD, STAGGERED AND 2-PASS ALGORITHMS

STANDARD	DOE	Merged	Grounded	Max. Coupling/Total	Min. Coupling/Total
intra-layer	2.377	10.336	0.002	15.91%	0%
first-layer	1.083	1.123	0.492	22.25%	17.11%
second-layer	1.126	0.726	0.094	6.84%	2.38%
STAGGERED	DOE	Merged	Grounded	Max. Coupling/Total	Min. Coupling/Total
intra-layer	2.579	25.9308	0.0021	23.33%	0%
first-layer	1.131	1.155	0.578	20%	16.32%
second-layer	1.153	0.559	0.107	6.870%	0%
2-PASS	DOE	Merged	Grounded	Max. Coupling/Total	Min. Coupling/Total
intra-layer	5.308	34.607	5.998e-6	3.607%	0.909%
first-layer	1.110	0.531	0.546	19.562%	15.913%
second-layer	1.0160	0.284	0.147	7.776%	3.566%

total capacitance.⁸ We have included both the maximum and minimum for this ratio. This ratio shows the importance of the given coupling capacitance.

The rows of Table V show intra-layer, first layer neighboring and second layer neighboring coupling, respectively, for each fill algorithm. Using the data from the 2-pass algorithm as an example, looking at the last two columns, we can say that the intra-layer coupling shows less impact as compared to second-layer and first layer couplings. In terms of accuracy, we can see that, the increase in intra-layer coupling due to fills can be 13.73 times greater using merged fill as compared to the DOE results, whereas this ratio can be almost negligible for the grounded fills.⁹ The DOE results are closer to “actual results” than are to the outputs of approximate methods such as merged fill or grounded fill. Merged fills result in an overestimation of coupling capacitances, whereas grounded fills result in a significant underestimation. Although overestimation could be thought of as advantageous, there are two reasons why it is not an advantage. The first reason is that the overestimation is significantly high. The second reason is that, as we observe the next two rows, we see that the overestimation for the intra-layer coupling has resulted in an underestimation for both first and second neighboring layer couplings due to the fact that merged fills attract most of the flux which would otherwise go to the interconnects on the neighboring layers. Observing the first-layer coupling row, although we would expect an increase in coupling capacitances due to the insertion of fills, we see a reduction for the merged and grounded fills as indicated by normalized values lower than 1. This happens due to the flux reasoning above. Considering the fact that these coupling capacitances are large portions of the total capacitance, inaccuracies will be highly important. Standard and staggered algorithms also have shown similar inaccuracies, especially for the intra-layer and second-layer couplings. As the proposed DOE uses accurate field solutions which take into consideration the pattern shapes and parameters, the results will be highly accurate with respect to known approximations. The run-time is kept reasonably low using the proposed guidelines.

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⁸Default settings for most extractors is to neglect coupling capacitances below 1%.

⁹Some of the high increase is due to allowing small keep-off distances, which can be helpful in achieving high density fills.

ing of the problems the industry faces to incorporate fills in extraction flows, and which helped us to direct this work to concisely target these problems.

IX. CONCLUSIONS

We have proposed a DOE set for extraction tools to generate normalize fill tables which can be used on top of existing extraction tools for accurate extraction of capacitances in the presence of floating fills. We have provided the parameterized design of experiments, which each design or mask house can implement in their flow to analyze and extract capacitances in the presence of fills. This field solver DOE set will complete the DOE set that comes with the extractors, which is not optimal for floating fills. We have shown that the proposed field solver-based DOE's provide significant accuracy improvements over methods and assumptions used by current extraction tools. We believe that this work will enable a better overall analysis and extraction possibility of the impact of fills on capacitances in interconnect technologies with the help of its extensive and parameterized nature.

REFERENCES

- [1] W. Yu, M. Zhang and Z. Wang, *Efficient 3-D extraction of interconnect capacitance considering floating metal fills with boundary element method*, Tran. on CAD of IC and Systems, Vol. 25, No. 1, Jan, 2006, pp. 12 - 18.
- [2] S. Batterywala, R. Ananthakrishna, Y. Luo and A. Gyure, *A statistical method for fast and accurate capacitance extraction in the presence of floating dummy fills*, VLSI Design, 2006.
- [3] A. Kurokawa, T. Kanamoto, A. Kasebe, Y. Inoue and H. Masuda, *Efficient capacitance extraction method for interconnects with dummy fills*, CICC, 2004, pp. 485-488.
- [4] Keun-Ho Lee, Jin-Kyu Park, Young-Nam Yoon, Dai-Hyun Jung, Jai-Pil Shin, Young-Kwan Park and Jeong-Taek Kong; *Analyzing the effects of floating dummy-fills: from feature scale analysis to full-chip RC extraction*, IEDM, 2001, pp. 31.3.1-31.3.4.
- [5] A. B. Kahng, K. Samadi and P. Sharma, *Study of Floating Fill Impact on Interconnect Capacitance*, ISQED, 2006, pp. 691 - 696.
- [6] A. Kurokawa, T. Kanamoto, T. Ibe, A. Kasebe, C.W. Fong, T. Kage, Y. Inoue and H. Masuda, *Dummy filling methods for reducing interconnect capacitance and number of fills*, ISQED 2005, pp. 586-591.
- [7] J.-K. Park, K.-H. Lee, J.-H. Lee, Y.-K. Park and J.-T. Kong, *An exhaustive method for characterizing the interconnect capacitance considering the floating dummy-fills by employing an efficient field solving algorithm*, SISPAD 2000, pp. 98-101.
- [8] Y.W. Chang, H.W. Chang, T.C. Lu, Y. King, W. Ting, J. Ku and C.Y. Lu, *A novel BCM method free from charge injection induced errors: investigation into the impact of floating dummy-fills on interconnect capacitance*, Int. Conf. on Microelectronic Test Structures 2005, pp. 235-238.
- [9] W.-S. Lee, K.-H. Lee, J.-K. Park, T.-K. Kim, Y.-K. Park and J.-T. Kong, *Investigation of the capacitance deviation due to metal-fills and the effective interconnect geometry modeling*, ISQED 2004, pp. 373-376.