Fill for Shallow Trench Isolation CMP

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ABSTRACT

Shallow trench isolation (STI) is the mainstream CMOS isolation technology. It uses chemical mechanical planarization (CMP) to remove excess of deposited oxide and attain a planar surface for successive process steps. Despite advances in STI CMP technology, pattern dependencies cause large post-CMP topography variation that can result in functional and parametric yield loss. Fill insertion is used to reduce pattern variation and consequently decrease post-CMP topography variation. Traditional fill insertion is rule-based and is used with reverse etchback to attain desired planarization quality. Due to extra costs associated with reverse etchback, "single-step" STI CMP in which fill insertion suffices is desirable.

To alleviate the failures caused by imperfect CMP, we focus on two objectives for fill insertion: oxide density variation minimization and nitride density maximization. A linear programming based optimization is used to calculate oxide densities that minimize oxide density variation. Next a fill insertion methodology is presented that attains the calculated oxide density while maximizing the nitride density. Averaged over the two large testcases, the oxide density variation is reduced by 63% and minimum nitride density is increased by 79% compared to tiling-based fill insertion. To assess post-CMP planarization, we run CMP simulation on the layout filled with our approach and find the planarization window (time window in which polishing can be stopped) to increase by 17% and maximum final step height (maximum difference in post-CMP oxide thickness) to decrease by 9%.

1. INTRODUCTION

Shallow trench isolation (STI) is the mainstream CMOS isolation technique used in all designs today. In STI trenches are created in Silicon substrate and filled with Silicon Dioxide (oxide) around devices or groups of devices that need to be isolated. Advanced STI processes involve many process steps of which nitride deposition, oxide deposition, and chemical-mechanical polishing (CMP) are of interest. Nitride is deposited over active regions to protect the underlying Silicon and to act as polish stop. In areas outside the active regions, trenches are created and void-free oxide is deposited over the wafer by chemical vapor deposition (CVD). Chemical mechanical polishing (CMP) is used to remove the excess oxide over the nitride and in the trenches to ensure a planar surface for successive process steps.

CMP is the planarization technique of choice and is used extensively in IC fabrication processes for metal layers and for STI. In CMP for STI, deposited oxide is removed until all oxide over nitride regions is removed. Unfortunately, due to high pattern dependency CMP is imperfect and, depending on the underlying patterns, can result in functional and parametric yield loss. The pattern densities of both the deposited oxide and the underlying nitride determine the planarization quality after CMP. Because oxide is deposited over nitride, oxide density is dependent on the shapes of the underlying nitride features as explained in the next section. Therefore the density and the shapes of the nitride features determines the planarization quality. Traditionally, planarity imperfections have been addressed by reverse etchback and by fill insertion. In reverse etchback, a second mask is created to etch away oxide in regions of high-oxide density prior to CMP, resulting in a more uniform oxide density. Unfortunately, an extra mask and additional process steps are required for reverse etchback and it is economically desirable to avoid reverse etchback. Fill insertion is another technique to control oxide and nitride densities. Fill insertion for STI CMP involves addition of dummy nitride features to increase the nitride and, through it, the oxide density.

Typically rule-based fill insertion is performed by shape-based tools such as Mentor Calibre. Dummy rectangles are tiled with a predefined size, spacing, and keep-off distance from the design's features. Often this approach is used to control only the nitride density along with reverse etchback which controls the oxide density. Beckage et al. proposed a model-based fill insertion methodology that uses CMP simulation, an area of active research [10, 3, 7], to identify regions for fill insertion [2]. Their approach uses two types of fill "tiles": (1) tiles that contribute to the nitride density but negligibly to the oxide density, and (2) tiles that contribute to both, oxide and nitride densities. Post-CMP topography simulation is then used to drive the insertion of these tiles in the layout. Topography simulation is based on complex models and determination of the oxide and nitride densities for the desired topography is complicated. Unfortunately, details are not provided by the authors. Also, due to the use of specific fill configurations (tiles), the flexibility to control densities is limited. In this paper, we propose a fill insertion methodology that targets oxide density variation minimization and nitride density maximization. These two objectives help alleviate the failures caused by CMP imperfections as discussed later.

We first apply a linear programming-based optimization that was previously proposed for back-end of the line (BEOL) CMP [6] to calculate target oxide densities that minimize the oxide density variation. With the target oxide densities determined, fill insertion is performed to maximize nitride density. We insert fill wherever per-

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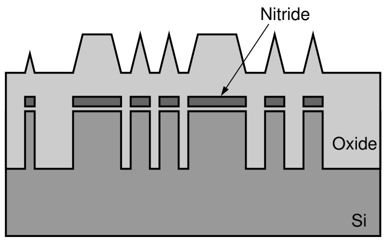

Figure 1: Profile before CMP. Oxide is deposited with slanted sidewalls over nitride features.

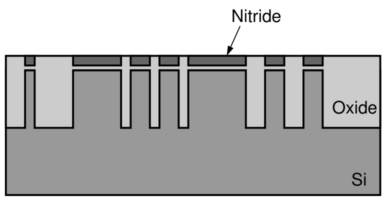

Figure 2: Desired profile after CMP. Oxide should be completely cleared over nitride, no nitride should erode, and no oxide dishing should occur in the trenches.

mitted by the design rules and then remove it on-demand to meet the target oxide density. An algorithm is developed to attain the target oxide density by removing the minimum amount of fill (so that nitride density is maximized). We evaluate the proposed approach on two large testcases. Compared to the unfilled layout and layout with fill tiling, we observe substantial reduction in oxide density variation and enhancement in nitride density. Further, we run CMP simulation to predict the post-CMP topography. We find the topography achieved for the layout in which fill insertion is performed with the proposed methodology to have superior characteristics. We also hypothesize that stress due to STI reduces when fill is inserted with the proposed approach.

The remainder of this paper is organized as follows. In the next section we present a background on CMP for STI. Section 3 describes motivations and objectives of fill insertion. Sections 4 and 5 give problem formulations for STI fill insertion. Section 6 presents our experimental study. Conclusions and future work are drawn in Section 7.

2. BACKGROUND

The basic STI process steps are as follows. First oxide, known as pad oxide, followed by nitride is deposited over the wafer. Then the deposited nitride is patterned and allowed to remain only over the active (or diffusion) regions. Everywhere else trenches are etched into the silicon and then oxide deposited by CVD over the wafer. Though the oxide is deposited to fill the trenches, it also deposits over the nitride features and is called *overburden* oxide. Figure 1 shows a cross-section after these steps.

CMP is used to planarize the surface for successive process steps. Figure 2 shows the desired cross-section after CMP. In reality, however, such a planar cross-section is not attained. Imperfect planarization can result to three key failure mechanisms shown in Figure 3 [4]. First, if the oxide over *all* nitride regions is not completely cleared then subsequent stripping of nitride will be prevented leading to device failure. Second, excessive polishing causes nitride erosion which leads to lowered isolation edge and consequently poor device characteristics. Excessive nitride erosion can cause stripping of underlying silicon and device failure. Third, oxide in larger trenches dishes due to pad-bending causing poor isolation.

The primary requirements of CMP are: (1) complete removal of oxide over all nitride regions, and (2) no stripping of silicon under the nitride. These two requirements determine the *planarization window*, which is time interval from the instant when all oxide over nitride just gets removed to the instant when silicon at any location is touched by the pad. Planarization can only be stopped at a time instant in the planarization window and it is desirable to have a large planarization to accommodate for variations. In addition, oxide dishing and nitride erosion must be minimized for improved device characteristics.

In STI CMP post-planarization topography is affected by the density of the overburden oxide that is polished and that of the underlying nitride. Interestingly, because oxide is deposited over nitride, oxide density is dependent on the underlying nitride features. For high density plasma (HDP) oxide deposition, which is the mainstream oxide deposition technology, the deposition profile exhibits a slanted sidewall. Consequently, features on the oxide layer appear as *shrunk* nitride features [9, 3, 10]. Specifically, a nitride polygon is shrunk or sized down by a fixed amount (denoted by α) on each side to get the oxide polygon deposited over it. For example, nitride squares smaller than 2α on a side do not appear on the oxide layer while squares of side 5α appear as squares of side 3α on the oxide. We note that shrinkage by α on all sides is a convenient approximation and accounts for sidewall slant and pad bending effects. Shrinkage allows us to control oxide and nitride densities independently up to some extent.

Fill insertion is performed by inserting features on the nitride layer to control densities of oxide and nitride layers. Design rules such as minimum nitride width and area, maximum nitride width, minimum nitride spacing and notch, and minimum enclosed area by nitride must be followed in fill insertion. Inserted fill is always separated by the minimum nitride-to-nitride spacing from all design features. So even after fill insertion there is a trench to isolate the design features ensuring negligible electrical impact of the inserted fill. Since there are no contacts with the inserted fill no stray devices, that can potentially act as parasitics, are formed. Moreover, no diffusion may be done over the fill features. Fill insertion can potentially affect stress induced due to STI. Stress affects device characteristics because of its impact on carrier mobility and is modeled, at least in part, in today's device models (e.g., BSIM v4.4.0) [1]. Recently STI fill insertion was noted to improve predictability of stress-induced effects and therefore reduce guardbanding [8].

3. MOTIVATIONS AND OBJECTIVES OF FILL INSERTION

In this section we present the motivation behind fill insertion when STI technique is used for CMOS isolation and formulate the objectives of fill insertion.

Fill insertion is used to attain a more uniform density and consequently reduce the topography variations after CMP which is patter dependent. The primary goal of fill insertion is to maximally reduce causes for three key manufacturing failures due to imperfect CMP – failure to clear oxide on top of nitride, nitride erosion, and oxide dishing (see Figure 3. The secondary goal of fill insertion is to control STI-induced stress, a significant component of which is unmodeled and due to the size of STI wells. With fill insertion, the size of STI wells around devices can be made consistent to increase the accuracy of device performance and power estimates.

Failure to clear oxide is the primary cause of CMP failure. It occurs in regions where oxide density is substantially higher than average. Therefore oxide density variation must be minimized. Reduction of oxide density variation is also beneficial for reduction of another type of CMP failure. Since more oxide over nitride can be cleared simultaneously, the size of the planarization window can be increased which results in reduction of nitride erosion.

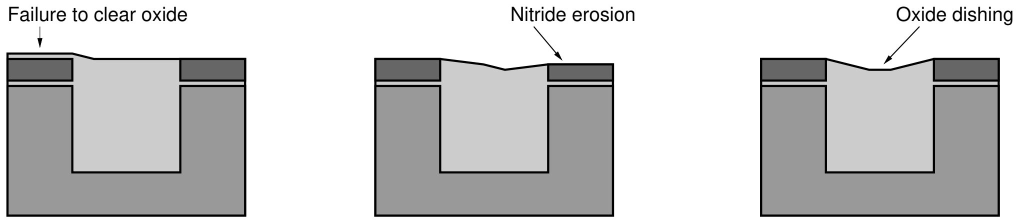

Figure 3: **Three key failure mechanisms caused by imperfect CMP.**

Oxide dishing and nitride erosion can be greatly reduced by increasing nitride density. Indeed, higher nitride density results in smaller trenches and, therefore reduces oxide dishing. The mechanism of reduction of nitride erosion is based on the fact that nitride is significantly harder than oxide. When polishing pad reaches nitride level, it should detect increased load on the driving motor and stop. Obviously, higher nitride density makes the detection of the nitride level more accurate.

STI stress is due to: (1) size of diffusion regions, and (2) size of the STI well isolating the diffusion region. Stress due to diffusion size are already included in today's SPICE models. However, stress due to STI well size are not yet modeled and can be a significant source of variation [8]. Typical power/performance characterization considers wells of smallest or largest size for the best- and worst-case estimates. When nitride density is higher, then devices get smaller STI wells around them which reduces the difference between these estimates which makes their power/performance more predictable.

The above analysis leads to the following two objectives for fill insertion in order of their priority:

1. Minimize oxide density variation
2. Maximize nitride density

The corresponding bi-criteria problem formulation is described in the next section. In Section 5, this problem is transformed into the problem of nitride density maximization subject to upper bound on oxide target density.

4. BI-CRITERIA FORMULATION AND OPTIMIZATION FOR FILL INSERTION

Given:

- set of rectilinear nitride regions contributed by the devices in the design;
- parameter α by which nitride features shrink on each side to give oxide features; and
- design rules: minimum nitride width, maximum nitride width, minimum nitride space and notch, minimum nitride area, minimum enclosed area by nitride.

Find:

- locations for fill insertion.

Such that:

1. oxide density variation is minimized; and
2. nitride density is maximized.

The above bi-criteria formulation has clear prevalence of the first objective over the second. Therefore, we first address the primary objective: oxide density variation minimization and afterwards maximize nitride density such the first objective is not affected.

Formally, *density variation* is defined as the maximum difference in densities computed over fixed-sized windows of the layout [6]. Figure 4 shows overlapping windows over which density is computed. Tile size is the distance by which the windows are offset from each other. The *fill synthesis* problem for minimum density variation can be formulated as follows:

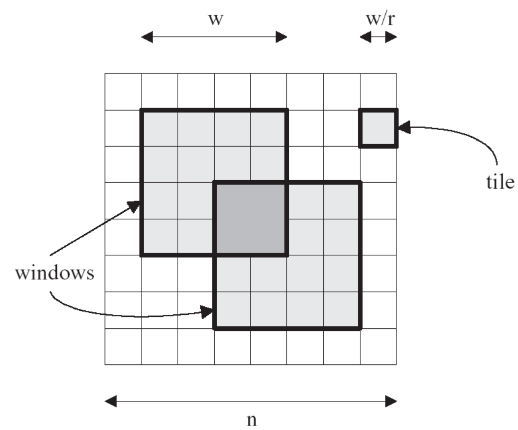

Figure 4: **Layout is partitioned into windows of fixed size $w \times w$ and density is computed over them. Density variation is the maximum difference between densities computed over any two windows.**

Given:

- *Fill slack*, s_i, the maximum amount of fill that can be inserted in Tile i, without any DRC violations.
- *Window size*, r, as a multiple of tile size, over which density is computed.

Find:

- *Target fill*, t_i, the amount of fill to be inserted in Tile i.

Such that:

- Density variation is minimized.

The fill slack for the STI technique is equal to the maximum oxide density contributed by fill insertion. We observe that the maximum contribution is made by maximum fill insertion on the nitride layer (i.e., insert fill wherever possible). The *maximum fill region*, the union of all regions where fill can be inserted subject to DRC constraints, is denoted by $Nitride_{max}$ (density = $|Nitride_{max}|$).

The procedure for finding the region $Nitride_{max}$ is illustrated on Figure 5. The nitride regions contributed by the devices in the design are shown in Figure 5(a). First, to obey the minimum spacing design rule, the features are bloated by the minimum spacing. Minimum spacing design rule-correct fill may be inserted in the remaining regions (Figure 5(b)). Next, to obey the minimum nitride width and area rules, regions that are too small are removed (Figure 5(c)). $Nitride_{max}$ is the region available for fill insertion after these two steps.

Maximum oxide density contribution is found by shrinking $Nitride_{max}$ by α on all sides. We use $|Oxide_{max}|$ to denote the oxide density due to $Nitride_{max}$ and it is highest oxide density achievable by fill insertion.

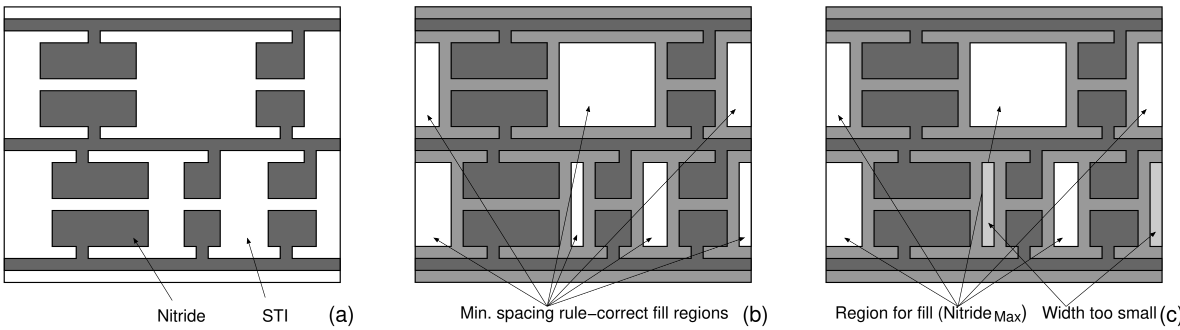

Figure 5: Computation of maximum fill region ($Nitride_{max}$). (a) Unfilled layout. (b) Design features bloated by minimum spacing design rule. (c) Spaces of small width and area (illustrated in the lightest shade of gray) are not available for fill.

We use the linear programming based solution proposed in [6] to solve the fill synthesis for minimum density variation problem. Other approaches such as Monte-Carlo methods based, greedy, and hybrid approaches can also be used [5]. These solutions find the target oxide density per tile.

5. NITRIDE MAXIMIZATION FORMULATION AND OPTIMIZATION

The bi-criteria problem statement can be transformed into the followings:

Given:

- set of rectilinear nitride regions contributed by the devices in the design;
- parameter α by which nitride features are shrunk on each side to give oxide features; and
- design rules: minimum nitride width, maximum nitride width, minimum nitride space and notch, minimum nitride area, minimum enclosed area by nitride.
- *target oxide density per tile*

Find:

- locations for fill insertion

Such that:

1. nitride density is maximized.

Proposed Solution

We first consider the following two important limit cases of $|Oxide_{target}|$:

1. $|Oxide_{target}| = |Oxide_{max}|$
2. $|Oxide_{target}| = 0$

Case $|Oxide_{target}| = |Oxide_{max}|$. This is the trivial case. Fill is inserted at $Nitride_{max}$ to attain oxide density of $|Oxide_{max}|$ and nitride density of $|Nitride_{max}|$. We note that the maximum nitride size design rule is typically over $100\mu m$ which is significantly larger than typical lengths of polygons in $Nitride_{max}$. Therefore, we ignore the maximum nitride size design rule for computing $Nitride_{max}$; any DRC violations are fixed post-fill.

Case $|Oxide_{target}| = 0$. We note that due to the nature of the problem, there is no need to increase the oxide density of most tiles and this case is very frequent. For this case, nitride fill features that do not contribute to the oxide density must be inserted. Fill rectangles that have one side smaller than 2α do not contribute to the oxide density due to shrinkage by α on each side. Unfortunately, rectangular fill features are suboptimal in offering the highest nitride density. To have zero oxide density, all points on inserted fill shapes must be within a distance α from the nearest edge of the shape. We first insert fill at $Nitride_{max}$ and then *dig* holes of minimum size in the fill to ensure all points on fill are within a distance α from the nearest edge, i.e., no density is contributed to oxide.

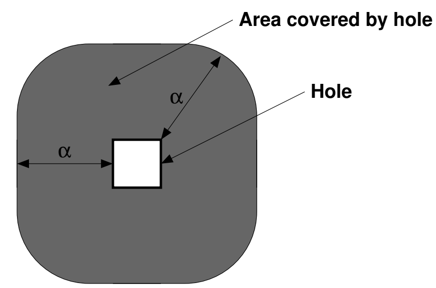

Figure 6: Gray area is the *area covered* by the white hole, i.e., fill features added in the gray area do not contribute to the oxide density due to the hole. α is the shrinkage; oxide features can be computed from nitride features by shrinking by α on all sides.

LEMMA 1. *Fill at $Nitride_{max}$ with rectangular holes of minimum combined area, such that (1) all points on fill are within a distance α from an edge, and (2) hole size is no smaller than that permissable by DRCs, offers the highest nitride density with zero oxide density.*

Proof. Due to shrinkage by α on each side, no point on the nitride contributes to the oxide density. The oxide contribution is therefore zero. All rectilinear nitride fill configurations can be realized with fill at $Nitride_{max}$ with rectangular holes. Minimization of hole area is equivalent to nitride density maximization. □

We refer to the area on nitride that is within a distance α of a hole as the *area covered* by the hole. Area covered by a hole does not contribute to the oxide density.

LEMMA 2. *Highest area is covered per unit hole area by holes that are square in shape and of the smallest size permissable by DRCs.*

Proof. Figure 6 shows a hole and the area covered by it. The area covered by a hole of size $a \times b$ is $\pi\alpha^2 + 2a\alpha + 2b\alpha$. The ratio of area covered and the hole size is $(\pi\alpha^2 + 2a\alpha + 2b\alpha)/(ab)$ and is the highest for the square hole of the smallest size. □

Lemmas 1 and 2 suggest the following strategy: (1) insert maximum fill in the entire region $Nitride_{max}$ and (2) dig the minimum number of smallest-sized squared holes in this region. The smallest size of squared holes is determined by the minimum diffusion-diffusion spacing rule and/or the minimum diffusion notch rule.

We denote the minimum hole size by β. For zero oxide contribution we must ensure that the entire $Nitrdie_{max}$ region is covered with the rounded squares. In addition, the overlap between rounded squares should be minimized to require the minimum number of holes. The problem is essentially the known *covering* problem in computational geometry.

Unfortunately rounded squares are difficult to handle in covering and must be simplified to a shape that is more amenable to the covering problem. Triangles, rectangles and hexagons are such shapes. Several other polygons such as pentagons, heptagons, and octagons require substantial overlap for covering. The simplified polygon must be completely inscribable in the rounded square and then covering done with the simplified polygon. Due to this simplification, not all area offered by the rounded square will be used for covering. The area of the rounded square that is outside the inscribed simplified polygon is referred to as the *inloss*. Figure 7 shows an inscribed hexagon and the associated inloss. We wish to use the polygon that offers the minimum inloss. Triangles, clearly, have a larger inloss in comparison to rectangles and hexagons. We use hexagons, that are similar to regular hexagons but allow two parallel edges to be of different lengths than other four, for covering. We refer to such hexagons as *parallelohexagons* because opposite edges are parallel. Parallelohexagons are more flexible than regular hexagons and can be used for covering. Parallelohexagons are flexible enough to be reduced into rectangles so covering with parallelohexagons is better than with rectangles.

We now calculate the best parallelohexagon given a rounded square of parameters α and β. As the rounded square is symmetrical about X- and Y- axes, only the orientation in Figure 7 and those generated by it after up to 45^o of rotation need to be evaluated. If may be shown that the smallest inloss is attained in the orientation of Figure 7 and when one vertex of the parallelohexagon is on the top edge of the rounded square and another on the bottom. The area of the parallelohexagon, the X-coordinate of the two rightmost vertices is x, is denoted by $A(x)$.

$$A(x) = \frac{1}{2}\left[x\sqrt{\alpha^2-(x-\beta/2)^2}+\alpha x+\beta x\right]$$

$$\begin{aligned}\frac{dA(x)}{dx} &= \frac{1}{2}\left[\sqrt{\alpha^2-(x-\beta/2)^2}+\frac{x(x-\beta/2)}{\sqrt{\alpha^2-(x-\beta/2)^2}}+\beta+\alpha\right]\\ &= \frac{1}{2\sqrt{\alpha^2-(x-\beta/2)^2}}\left[\alpha^2+\frac{1}{2}\beta x-\frac{1}{4}\beta^2\right]+\frac{1}{2}(\alpha+\beta)\end{aligned}$$

¿From the derivative it is clear that the parallelohexagon area increases with x. Therefore the parallelohexagon with the minimum inloss has all its vertices on the rounded square. The corresponding inloss is given by $\{\alpha\beta+(\pi-2)\alpha\}/\{\beta^2+4\alpha\beta+\pi\alpha^2\}$ and is under 10% for typical values of α and β.

We consider two orientations of the parallelohexagon within the rounded square that are likely to have small inloss. The first orientation is show in Figure 7 and the second has the parallelohexagon rotated by 45^o. All other orientations are equivalent due to symmetry of the rounded square about X- and Y-axes or have a higher inloss.

Covering rectilinear regions with parallelohexagons. We now present our algorithm to cover $Nitride_{max}$ which is rectilinear in shape with parallelohexagons that represent the area covered by holes. We overlay a honeycomb structure which is a tessellation of parallelohexagons on the rectilinear polygon such that minimum number of hexagons are required in the honeycomb. A honeycomb overlay that completely covers the rectilinear polygon and requires

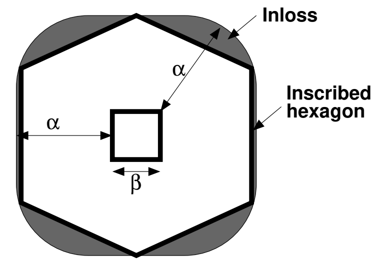

Figure 7: **Hexagon inscribed in a rounded square and the associated inloss (shown in Gray). β is the minimum hole size permitted by the design rules.**

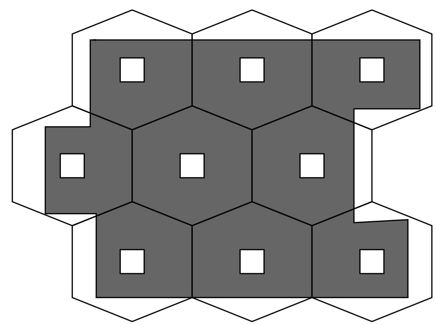

Figure 8: **Gray rectilinear polygon represents $Nitride_{max}$. Transparent hexagons are tessellated in a honeycomb to cover the polygon with minimum number of hexagons. Holes created in $Nitride_{max}$ at the center of the hexagons (shown in White) ensure zero oxide density contribution due to $Nitride_{max}$.**

the minimum number of hexagons is referred to as an *optimal* overlay. To propose an algorithm for minimum overlay, we develop the following terminology. As shown in Figure 9(a), we define V-segments, HL-segments, and HU-segments of a rectilinear polygon as its vertical edges, horizontal edges which have the polygon over them, and horizontal edges which have the polygon under them. Figure 9(b) shows V-segments, HL-segments, and HU-segments of a honeycomb structure.

THEOREM 1. *In an optimal overlay:*

- *at least one V-segment of the honeycomb must align horizontally with corresponding segment from the rectilinear polygon; and,*
- *at least one HL- or HU-segment of the honeycomb must align vertically with corresponding segment from the rectilinear polygon.*

Proof. Given an optimal overlay, the honeycomb can be perturbed to horizontally align *one* V-segment of the honeycomb with that of the rectilinear polygon, and vertically align *one* of HL- or HU-segment of the honeycomb with that of the rectilinear polygon, without requiring any additional hexagons to cover. Hence, there is an optimal overlay for which at least one V-segment of the honeycomb is horizontally aligned with corresponding from the rectilinear polygon, and at least one HL- or HU-segment of the honeycomb is vertically aligned with corresponding from the rectilinear polygon. Hence proved. □

Our algorithm to find the optimal overlay is as follows. Select one V-segment and one HL- (HU-) segment of the honeycomb, and one V-segment and one HL- (HU-) segment of the honeycomb. Horizontally align the V-segments and vertically align the HL- (HU-) segment to fix the position of the honeycomb over the rectilinear polygon. Count the number of hexagons required to cover the

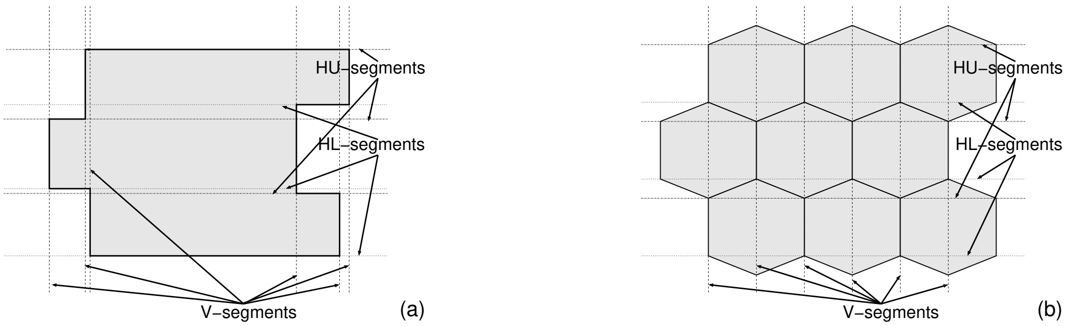

Figure 9: Illustration of V- (vertical), HL- (lower horizontal), and HU- (upper horizontal) segments for a (a) rectilinear polygon, and (b) honeycomb.

polygon. Iterate over all combinations of V- and HL- (HU-) segments to find the one with minimum number of hexagons. To evaluate overlays in which the honeycomb is rotated by 90^o, the polygon is rotated by 90^o and algorithm repeated. We do not consider other orientations of the honeycomb since only axes-aligned holes can be created. The complexity of the algorithm is $|PolygonV - segments| \times (|PolygonHL - segments| + |PolygonHU - segments|) \times |Polygonarea|$. Where, $|PolygonV - segments|$, $|PolygonHL - segments|$, $|PolygonHU - segments|$, and $|Polygonarea|$ are the number of V-segments, number of HL-segments, number of HU-segments, and area of the polygon.

General Case. $0 < |Oxide_{target}| < |Oxide_{max}|$. Due to the nature of the linear programming solution [6], tiles which require density increase get an $|Oxide_{target}| = |Oxide_{max}|$ and this case is very infrequent. As in the previous subsection, we first perform fill insertion in $Nitride_{max}$ and then create holes of the minimum size since they offer high nitride density with zero or small oxide density. Area covered by holes, which is rounded square in shape, is approximated by parallelohexagons. However, unlike the previous subsection, it is not necessary to cover the rectilinear polygon with hexagons. To ensure coverage in the previous subsection, rounded squares were approximated with *inscribed* parallelohexagons which caused the rounded square area outside the parallelohexagon to overlap and therefore required more holes. Since covering the polygon is no longer necessary, we approximate rounded squares with *circumscribed* parallelohexagons. Packing the polygon with such parallelohexagons ensures no overlap between covers of two holes and requires fewer holes. Unlike the previous subsection, each parallelohexagon contributes to the oxide density in the regions that lie outside the rounded square but inside the parallelohexagon. We use the parallelohexagon of the smallest area so that its oxide density contribution is small; oxide density can easily be increased by not creating holes as described later. With an iterative program, we have found the smallest parallelohexagon to be under 8.9% larger than the rounded square (Figure 10. We refer to the ratio of the contributed oxide area to the parallelohexagon area as *outloss*. I.e., $outloss = (area_{hexagon} - area_{roundedsquare})/area_{hexagon}$. Depending on the outloss, we now consider two cases:

1. $|Nitride_{max}| \times Outloss \leq |Oxide_{target}|$.
   I.e., if $Nitride_{max}$ was packed with the circumscribed hexagons, resultant oxide density would be less than $|Oxide_{target}|$. We use the parallelohexagon covering algorithm proposed in the previous subsection to overlay a honeycomb over a rectilinear polygon. Hexagons are then removed from the honeycomb, in decreasing order of their area outside the polygon, until oxide density = $|Oxide_{target}$.

2. $|Nitride_{max}| \times Outloss > |Oxide_{target}|$

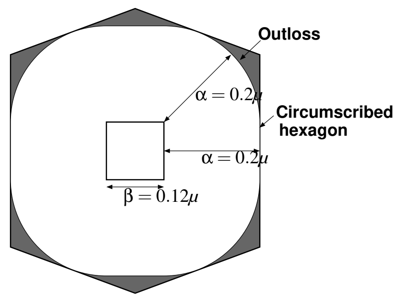

Figure 10: Smallest hexagon circumscribed around the rounded square. Gray area represent the outloss.

We partition the rectilinear polygon into two rectilinear polygons such that the area of the first, $A_1 = |Oxide_{target}|/Outloss$. In the first polygon, circumscribed hexagons are overlayed using the covering algorithm in the previous section. In the second polygon, which requires zero oxide density is needed, we use solution of the $|Oxide_{target}| = 0$ case.

6. EXPERIMENTAL STUDY

We now describe our empirical validation of the proposed methodology. In the experiments we start with the design layout and insert fill with rule-based tiling and with the proposed approach. Comparisons are then performed between: (1) the original layout, (2) layout after tiling-based fill insertion, and (3) layout after fill insertion performed with the proposed methodology. Our comparison studies are of two types: (1) analysis of oxide and nitride densities, and (2) assessment of the post-CMP topography as predicted by a CMP simulator.

For the experiments, we create two large designs by assembling smaller cores. Commercial EDA tools with Artisan TSMC 90*nm* libraries and layouts are used for synthesis and placement of these circuits. Since interconnects do not affect nitride and trench regions, no routing was performed. We keep the utilization ratio between 60% and 70% which is typical. The first testcase, *mixed*, is composed of a RISC processor, a JPEG compressor, and AES and DES3 encryption cores. The design contains static memory and 756K cells, and measures $2mm \times 2mm$. The second design, *OpenRisc8*, is composed of eight RISC processor cores, contains static memory and 423K cells, and measures $2.8mm \times 3mm$.

Figure 11 shows a small section of *OpenRisc8*. Figure 11(a) is the unfilled layout with nitride in the shaded rectilinear regions and trenches everywhere else. The same section after tiling-based fill insertion (fill size = 0.5μ, fill spacing = 0.5μ) performed with *Mentor Calibre v9.3_5.9* is shown in Figure 11(b). Fill regions are illustrated in gray. In Figure 11(c) the same section with fill insertion performed with the proposed methodology is shown. As is evident, nitride density is substantially higher with the proposed fill approach. Holes created in fill regions to control the oxide density are also visible.

Analysis of Nitride and Oxide Densities

The proposed methodology is driven by oxide and nitride density objectives that largely determine post-CMP planarity. Our two objectives of our approach are oxide density variation minimization and nitride density maximization. Table 1 presents the maximum oxide density variation, minimum nitride density, and average nitride density. In all our experiments, density is computed over overlapping square windows of side 160μ; the offset between successive windows is 40μ. For tiling-based fill insertion, we consider three fill-width/fill-spacing combinations: $0.5\mu/0.5\mu$, $1.0\mu/0.5\mu$, and $1.0\mu/1.0\mu$. It is clear that fill insertion with the proposed approach significantly decreases the oxide density variation and increase the nitride density. Compared to $0.5\mu/0.5\mu$ tiling-based fill, oxide density variation reduces by 63% and minimum nitride density increases by 79% when averaged over the two testcases. We also observe that tiling-based fill may increase the oxide density variation requiring costly etchback process steps to reduce it.

Post-CMP Topography Assessment

The density results show that the proposed approach achieves its objectives well. However, the real goal of fill insertion is improved post-CMP planarity so it is important to assess that. We use the STI CMP simulator developed and calibrated by MIT's MTL group [7, 10] to predict post-CMP topography. Typical values are used for the initial structure and CMP model parameters such as planarization length, pad bending, slurry selectivity, etc. We study the two primary characteristics of CMP quality - planarization window and final step height. Planarization window is the time window in which polishing may be stopped. If polishing is stopped earlier, oxide does not clear up completely from over nitride. If polishing is stopped later, underlying silicon is stripped. Both these effects can lead to device failure. It is desirable to have a large planarization window to accommodate for variations. Final step height is the difference in oxide thickness after CMP and is used to quantify oxide dishing. Large final step height leads to poor device characteristics such as excessive leakage and parasitics. Table 2 presents the planarization window and maximum final step height predictions from the CMP simulator for the unfilled layout, the layout with tiling-based fill, and layout with fill inserted using the proposed methodology. Compared to tiling-based fill, we observe a 17% increase in planarization length and a 9% decrease in maximum final step height on average over the two testcases.

Figure 12 presents the final step height maps for the the unfilled layout, layout with tiling-based fill, and layout with fill inserted by the proposed methodology. We assume CMP to stop at the middle of the planarization window. The final step height is lower all over the chip when fill is inserted by our approach.:

7. CONCLUSIONS

In this paper we presented a new methodology for fill insertion to improve STI planarity after CMP. To alleviate the failures caused by imperfect CMP, our approach minimizes oxide density variation and maximizes nitride density. We leverage on the fact that the density of oxide, which is deposited over nitride, depends on the underlying nitride shapes due to deposition bias. We first insert maximal fill subject to the design rules and then create holes in it to control the oxide density. Oxide density for minimum density variation is computed with a liner programming-based solution and then nitride is maximized with the computed oxide density as a constraint. To maximize the nitride density we minimize the number of holes that need to be created. Towards this, regions that not contribute to oxide density due to the presence of a hole are approximated by hexagons and an algorithm is proposed to cover the nitride area with the hexagons efficiently.

Experimental results indicate substantial reduction in oxide density variation and increase in nitride density in comparison to traditional tiling-based fill insertion. We also study the post-CMP topography predicted by a CMP simulator for two layouts when fill insertion is done with the proposed method and with traditional tiling-based method. We find the topography of the layouts with our fill insertion to be significantly more desirable than obtained by traditional tiling-based fill. Specifically, the planarization window increases by 17% and maximum final step height decreases by 9%.

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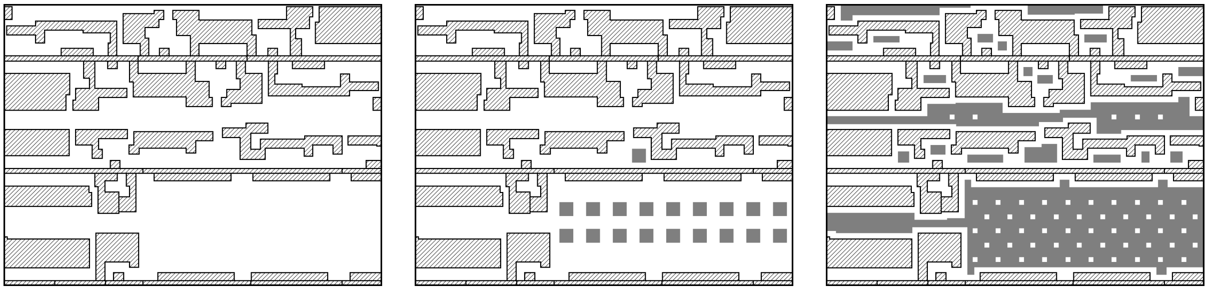

Figure 11: **Layout with fill inserted using tiling-based method and with the proposed method. Unfilled layout, layout with tile-based fill inserted, and layout with fill inserted with the proposed method are shown. Fill is shown in gray and the shaded regions represent nitride due to CMOS devices (i.e., diffusion regions).**

Testcase	Fill Approach	Oxide Density Variation	Min. Nitride Density	Average Nitride Density
Mixed	Unfilled	11.13%	21.47%	27.56%
	Tiled $0.5\mu/0.5\mu$	11.25%	28.13%	31.89%
	Tiled $1.0\mu/0.5\mu$	12.91%	25.54%	31.25%
	Tiled $1.0\mu/1.0\mu$	12.05%	23.97%	29.59%
	Proposed	2.79%	57.20%	66.34%
OpenRisc8	Unfilled	9.93%	25.87%	36.05%
	Tiled $0.5\mu/0.5\mu$	9.74%	31.91%	38.25%
	Tiled $1.0\mu/0.5\mu$	9.52%	31.50%	38.30%
	Tiled $1.0\mu/1.0\mu$	9.51%	29.02%	37.33%
	Proposed	4.73%	49.61%	59.35%

Table 1: **Density improvements from the proposed fill insertion method. Oxide density variation, minimum nitride density, and average nitride density are compared for two testcases for the unfilled layout, layout with tiling-based fill for three fill-width and fill-spacing combinations, and layout with fill inserted using the proposed method.**

Testcase	Fill Approach	Planarization Window (s)	Max. Final Step Height (nm)
Mixed	Unfilled	45.3	142
	Tiled $0.5\mu/0.5\mu$	46.5	143
	Proposed	53.6	129
OpenRisc8	Unfilled	42.7	146
	Tiled $0.5\mu/0.5\mu$	44.7	144
	Proposed	50.4	133

Table 2: **CMP simulation results for unfilled layout, layout with tiling-based fill insertion, and layout with the proposed fill insertion method. Planarization window is the time window in which polishing can be stopped. Max. final step height is the maximum difference in oxide height after CMP.**

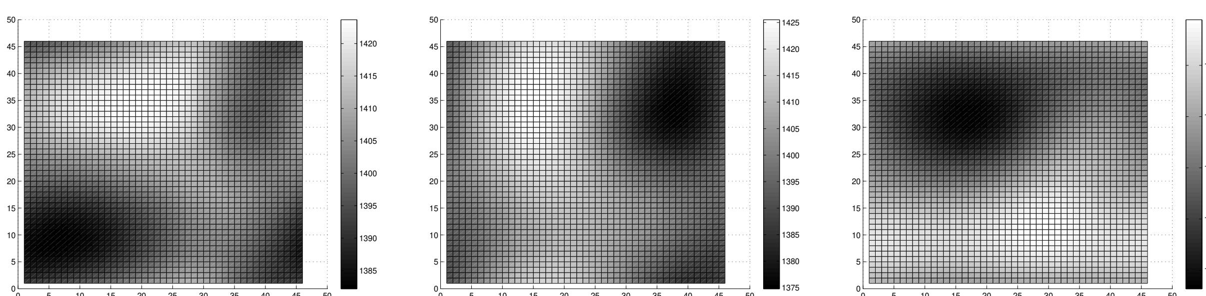

Figure 12: **Final step height maps for the unfilled layout, layout with tiling-based fill insertion, and layout with the proposed insertion method. The step height is in Angstrom.**