Interconnect Matching Design Rule Inferring and Optimization through Correlation Extraction

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Fig. 1. Two interconnects are nominally designed to have equal dimensions. As a results of process variations, they have mismatch.

Abstract— New back-end design for manufacturability rules have brought guarantee rules for interconnect matching. These rules indicate a certain capacitance matching guarantee given spacing between interconnects and interconnect area. Yet, the number of these rules is so few that they are of limited value in circuit or interconnect optimization. A method to infer additional guarantees from the provided guarantees is necessary so that optimization can be optimal. In this paper, we target two problems. First, we present a methodology to infer additional matching guarantees through extracting correlation information from the given limited set of matching guarantees in the design manual. In order to achieve this, we propose a multi-function variant of multi-variate Newton-Raphson method to extract parameters of the proposed dimension- and distance-based process correlation model for interconnects. We propose to use the extracted correlation information to infer a continuum of matching rules through simulation with proposed modifications to the standard capacitance extraction procedure. Secondly, we show how to directly incorporate the inferred interconnect matching guarantees for accurate interconnect optimization in a flexible geometric programming construction. We show how much resource savings are possible through inferring of new matching rules. Applying the inferred mismatch guarantees allows a geometric programming-based H-tree optimization to reduce the clock tree resources 27% on average and up to 56%.

Index Terms— design guarantee inferring, correlation extraction, interconnect matching, H-tree optimization

I. INTRODUCTION

Increased interconnect delay and interconnect variability in sub-90nm technologies have resulted in consideration of including interconnect matching guarantees in design rule manuals. Process variations cause a mismatch between certain interconnects, which are nominally designed to be equal. This is illustrated in Figure 1. Initially, two or more interconnects might be designed for same width (w) and height (h), but due to process variations, the interconnects might end up having widths $w' \neq w''$ and heights $h' \neq h''$. The mismatch in physical dimensions causes a mismatch in electrical parameters, such as the capacitance or RC delay.

A set of matching guarantee rules has started to appear in design manuals. These rules are low in number, e.g. as low as one to four, and they provide guarantees given spacing and dimension combinations. These kind of design for manufacturability rules are usually not mandatory for DRC but only informative and suggestive, hence addition of new such rules will not conflict with any other design rule. Interconnect matching rules are provided for only certain fixed spacing and dimension combinations, although spacing between interconnects and interconnect dimensions can take a continuum of values. It is not economic for foundries to just increase the number of rules in design manuals, as each rule requires significant resources in terms of test chip area. It is highly desirable to find a way to *infer matching guarantees* for spacing and dimension combinations that are not given in the manual. This will help in better utilizing the resources for circuit optimization.
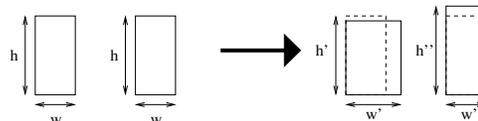
Inferring a continuum of interconnect matching guarantees can be beneficial to utilize design resources, such as area, efficiently through interconnect optimization. Inferring additional guarantees and integration of them into optimization, however, is not a straightforward process:

Problem 1: An extraction must first be applied to acquire the process variations that have led to the guarantees given in the manual.

The rules in the design rule manual (DRM) are measurement results, which have been acquired from actual test chips. The proposed method should try to go as lower as possible into the process information to infer new rules. A straightforward data interpolation or extrapolation is not possible in this respect. We should trace the matching rule back to its physical reasons. The proposed flow is illustrated in Figure 2. The left hand side in Figure 2 corresponds to the design rule generation in the foundry, whereas the proposed method is illustrated on the right hand side. The proposed method uses the provided design rules and tries to first infer the process model which has led to the original rules. Then, using suggested types of simulation, the proposed method infers new design rules.

Problem 2: Given a set of (original and inferred) mismatch guarantees, perform interconnect optimization that utilizes the mismatch guarantees as tightly as possible.

Problem 1 requires a correlation extraction method and a correlation model. We need to furthermore modify the standard capacitance extraction procedure to be able to account for mismatch. A means to *directly integrate* the design rule inferring with interconnect optimization is needed for Problem
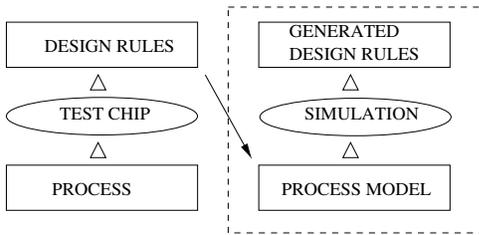
Fig. 2. The proposed method provides a way to extract process information and infer new rules.

Fig. 3. Matching Guarantee Space. Original interconnect matching rules given in the manual shown. For each region, Ri, a given matching percentage is guaranteed.

2. We have particularly focused on *resource utilization* in a clock tree optimization problem as clock trees may consume a large amount of resources and their branches need to be matched for low timing skew.

In this paper, given a set of limited interconnect matching guarantees; we propose a method to infer additional guarantees for spacings and dimensions not given in the DRM. We propose a multi-function variant of multi-variate Newton-Raphson optimization algorithm to optimize a correlation function. We modify the standard interconnect extraction scheme to account for interconnect mismatch. In this paper, the major contributions over what we have presented in [11] are:

- a detailed example of how inferred design rules compare to original rules
- seamless integration of the proposed design guarantee inferring technique into global clock H-tree optimization using geometrical programming constraints
- examination of resource utilization reduction through usage of the proposed matching guarantee inferring and interconnect optimization method with respect to the traditional approach

Optimization is an important step in VLSI CAD. Without the integration of rule inferring into an optimization scheme, the mismatch inferring itself has limited value. This makes the contribution in this paper very valuable, as provision of the integration of rule inferring into a practical optimization flow can show how much resource saving is possible.

In Section II, we start with a motivational example. After presenting the previous work in this area, we move on to introduce the modifications to standard extraction methods. In Section IV-A, we give an outline of the proposed flow. In this section, after introducing a correlation model, we show proposed extraction for mismatch in Section IV-D after a reminder for standard extraction in Section IV-C. Sections IV-E to IV-H are devoted to the implementation details of extraction for mismatch. Section V is assigned to the implementation of the proposed methods into interconnect optimization. We conclude the paper after an extensive experimental section in Section VI.

II. MOTIVATIONAL EXAMPLE

Let us try to illustrate the guarantee rules and guarantee inferring idea using Figure 3. Let the S axis in the figure be the spacing between matched interconnects and the A axis be the nominal cross-sectional area of one of the matched interconnects. We name such a space as the *matching-guarantee space*. Nominally, areas of the matching interconnects should
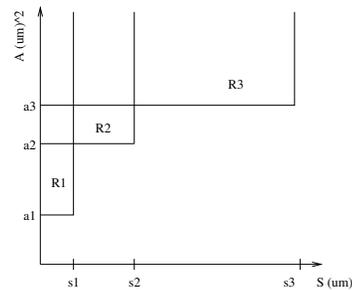
be same. Assume 3 rules are given in the design manual. Each rule defines a region in this plane. For example, rule i defines the region Ri, which is where $A > ai$ and $S < si$. Here, ai and si are constant values as given in the DRM. Each Ri is associated with a percent mismatch, say m_{Ri}. Rule i means that, if the matched interconnects have a nominal area larger than ai and if they are located at a spacing less than si, their total capacitances are guaranteed to match within m_{Ri} percent. Given these rules, if a new area and spacing combination is available in the design, a way to infer the corresponding matching guarantee is needed.

III. PREVIOUS WORK

Process variations on matched structures result in mismatch. For interconnects, this mismatch can show its effects on electrical parameters such as resistance, capacitance or delay, although the source of a mismatch is in the physical parameters like the dimensions of the interconnects and all the way into the process parameters. Mismatch has traditionally been a major problem for transistors. The most well known mismatch model in use today is Pelgrom's model [1] which states that increasing transistor area and decreasing the spacing between matched transistors decreases mismatch. In [2] mismatch is tied to physical reasons and models are formulated so that physical parameters instead of the resultant electrical parameters are used in the equations directly. This type of physics-based modeling is especially reasonable for interconnects as the relation to physical parameters is explicit.

Interconnect performance in the presence of process variations has been analyzed in a number of papers [24] [22] [20] [5] [4]. In [3] and [4] sensitivity analysis is used to relate delay to interconnect dimensions. As interconnect performance is projected to increasingly dominate the circuit delay, there is significant possibility for design constraint relaxation. [18] and [19] target crosstalk noise and RLC delay pessimism reduction, respectively. Techniques have been presented to account for process variations [23] [22] [21]. Capacitance extraction under process variations has been handled in [4]. Recently, [17] presented a post-silicon clock-tuning method.

Former clock optimization methods are based on tree-based clock optimization algorithms [12] [10] [8]. These algorithms did not consider layout resources and process variations in general. A good coverage of these initial work can be found in [9]. [14] has used Gauss-Marquardt optimization to optimize a clock-tree. [6] has used posynomial programming to optimize

wire widths. [13] has used convex optimization for general RC networks. However, these studies have not considered skew constraints due to process variations or simultaneous buffer sizing. Recently, [16] introduced temperature-aware clock tree optimization. [7] has used linear programming using Taylor expansions considering buffer and wire widths. However, linear programming can give local solutions and a direct link between process information from design rules and optimization constraints is not available in these works. Recently, process correlation extraction has been studied in [25].

IV. EXTRACTION OF PROCESS CORRELATION

A. Overview

We present the following algorithm to give an outline of the proposed flow:

Proposed Flow:
[1] Choose a correlation model.
[2] Use proposed optimization algorithm to extract the parameters of the correlation model, such that they are optimal for all given design rules.
[3] Simulate a range of spacing-dimension combinations using the correlation model to infer new rules and formulate a regression function to be able to interpolate for the remaining combinations.
[4] During full-chip design or optimization, infer new rules for each spacing-dimension combination seen in design using the regression function directly

B. Correlation Model

Since an analytic model can be integrated into an optimization scheme efficiently and is preferable by designers, our proposed methodology first assigns an analytical interconnect-matching correlation model. We have assumed the following correlation model:[1]

$$\rho = \begin{array}{lll} 1 & , & 1 < (a * A + b/S^2) \\ a * A + b/S^2 & , & 0 \leq (a * A + b/S^2) \leq 1 \\ 0 & , & (a * A + b/S^2) < 0 \end{array} \quad (1)$$

Here, A is the nominal area of one of the matched interconnects and S is the spacing between matched interconnects. The divisor in each term enables the correlation function to stay in the range of $[0, 1]$ as the correlation function is defined in this range. Parameters a and b assign weights to area dependence and spacing dependence individually, as the contributions might not be equal. The sum of a and b can also be used to restrict the upper bound of the correlation function to a value lesser than 1. The assumed correlation function is also chosen such that correlation is directly proportional to the area and inversely proportional to the spacing squared, similar to the reasoning presented in [1] for transistors.

C. Standard Extraction

An overview of the standard procedure will be helpful to understand the differences between standard extraction and extraction for mismatch. Standard capacitance extraction for various spacing and dimension combinations is handled by using field solvers and various interconnect patterns such as parallel interconnects over a ground plane or a cross-over structure. To reduce the simulation time for arrays of multiple interconnects, typically three or five such parallel interconnects are used in a finite mesh and the field solvers are used to extract the capacitances. The reason to use an odd number of interconnects is to introduce symmetry with respect to the interconnect in the middle, so that the coupling capacitances to neighboring interconnects are accounted for. At the end of the simulation, only the capacitances that pertain to the middle interconnect are used, as the outside interconnects have less coupling. This simulation is repeated for a number of interconnect width, length, height and spacing combinations for each structure, and then a regression analysis is used to fit an analytic model to the simulation data. The resultant fitted analytical model can then be used after appropriate model order reduction and signal integrity analysis flows in the timing analysis.

D. Proposed Extraction for Mismatch

We need to add one more interconnect into the simulation box to simulate for mismatch. We propose to use the two middle interconnects to extract the matching criteria, as they are symmetric. For mismatch, a statistical computation is further necessary for each spacing and dimension combination, whereas for standard extraction, it is not. The statistical step can be handled using a Monte Carlo simulation or the statistical method described in [26], which can help reduce number of simulations and improve accuracy. In standard extraction, the result is the capacitances of the middle interconnect. These capacitances can be coupling or total capacitance. In the extraction for mismatch, we propose to use the standard deviation of the difference of capacitances of the middle interconnects divided by the mean of the capacitance in one of the middle wires.[2]

E. Extraction of Correlation Model Parameters

To be able to generate design guarantees, information regarding the process must first be extracted from the limited number of guarantees provided. In order to do this, a correlation model is used. The correlation model is used to assign variations of the interconnect dimensions for each Monte Carlo run. We have used the following equations to implement the statistical simulations.

$$C = M.M^T \quad (2)$$

$$Z = MG \quad (3)$$

Here, C is an nxn, positive-definite and symmetric correlation matrix where n is the number of interconnects in the

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[1]The proposed method is independent of the correlation model assumption. We verify this in the experimental section by using a different correlation model.

[2]We assume that the design guarantee rules are also given using this metric. If they are not, then the correct metric should be used in the extraction of mismatch statistical simulations instead.

simulation box. Matrix M can be found through Cholesky decomposition of C. M^T is the transpose of matrix M. Given nx1 vector G consisting of independent normal Gaussian random variables, vector Z gives a correlated set of random numbers. Elements of Z, Z_i, can then be used to calculate $W_i = Z_i * W_{std} + W_{mean}$, where W_i is the width of the ith interconnect, W_{std} is the standard deviation of the width dimension and W_{mean} is the mean of the width. Height dimension for the interconnects are assigned similarly using Z_i parameters, with the exception of using the standard deviation and mean of height random variable./footnoteIn our analysis, we have assumed height and width as independent, but it is possible to incorporate these correlations into C matrix directly.

We need to first extract the two parameters of the correlation model, a and b, from the given design guarantees. If we can extract these parameters, then we can infer new rules by simulation. However, different A and S combinations are given in the DRM for each rule. This means different correlation functions with respect to the parameters a and b need to be optimized at the same time. Standard multi-variate Newton-Raphson algorithm uses a single function to optimize. Hence, we propose a multi-function variant of multi-variate Newton-Raphson to extract correlation parameters a and b from the provided design guarantees:

Multiple-Function Variant for Multi-Variate Newton-Raphson Algorithm:

[1] **While** $(((\rho_1\text{-}\rho_1^*)/\rho_1 > \epsilon)$ **OR** $((\rho_n\text{-}\rho_n^*)/\rho_n > \epsilon))$ {
[2]   **If** $((\rho_1\text{-}\rho_1^*)/\rho_1 > \epsilon)$ {
[3] $a = a - (\rho_1^* - \rho_1)/\frac{\partial \rho_1}{\partial a}$
[4] $b = b - (\rho_1^* - \rho_1)/\frac{\partial \rho_1}{\partial b}$
[6] $\rho = a * A_n + b/S_n^2$ }
[7]   **If** $((\rho_n\text{-}\rho_n^*)/\rho_n > \epsilon)$ {
[8] $a = a - (\rho_n^* - \rho_n)/\frac{\partial \rho_n}{\partial a}$
[9] $b = b - (\rho_n^* - \rho_n)/\frac{\partial \rho_n}{\partial b}$
[10] $\rho_n = a * A_n + b/S_n^2$ }}

In the algorithm, parameter ρ_n refers to the correlation predicted for the nth design guarantee for the parameter a and b in the current iteration, whereas ρ_n^* indicates the correlation given by the nth design guarantee in the manual. Notice that in reality, the design guarantees do not directly give the correlation, but rather the resultant standard deviation of mismatch over mean of total capacitance for a particular dimension and spacing. Hence, in each iteration of the algorithm, using the a and b of the current iteration, a Monte Carlo is actually run on the field solver and the resultant normalized standard deviation of mismatch is used to compare with the one given in the manual. As Newton-Raphson is known to be fast, convergence is achieved in few iterations within the accuracy level set by the parameter ϵ and a good initial point. We show how to guess a good starting point in the next section.

Here, the algorithm is given for two matching rules. Each criterion corresponds to one particular area and spacing combination. By modifying this formulation, whether there is single or multiple matching criteria in the design manual, a model can be extracted. For the single-criterion case, the statements following the **OR** and the second **If** block need to be eliminated. If there are more than two criteria, then, that many additional terms are added **OR**-wise into the **while** statement and corresponding **If** clauses are added to the algorithm.

If any of the design rules do not provide a close estimation to the DRM for the standard deviation of mismatch over mean using the current a and b values, then the **if** statements help the algorithm to optimize a and b for the violating rules until ϵ error rate can be satisfied for all the design guarantees.

F. Correlation Model Decomposition for a Close Initial Guess

As the area of matched interconnects increases or the spacing decreases, the correlation increases. This analytic model has been proven to work well for small spacings. This restriction is justifiable as the spacing range as well as the area range will be restricted by the process. For example, assuming $0.12^2 < A < 0.36^2$ μm^2 and $0.12 < S < 0.36 \mu m$, the model can be decomposed to:

$$\rho = a' * A/0.36^2 + b' * 0.12^2/S^2 \tag{4}$$

where the maximum area has been used for the first term and minimum spacing squared has been used for the second term as normalization numbers. Now, a' and b' indicate the effective area-dependence and spacing-dependence weights on the final correlation. For example, area-dependence could be more influential than the spacing dependence. If each part is equally important and the normalization constants are chosen according to the technology, a' and b' would be chosen as 0.5 each, hence making the sum equal to 1. A correlation of 1 is the maximum value, which the correlation factor can take by definition. However, a correlation of value 1 would occur only if the two interconnects have the exact same variations, which is not realistic. In practice, a' and b' could add up to somewhere around 0.9 [**?**]. Furthermore, the constants chosen during the decomposition does not exactly correspond to the actual constants as the optimization step will help them converge to their actual values. Such a decomposition makes it possible to come up with close-to-real initial guesses for a and b.

G. Inferring New Guarantees

Given a and b of the correlation model, more $A - S$ combinations can now be inferred. We have run Monte Carlo for field solutions on various $A - S$ combinations using the proposed mismatch extraction method. To extract the mismatch, we propose to use separate Monte Carlo simulations for each width, spacing and length combination. For a single width, spacing and length, 100 to 1000 Monte Carlo simulations are sufficient. For each simulation, we have chosen one of the proposed interconnect patterns, and then widths, lengths, heights and spacings of the interconnects are generated according to the correlation model and extracted values of a and b. We then fit an analytical function over the simulation data.

H. Regression Models for Mismatch.

Herein, we propose regression models for mismatch. These models can be used in CAD tools as compact models for

mismatch data. A high correlation means a lower mismatch, hence A and S^2 have been inverted for the regression model as compared to the correlation model.

The Mismatch Metric. The normalized percentage mismatch metric is calculated using the ratio of standard deviation of the distribution for the difference of capacitances of interconnects 2 and 3, divided by the mean of the distribution for the capacitance of interconnect 2: $\sigma(I2 - I3)/\mu(I2)$

Consideration of Pattern Density. Design guarantees in the manuals bring restrictions on to the allowed minimum and maximum interconnect density due to the CMP step in the manufacturing process. We have considered these cases in our analyses. In the regression analysis, we have used data that covers the maximum and minimum densities so that any valid (A,S) combination can be calculated accurately.

Coupling Capacitance Mismatch Model. The first term for the coupling capacitance model introduced below is a constant term. Second and third terms give the relationship with respect to area and spacing respectively. Finally, the last term is the cross-coupling term.

$$\sigma(I2 - I3)_c/\mu(I2)_c = \alpha + \beta/A + \gamma.S^2 + (1 + \zeta.A/S) \quad (5)$$

Ground Capacitance Mismatch Model. For the ground capacitance mismatch model, we have observed that the power of the spacing term needs to be reduced to 1. Hence the model is given as:

$$\sigma(I2 - I3)_g/\mu(I2)_g = \alpha + \beta/A + \gamma.S + (1 + \zeta.A/S) \quad (6)$$

Special Case: Edge Matching. Chemical-mechanical polishing and lithography require dummy fills or interconnects to avoid dishing. However, on certain designs, inclusion of such dummies might not be possible due to reasons such as chip area or increased coupling. When dummies are not present, matching of a line at the edge and its neighbor will be different than the matching of two middle interconnects. For example, $I1 - I2$ or $I3 - I4$ capacitance matching can be different than matching of $I2 - I3$. In cases when dummies are not used in the design, edge matching can be handled as special cases if increased accuracy is needed. The standard deviation of matching for edge-matching case will have a bias (or rather, a non-zero mean in the density of mismatch), as the line at the edge lacks a coupling capacitor on one side. We have handled these conditions by modeling the edge matching by a separate function.

We have found that the regression model for edge-pair ground capacitance mismatch has the same form as coupling capacitance mismatch.

$$\sigma(I1 - I2)_g/\mu(I2)_g = \alpha + \beta/A + \gamma.S^2 + (1 + \zeta.A/S) \quad (7)$$

Capacitance Regression Model for Mean. When the standard deviation of mismatch needs to be calculated directly, a mean function has to be multiplied with one of the regression functions above as they all are normalized with respect to the mean of a middle interconnect. Hence the mean function is given below:

$$\mu(I2)_g = \alpha + \beta.A + \gamma.S^2 \quad (8)$$

Here, parameters α, β and γ and ζ are fitting constants and each have different values for each model.
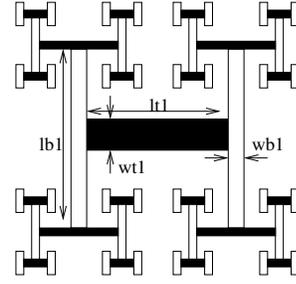

Fig. 4. A 3-level H-tree.
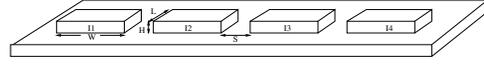
Fig. 5. Proposed mismatch simulation pattern to be used in the field solver

V. UTILIZING INFERRED RULES IN INTERCONNECT OPTIMIZATION

A three-level H-tree is shown in Figure 4. Trunks of the tree are indicated by dark rectangles whereas branches are indicated by light rectangles. One level of the tree corresponds to a trunk and two branches. Given tree level i, level $i + 1$ constitutes of four smaller H-shaped interconnects. Each branch in level $i+1$ needs to match to one another so that clock skew is minimized.[3] For various levels, the branches are sized differently and the spacing between them are also different. We have used 3D field simulations using an interconnect pattern, for which we have proposed to include a fourth line as shown in Figure 5 to extract the percentage mismatch. The interconnects have equal spacings, and are located above a ground plane with inter-layer dielectric separating and surrounding them. We have placed four interconnects into the simulation box and we have extracted the mismatch information from the middle interconnects. The outer interconnects are used to make sure that the coupling capacitances to neighboring interconnects are accounted for the middle interconnects.

A. Interconnect Optimization Formulation for Problem 2

Using geometric programming, we have formulated the H-tree optimization problem while considering mismatch. We have employed simultaneous buffer- and wire-sizing in our optimization.

minimize $(\Omega) \sum_i w_{ti} l_{ti} + (1 - \Omega) \sum B0(b_i + b_{ia})$
subject to:
foreach *i=1:treelevels-1* {
$(R0/b_i) * (\beta * w_{ti} * l_{ti} + 2 * C0 * b_{ia}) \leq t_{ia}$
$(R0/b_ia) * (\beta * w_{bi} * l_{bi} + 2 * C0 * b_{i+1}) \leq t_{ib}$
$(0.125 * \alpha * l_{bi}/w_{bi}) * (\beta * w_{bi} * l_{bi} + 4 * C0 * b_{i+1}) \leq t_{ic}$
$t_{1a} + t_{1b} + t_{1c} \leq D_i$
$Wmin_{ti} \leq w_{ti} \leq Wmax_{ti}$
$Wmin_{bi} \leq w_{bi} \leq Wmax_{bi}$
$w_{bi} \leq w_{ti}$
$w_{ti+1} \leq w_{bi}$
$1 \leq b_i \leq Bmax_i$

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[3]As skew is spatial difference, mismatch in matched interconnects in the same level correspond to a mismatch in clock skew. Hence putting a bound on mismatch is equivalent to putting a bound on skew.

$\sigma_{ti}max <= f_{reg}(A, S)$;
$\sigma_{bi}max <= f_{reg}(A, S)$;

We have used Elmore delay in the optimization. w_{ti} is the width of the trunk, indicated by t, for tree level i. w_{bi} is the width of the branch, indicated by b, for tree level i. l_{ti} and l_{bi} are defined similarly, with l indicating the length of the interconnect. $R0$ and $C0$ are the unit resistance and capacitance of a buffer, respectively. $B0$ is the unit buffer area. b_i and b_{ia} are the buffer size factors for tree level i for trunk and branch respectively. The formulation above is for fixed buffers at each level, one for trunk and one for the branch. The buffers are located at the end points of each trunk or branch. Given b_i, the resistance and capacitance associated with the buffer are $R0/b_i$ and $C0.b_i$ respectively. t_{ia}, t_{ib} and t_{ic} are delays of the buffer, trunk and branch respectively for level i. Ω is the factor which defines the weight of interconnect area vs. buffer area in the optimization. The sum of t_{ia}, t_{ib} and t_{ic} are bounded by the assigned delay, D_i, of level i. $Wmin$ and $Wmax$ parameters are the allowed minimum and maximum widths for the corresponding interconnects. These parameters are selected from the design manual according to which metal layer is to be used for level i.[4] $Bmax$ parameter is used to restrict the maximum allowed buffer size.[5]

The last two constraints are the mismatch constraints used to bound the skew. $\sigma_{bi}max$ is the maximum standard deviation of mismatch assigned to the branches for level i and $\sigma_{ti}max$ for the trunks. We have introduced one constraint for each trunk and branch matching at each level and assumed matched trunks and branches are located at distances of l_{ti} and l_{bi}. If more accuracy is needed, exact distances from layout should be extracted and the geometric program should be updated. f_{reg} is the regression function for mismatch, as given in Section IV-H. f_{reg} takes area and spacing as its parameters.[6]

The geometric programming constraints we have provided are quite flexible. Delay constraints can be assigned to individual wire segments or levels. Similarly, matching constraints can be assigned separately for each level. The wire lengths, number of H-tree levels, number of buffers, buffer locations, delay models and additional constraints can all be changed by trivial modifications. We have limited the optimization criteria to buffer- and wire area-sizing in order to be able to demonstrate the significance of under-utilized resources.

VI. EXPERIMENTAL RESULTS

A. Design Rule Generation Experiments

First, we have conducted experiments for rule generation and then for H-tree optimization. For rule generation, a standard deviation of 5% for process variations is assumed. We have assumed that capacitance mismatch guarantee data is provided in the manual as the starting point. Parameter values

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[4]Usually, top-two metal layers are reserved for power routing and the following 1-3 layers can be used for global tree routing. These three layers are taken to have the same size restrictions.

[5]In standard-cell design, number of allowed sizes are integers. Integration of integers into geometric problems may result in un-optimal solutions. Instead, we have assumed continuous sizes for buffers, corresponding to a custom-buffer design.

[6]As we provide regression functions for both standard deviation over mean and mean separately in Section IV-H, it is possible to calculate the standard deviation only.

TABLE I
EXTRACTED PARAMETERS

	α	β	γ	ζ
coupling	0.3016	-0.0087	0.3872	-0.1908
ground	-0.0703	-0.0073	0.0841	-0.1409
ground for edge	-0.1098	-0.0042	0.4335	-0.1240
mean	0.6117	2.0030	0.2324	

used in the experimentation are based on $65nm$ parameters. 3 initial rules are assumed to be provided.

Rule1: If W$\geq$0.10μm and S$\leq$0.08μm, σ/μ $\leq$0.6875
Rule2: If W$\geq$0.18μm and S$\leq$0.18μm, $\sigma/\mu\leq$0.7635
Rule3: If W$\geq$0.32μm and S$\leq$0.30μm, $\sigma/\mu\leq$0.7819

Height is selected as $120nm$ and the dielectric constant is selected to be a constant of 3 all around the interconnects in the simulation box. The dielectric thickness is selected as $0.140\mu m$. Minimum pattern density is selected to be 25% and the maximum as 75%. Raphael from Synopsys is used for the field simulations.

Using the extracted correlation parameters a and b, widths of the transistors are assigned values for each Monte Carlo run. We have used the width parameters instead of the area to simplify interpreting the simulation results, as area is already proportional to width. We have fit the regression models to the distributions obtained by Monte Carlo simulations. We provide the extracted values for regression models in Table I.

From the provided matching guarantees, actual correlation variables a and b are extracted as 0.1983 and 3.5433 by initializing them as 0.2203 and 3.9370 respectively according to the proposed initialization scheme. Convergence is achieved in only 2 iterations for an error rate of 10E-4 by multiplying the derivatives with 0.5 to avoid divergence. In Figure 6 the original rules from the design manual and 3 generated rules as examples, **R4-R6** are shown with dashed regions. A continuum of such rules can be inferred using the method. A small subset of the generated interconnect matching guarantees are given below.

Rule4: If W$\geq$0.24μm and S$\leq$0.20μm, σ/μ $\leq$0.7471
Rule5: If W$\geq$0.14μm and S$\leq$0.16μm, σ/μ $\leq$0.7679
Rule6: If W$\geq$0.18μm and S$\leq$0.24μm, σ/μ $\leq$0.8038

Going from **R2** to **R6** the spacing has increased while the area has stayed the same, so the mismatch increases. Going from **R3** to **R6** though, the spacing has decreased while the area also has decreased, so the net effect depends on whether the correlation decrease due to decrease of area or the correlation increase due to decrease of spacing dominates. The result shows that decrease of area dominates as the mismatch increases as a result of lower correlation between matched interconnects.

B. Interconnect Optimization Experiments

For the interconnect optimization experiments, we have run the geometric program using traditional optimization and the
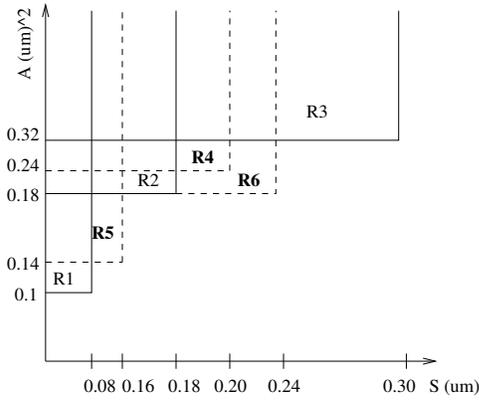
Fig. 6. R4-6 are the generated design guarantees using the proposed method from the original design guarantees R1-3.

proposed method with design rule generation capability, both for minimal total wire and buffer area. We have used a global clock-tree for a $10mm$ by $10mm$ chip. The H-tree is 5 levels. The lengths of the trunk and the branch for level 1 are $5mm$ and these lengths are reduced to one third each consequent level, hence the total length from the driver to each sink is 14.94mm. Total delay is restricted to 300ps.[7] Other parameters are provided in Table II. Raphael from Synopsys is used for the 3D field simulations. GGPLAB from Stanford University is used for solving the geometric program using Matlab [15]. Traditional optimization without design guarantee generation is restricted to selection of matching guarantees directly given in the design manual. Proposed simulation uses the generated guarantees. We have used four experiment sets to cover a range of design decisions for the H-tree.

To demonstrate the flexibility of the proposed method for a variety of correlation function types and to consider the inaccuracy of the correlation model for longer distances for the global interconnect, we have assumed a different correlation function:

$$\rho = f(A, D) = 0.45/3 log_{10}W + 0.375(1 - 1/3 log_{10}S) \quad (9)$$

We have used $\sigma_t(I2-I3) = \sqrt{\sigma_g^2(I2 - I3) + \sigma_c^2(I2 - I3)}$, normalized by W before fitting the regression function. Subscript t indicates the total capacitance. We have introduced the normalization by the width W, as larger widths give larger standard deviations, whereas mismatch is expected to decrease. We have obtained the following regression function directly to calculate the standard deviation of mismatch.

$$\sigma_t(I2 - I3) = 18.1399 + 8.7874/W \quad (10)$$

For the given correlation model for global interconnects and assumed input range, we have observed that spacing does not have to be included in the regression function. We have used this regression function in the geometric optimization algorithm.

C. Discussion of Experiment Sets.

Experiments set 1. Standard deviation of the skew has been restricted to 0.20, 0.20, 0.30, 0.30 and 0.40 ps for tree levels 1 to 5 respectively, both for trunks and branches. Minimum

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[7]The total delay can be decreased by the addition of buffers if needed.

cross-section areas to yield these capacitance-matching conditions have been taken from the DRM. We have handled the traditional optimization by directly using these values from the design manual. Assuming that the designers indeed were satisfied with skew deviations of 0.20, 0.25, 0.30, 0.35 and 0.40 ps for the tree levels, we can see that there is room for constraint relaxation, as second level and fourth level can be relaxed by $0.50ps$ each. Minimum cross-section area to yield these matching conditions can be calculated from the regression function. Hence in the proposed optimization, values calculated through the regression function are used. Four different optimization conditions are furthermore observed. *Actual* condition gives the actual area reduction in Figure 7 whereas the remaining ones give the weighted optimization values for different values of Ω. We have tried different Ω values, in case wire area or buffer area needs to be given a weight due to a design priority. These results are shown in Figure 7. All values indicated in Figure 7 are the percent savings over optimization with original rules.

Experiment set 2. Actual skew matchings are given as 0.20, 0.25, 0.30, 0.40 and 0.60 ps respectively. Assuming the provided rules, which are largest amongst those smaller than the given bounds, are 0.20 and 0.60 ps, skew deviations for the tree levels are chosen as 0.20, 0.20, 0.20, 0.60 and 0.60 ps. 23.1% reduction is observed in the area using optimization with generated design guarantees as compared to optimization with provided guarantees.

Experiment set 3. Actual skew matchings are given as 0.190, 0.192, 0.194, 0.196 and 0.198 ps respectively. Assuming the provided rule, which is largest amongst those smaller than the given bounds, is 0.190 ps only, skew deviations for the tree levels are chosen as 0.190 ps for all levels. 7.91% reduction is observed in the area using generated design guarantees.

Experiment set 4. Actual skew matchings are given as 0.199 ps for all tree levels. Assuming the provided rule, which is largest amongst those smaller than the given bounds, is 0.189 ps only, skew deviations for the tree levels are chosen as 0.189 ps for all levels. 56.8% reduction is observed in the area using the generated design guarantee.

Area can be reduced with the proposed method, as each line can be optimized more accurately using a direct link to the process through which a continuum of rules can be generated instead of a step-wise change as given in the original rules. The larger reduction in the last experiment set is due to continuity becoming more important as constraints get tighter for the given example and process technology. Using the proposed method, designers or circuit optimization tools can save resources by being able to optimize interconnects continuously.

VII. CONCLUSIONS

New back-end rules are projected to provide matching guarantees for interconnects. To cover a continuous range of
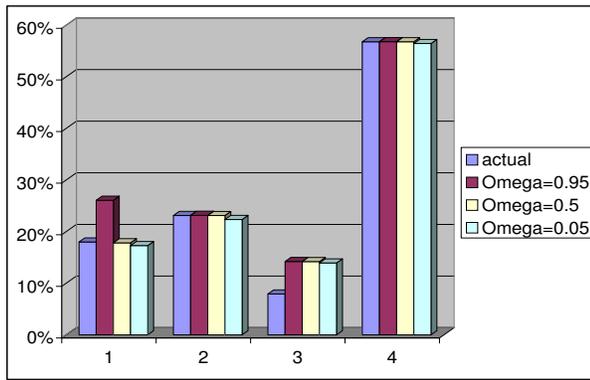
Fig. 7. Percent area reduction using generated guarantees vs. provided guarantees for 4 experiment sets and various optimization weights

interconnect areas and spacings, which are not provided in the manual, we must infer guarantees from the provided ones. Direct extrapolation is not possible as the number of provided design guarantees is so limited; an extraction must be applied to acquire the process variations that have led to the guarantees given in the manual; and finally the standard capacitance extraction procedure has to be modified to be able to account for mismatch. In this paper, we have proposed a methodology that addresses the indicated issues. We have proposed a multi-function variant of Newton Raphson for correlation extraction. We have introduced a decomposition method to guess initial points. We have modified the standard extraction procedure for mismatch. We have introduced parameterized regression functions for mismatch. We have shown the methodology to be working properly on a detailed example. Next, using geometric programming, we have seamlessly incorporated the methodology into a global H-tree optimization scheme for simultaneous wire and buffer sizing for mismatch matching constraints. We have shown that significant resources can be redeemed with the proposed optimization method including guarantee inferring due to continuous traversal of the design space instead of discrete traversal. The designers can either use the generated rules for a process, or the proposed flow can be integrated into in-house CAD tools. The proposed methods will be helpful in other circuit optimizations such as power grid optimization as well with modifications. We plan to extend this methodology to incorporate impact of fills on matching of interconnects.

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