Statistical Gate Delay Calculation with Crosstalk Alignment Consideration

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ABSTRACT

We study gate delay variation caused by crosstalk aggressor alignment, i.e., difference of signal arrival times in coupled neighboring interconnects. This effect is as significant as multiple-input switching on gate delay variation [2]. We establish a functional relationship between driver gate delay and crosstalk alignment by deterministic circuit simulation, and derive closed form formulas for statistical distributions of driver gate delay and output signal arrival time.Our proposed method can be smoothly integrated into a static timing analyzer, which runtime is dominated by sampling deterministic delay calculation, while probabilistic computation and updating take constant time. Our experimental results on 70*nm* technology global interconnect structures and 130*nm* technology industry designs show respectively 159.4% and 147.4% differences in mean and standard deviation of gate delay without crosstalk aggressor alignment consideration, while our method gives within 2.57% and 3.86% offset in gate output signal arrival time mean and standard deviation, respectively.

Categories and Subject Descriptors

B.8.2 [**Hardware**]: INTEGRATED CIRCUITS—*Design Aids*

General Terms

Algorithms, Performance, Design.

1. INTRODUCTION

The latest VLSI manufacturing processes lead to increased variations on layout geometries and circuit performance. Lithographical limitations of manufacturing equipments, e.g., optical proximity, defocus, and lens aberration, affect layout feature dimensions, e.g., wire width and transistor channel length; the chemical mechanical polishing (CMP) process affects layout feature thickness; and ion implantation implies inherent dopant variation. On the other hand, aggressive VLSI design methodologies lead to increased system performance variation. For example, reduced supply voltage and transistor threshold voltage imply reduced noise margin and increased variability; increased device density in a single chip results in increased supply voltage and temperature variations; higher operating frequencies lead to increased capacitive and inductive couplings on silicon surface and in silicon substrate; aggressive performance optimization increases the number of near-critical paths and the probability of timing failure.

Timing verification has been moving away from the traditional over-pessimistic best/worst case analysis and addresses increased variability. Traditional timing analysis takes into account only die-to-die variations, by computing minimum and maximum delays separately, and verifying timing requirements between either minimum or maximum path delays. Corner based timing analysis takes into account on-chip variation by computing minimum and maximum delays simultaneously, and allowing timing verification between minimum and maximum path delays. Statistical static timing analysis (SSTA) computes delay distribution for each pin (block-based) or path (path-based), and provides "timing yield" or probability for a chip to meet its timing requirements.

SSTA is categoried as being either block-based or path-based. Block-based SSTA [1, 6, 16] captures signal arrival time variation at each timing node in a probability distribution function (pdf), and propagates these signal arrival time pdf's in a breadth-first netlist traversal. This is an efficient analysis, which allows incremental update and fits well with optimization. Path-based SSTA [10, 11] provides more accurate statistical analysis, by allowing signal arrival time at a timing node to have different distributions in different timing paths. However, its computational complexity limits the analysis to only a small number of near-critical paths.

A major challenge in SSTA is to capture the correlations between signal arrival times. Signal arrival times are correlated if they come from the same fanout net, or if they are affected by the same global variational parameters. These can be taken into account respectively by conditional signal arrival time pdf computation in the presence of fanout nets [1], and sensitivity-based [3], interval-valued [8], or matrix-perturbation-theory-based [7] analysis which translates layout geometry variation into performance variation. Principle component analysis (PCA) [9] reduces global variational parameters to a smaller set of uncorrelated variations.

Including more sources of variation into consideration has significantly improved accuracy of statistical timing analysis. For example, the mean and the standard deviation of the delay of a gate observe significant deviation when multiple inputs of the gate are switching at the same time [2]. Neglecting this multiple-input switching effect could underestimate the mean delay of a gate by up to 20% and overestimate the standard deviation of the delay of a gate by up to 26%.

We consider another significant source of variation in SSTA, which is the crosstalk aggressor alignment induced driver gate delay variation. A crosstalk aggressor signal switching injects a noise

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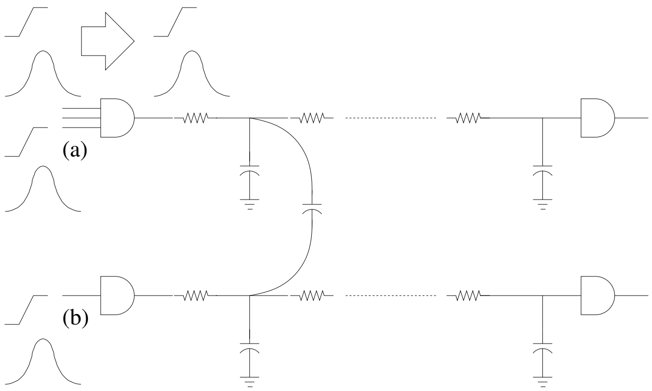

Figure 1: Statistical gate delay calculation taking into account (a) multiple-input switching, and (b) load interconnect crosstalk aggressor alignment (this paper).

to the victim net, which leads to a changed effective load capacitance, and a variation of gate delay for the driver of the victim net. Different crosstalk aggressor signal switching time leads to different gate delay variation for the victim net driver. Finding the worst case crosstalk aggressor alignment which leads to the maximum/minimum gate delay is still open in deterministic timing analysis, although finding the worst case crosstalk aggressor alignment which leads to the maximum/minimum interconnect delay is known [14]. Sinha and Zhou proposed an iterative method for coupling-aware SSTA and proved its convergence [13]. In this paper, we establish a functional relationship between gate delay and crosstalk aggressor alignment, and derive closed form formulas for driver gate delay and its output signal arrival time distributions.

We organize the rest of this paper as follows. Section 2 gives our problem formulation. Section 3 presents our proposed method. Section 4 describes application issues. Section 5 presents empirical observations and experimental results. Section 6 concludes the paper with our ongoing works.

2. PROBLEM

Multiple-input switching has been observed to cause significant gate delay variation (Fig. 1 (a)). We consider another source of variation for gate delay: the difference of the signal arrival time at a coupled neighboring interconnect, i.e., crosstalk aggressor alignment. Different crosstalk aggressor alignment results in different injected crosstalk noise on the victim net and leads to different effective capacitive load for the driver of the victim net, hence different driver gate delay (Fig. 1 (b)).

PROBLEM 1. *Given a system of coupled interconnects, and signal arrival times at the inputs of the drivers, find the signal arrival time distributions at the outputs of the drivers.*

We adopt a recently developed general representation in statistical timing analysis, and consider input signal arrival time distributions in polynomials of possibly correlated random variables [5]. We apply deterministic delay calculation and establish a functional relationship between driver gate delay and crosstalk alignment, which serve as a foundation for statistical delay calculation in consideration of crosstalk alignment effect. In particular, we derive closed form formulas for driver gate delay and driver gate output signal arrival time distributions for given statistical crosstalk alignment. Algorithm 1 summarizes our proposed method.

Algorithm 1: Statistical Driver Gate Delay Calculation for Coupled Interconnects

Input: Coupled interconnects in RC networks, driver gate input signal arrival time distributions
Output: Driver gate output signal arrival time distributions

1. Deterministic gate delay calculation for sampling crosstalk alignments
2. Compute probabilistic gate delay distribution due to crosstalk alignment
3. Compute probabilistic gate output signal arrival time distribution due to crosstalk alignment
4. Include effects of other variation sources, e.g., multiple-input switching, gate length, threshold voltage, and wire width variations

We use the following notations in this paper:

- x_1, x_2 = input signal arrival times
- $x' = x_2 - x_1$ = crosstalk alignment
- D_g = driver gate delay
- y = driver gate output signal arrival time
- μ_1, μ_2 = the means of the input signal arrival times
- σ_1, σ_2 = the standard deviation of the input signal arrival times
- $\sigma_{1,2}^2$ = the covariance of the input signal arrival times
- μ' = the mean of the crosstalk alignment
- σ' = the standard deviation of the crosstalk alignment
- $N(\mu, 3\sigma)$ = normal distribution of the mean μ and the standard deviation σ

We present the details of our proposed method as follows.

3. METHOD

3.1 Inputs

Traditional statistical timing analysis represents a signal arrival time in a normal distribution. Recently, a more generalized statistical representation has been proposed, i.e., by representing a signal arrival time in a polynomial of random variables, which are, e.g., in normal distributions [5].

$$\begin{aligned} x_i &= f_i(r_1, r_2, \ldots) \\ r_i &\sim N(\mu_i, 3\sigma_i) \end{aligned} \quad (1)$$

For simplicity and illustration purpose, we consider first order, i.e., linear approximation of two input signal arrival times in terms of two random variables respectively, s.t., each input signal arrival time is in a normal distribution, and the crosstalk alignment is also in a normal distribution:

$$\begin{aligned} x_1 &\sim N(\mu_1, 3\sigma_1) \\ x_2 &\sim N(\mu_2, 3\sigma_2) \\ x' = x_2 - x_1 &\sim N(\mu' = \mu_2 - \mu_1, 3\sigma\prime = 3\sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_{1,2}^2}) \end{aligned} \quad (2)$$

Our technique can be extended to include multiple random variables in representing a signal arrival time, and to approximate a signal arrival time in higher order polynomials. We can similarly compute closed-form output signal arrival time distributions for higher order, i.e., up to quartic, polynomial approximations which have closed-form roots.

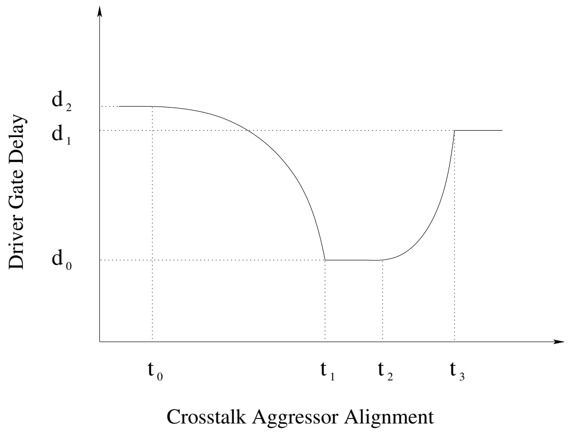

Figure 2: Driver gate delay as a function of crosstalk alignment.

3.2 Deterministic Delay Calculation

We establish a functional relationship between driver gate delay and crosstalk aggressor alignment, as a foundation of the following derivation of driver gate delay and driver gate output signal arrival time distributions. This can be achieved by any deterministic delay calculation method, e.g., most accurately, by a DC sweep analysis in SPICE circuit simulation. Such a simulation integrates effects of various factors, e.g., variations of gate length, transistor threshold voltage, crosstalk alignment, etc., and is common in analog design analysis and optimization, where this is known as the "training" process to establish functional relationships among variables [15]. The resultant sweep function is approximated as a piecewise quadratic function as follows (Fig. 2).

$$D_g = \begin{cases} d_2 & x' \leq t_0 \\ a_0 + a_1 x' + a_2 x'^2 & t_0 \leq x' \leq t_1 \\ d_0 & t_1 \leq x' \leq t_2 \\ b_0 + b_1 x' + b_2 x'^2 & t_2 \leq x' \leq t_3 \\ d_1 & t_3 \leq x' \end{cases} \quad (3)$$

3.3 Derivation of Probabilistic Distributions

Given the input signal arrival time distributions in (2), and the sweep function of driver gate delay in terms of crosstalk alignment in (3), we derive closed form formulas for the victim net driver gate delay and its output signal arrival time distributions, as are presented in Appendix A and B, respectively. The basic technique is to transform the probabilities by finding inverse functions. We use conditional probabilities when variables are correlated, e.g., the input signal arrival time of the victim net and the crosstalk aggressor alignment in computing driver gate output signal arrival times.

The resultant distributions may not be in normal distributions, unless the inputs are normal distributions, and the crosstalk alignments fall in a small region, such that the sweep function in (2) can be approximated in a linear function.

4. APPLICATION

4.1 Combining with Other Variations

Gate delay variation also comes from (1) input signal transition time variation, (2) variation of process parameters, e.g., channel length and threshold voltage of a transistor, and (3) supply voltage variation and multipl-input switching effect. To combine the effects of multiple correlated variations, an effective approach is to (1) reduce the number of variational variables, e.g., via PCA [9], (2) represent delays in closed form functions of the variational variables [5, 8], (3) compute signal arrival times, and (4) achieve

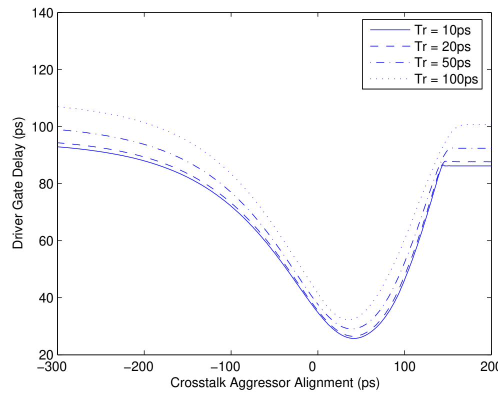

Figure 3: Driver gate delay as a function of crosstalk alignment for a pair of $1000\mu m$ coupled global interconnects in BPTM $70nm$ technology.

timing distribution by sampling and regression based on the correlations between the variational variables. Ongoing research aims for efficiency improvement of this approach.

For independent variations, e.g., crosstalk alignment and gate length variations, we achieve better efficiency by computing the driver gate delay variation by superposition.

$$\begin{aligned} \mu_{total} &= \mu_i + \mu_j \\ \sigma^2_{total} &= \sigma^2_i + \sigma^2_j \end{aligned} \quad (4)$$

where μ_{total} and σ_{total} are in the presence of simultaneous crosstalk alignment and gate length variations, μ_i (μ_j) and σ_i (σ_j) are in the presence of only crosstalk alignment (gate length variation). We give verification of this approach in Section 5.

4.2 Multiple Crosstalk Aggressors

In the presence of multiple crosstalk aggressors, the deterministic delay calculation needs to include multiple crosstalk aggressors for the most accurate results. A functional relationship is established between the driver gate delay and the multiple crosstalk aggressor signal arrival times, and conditional probabilities are applied, such that for each condition, inverse function is computed and gate delay or output signal arrival time distribution is achieved.

In general, the driver gate delay of the victim net cannot be achieved by summing up each aggressor's contribution on the driver gate delay variation, e.g., because the driver gate output resistance varies with load and the number of crosstalk aggressors. However, for certain long interconnects which are driven by large drivers with small output resistance, additivity holds with acceptable inaccuracy, which enables efficiency improvement.

4.3 Runtime Analysis

To apply our technique, we need $O(N)$ times pre-characterization to find the driver gate delay variation for N crosstalk alignment configurations. For each crosstalk alignment configuration, we compute gate delay by either SPICE simulation, or gate modelling and interconnect model order reduction based delay calculation techniques. Regression takes $O(N)$ time. Computing gate delay and gate output signal arrival time distributions takes constant time once the closed form formulas are achieved. Additional runtime requirements include characterization of effects of other variation sources, e.g., gate delay variation due to varied gate length can be obtained by SPICE simulation.

The overall runtime is dominated by gate delay pre-characterization. The number of crosstalk alignment configurations

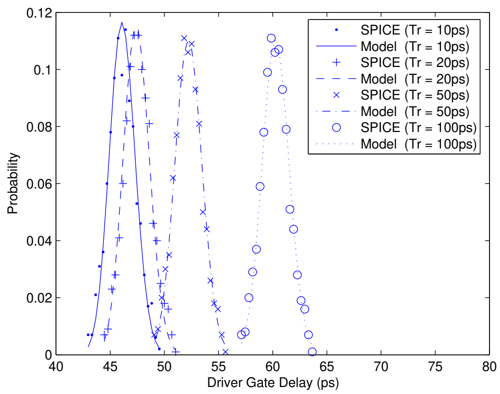

Figure 4: Driver gate delay distributions for a pair of $1000\mu m$ **coupled global interconnects in BPTM** $70nm$ **technology. Input signal transition time is** 10, 20, 50, **or** $100ps$**. Input signal alignment is in a normal distribution** $N(0, 10ps)$**.**

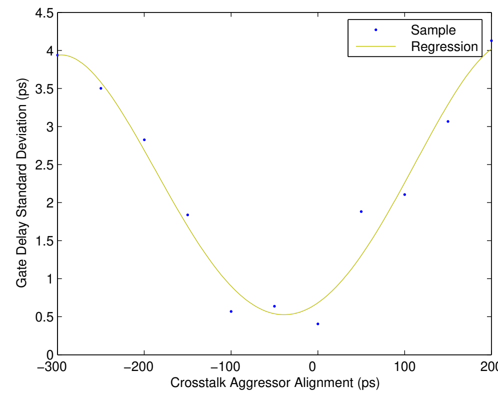

Figure 5: Driver gate delay standard deviation due to gate length variation as a function of crosstalk alignment for a pair of $1000\mu m$ **coupled global interconnects in BPTM** $70nm$ **technology. The transition times of two rising input signals are** $100ps$**. Gate length variation is in a normal distribution** $N(0, 15\%)$**.**

is given by $N = O(\Pi_{i=n} m_i)$ ($N = O(\Sigma_{i=n} m_i)$) for n crosstalk aggressors, each with m_i sampling alignments, when additivity cannot (can) be applied. For each crosstalk aggressor, the number of sampling alignments $m_i = MIN(t_3 - t_0, 6\sigma')/l$ is given by the smaller of (1) $t_3 - t_0$ the time frame within which an aggressor signal transition makes a difference on the victim net driver gate delay, and (2) the $6\sigma'$s of the crosstalk alignment (which can be based on the input signal "timing windows"), for a given time step l between sampling crosstalk alignments. Our method can be implemented in a statistical timing analyzer, where the regression coefficients can be saved, such that re-calculation of gate delay requires only constant time, e.g., in an iteration of signal arrival time pdf refinement.

5. EXPERIMENTS

Our experimental test cases include 16X inverters which drive coupled interconnect instances which are extracted from $130nm$ industry designs, or based on Berkeley Predictive Technology Model (BPTM) $100nm$ and $70nm$ technologies [4].

5.1 Driver Gate Delay Variation due to Crosstalk Alignment

We apply two rising signals to the drivers of a pair of $1000\mu m$ coupled global interconnects in BPTM $70nm$ technology, and conduct SPICE simulation with $2ps$ transient analysis time steps for 100 sampled crosstalk alignments in 1.0 second. The resultant Fig. 3 shows the driver gate delay variation due to crosstalk alignment with different input signal transition times.

A crosstalk aggressor signal transition in the same (opposite) direction leads to a reduced (increased) effective capacitive load for the driver of the victim net, and a victim net driver gate delay decrease (increase). Crosstalk effect takes place for a wide range of aggressor alignments, because the injected crosstalk noise takes longer time to discharge, and the driver gate delay varies with a remaining crosstalk noise charge. An extreme early and an extreme late aggressor signal transition result in different victim net driver gate delays, due to the difference in aggressor driver output resistance which depends on the logic state of the gate.

We approximate the coupled interconnect delay as a piecewise-quadratic function of crosstalk alignment, and compute driver gate delay variation due to varied crosstalk alignment based on the method as is presented in Section 3. Fig. 4 shows that our computed driver gate delay variations match well with the SPICE Monte Carlo simulation results.

5.2 Process Variation Effect with Different Crosstalk Alignments

We bring into account the effect of manufacturing process variations on gate delay variation, such an effect differs with different crosstalk aggressor alignments. As an example, we consider gate length (effective transistor channel length) variation, and study its effect on gate delay for different load interconnect crosstalk aggressor alignments. We consider a gate length variation in a normal distribution which 3σ is 15% of the minimum gate length [2]. We observe that *gate length variation induced gate delay variance is in a piecewise-quadratic function of load interconnect crosstalk alignment* (Fig. 5), similar with mean gate delay variation. For input signals which take transitions in the same (opposite) direction(s), gate delay variance due to varied wire width decreases (increases) when crosstalk effect occurs.

We separate the effects of gate length variation with load interconnect crosstalk alignment variation on driver gate delay. Table 1 demonstrates that *gate delay standard deviation obtained by superposition of the two effects match within* 2.20% *with SPICE Monte Carlo simulation results in the presence of gate length and crosstalk alignment variations.* This validates the superposition approach in the presence of independent variation sources.

We evaluate statistical driver gate delay calculation without crosstalk consideration. Compare the impact of gate length variation on gate delay in the presence of crosstalk effect with that in the absence of crosstalk effect. Table 1 shows that *assuming no crosstalk effect and grounding all coupling capacitors (which is the common practice without crosstalk consideration) results in up to* 159.4% *mismatch in mean interconnect delay, and up to* 147.4% *underestimate in standard deviation of interconnect delay in this case.*

5.3 Output Signal Arrival Time Variation

We compare our computed output signal arrival time distribution with SPICE Monte Carlo simulation results for a typical BPTM global interconnect structure in Fig. 6.

We apply our method to a variety of input signal transition times and input signal arrival time deviations from 50, 100, to $200ps$. To cover different technology nodes, our test cases include $16X$ inverters which drive (I) a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM, and (II) a pair of coupled interconnects which are extracted from a $130nm$ industry design with

Table 1: The means (μ) and the standard deviations (σ) of gate delay (ps) (1) with no variation, (2) with gate length variation, (3) with crosstalk alignment variation, (4) with both gate length and crosstalk alignment variations, (5) with gate length variation and grounded coupling capacitors, all by SPICE Monte Carlo simulation, and (6) our method's estimates with both gate length and crosstalk alignment variations. Input signal transition times $T_r = 10ps, 20ps$, or $50ps$. Mean crosstalk alignment $\mu' = -10ps, 0ps$, or $10ps$.

			(1)	(2)	(3)	(4)	(5)	(5) - (4)	(6)	(6) - (4)
T_r	μ'		none	length	skew	both	w/o xtalk	%diff	w/ xtalk	%diff
10	−10	μ	50.14	50.17	50.12	50.19	120.23	139.5	50.15	-0.08
		σ	-	2.11	1.31	2.44	5.81	138.3	2.48	1.78
10	0	μ	46.30	46.32	46.27	46.34	120.21	159.4	46.29	-0.11
		σ	-	2.11	1.25	2.41	5.81	141.2	2.45	1.76
0	10	μ	42.66	42.67	42.65	42.72	120.23	181.4	42.66	-0.14
		σ	-	2.10	1.15	2.35	5.81	147.4	2.39	1.88
20	−10	μ	51.65	51.66	51.60	51.67	121.68	135.5	51.61	-0.12
		σ	-	2.11	1.31	2.44	5.81	138.3	2.48	1.78
20	0	μ	47.74	47.75	47.71	47.78	121.72	154.7	47.72	-0.13
		σ	-	2.11	1.25	2.41	5.81	141.3	2.45	1.76
20	10	μ	44.14	44.16	44.11	44.18	121.72	175.5	44.13	-0.11
		σ	-	2.10	1.15	2.35	5.81	147.4	2.39	1.88
50	−10	μ	56.24	56.26	56.20	56.27	126.29	124.4	56.22	-0.09
		σ	-	2.11	1.31	2.43	5.81	139.2	2.48	2.20
50	0	μ	52.40	52.41	52.36	52.42	126.30	140.9	52.37	-0.09
		σ	-	2.11	1.25	2.40	5.81	142.2	2.45	2.18
50	10	μ	48.75	48.76	48.71	48.78	126.28	158.9	48.72	-0.12
		σ	-	2.10	1.17	2.36	5.81	146.3	2.40	1.86

Table 2: The means (μ) and the standard deviations (σ) of gate delay and gate output signal arrival times (ps) of (I) a $16X$ inverter which drives one of an array of coupled $1000\mu m$ interconnects of typical global structure in BPTM $70nm$ technology, and (II) a $16X$ inverter which drives a coupled interconnect with 451 resistors and 1637 ground and coupling capacitors in a $130nm$ industry design. Input signal arrival time deviation $3\sigma = 50ps, 100ps$, or $200ps$. Input signal transition time $T_r = 50ps$, $100ps$, or $200ps$.

input		delay				output					
3σ	T_r	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
$70nm$		SPICE		Model		SPICE		Model		%diff	
50	50	52.83	8.86	52.74	8.42	78.6	12.19	77.3	12.66	-1.65	3.86
50	100	60.66	8.71	60.52	8.37	111.4	12.21	110.8	12.64	-0.54	3.52
50	200	74.63	8.75	73.81	8.86	175.4	12.18	174.9	12.36	-0.29	1.48
100	50	54.31	16.31	55.12	16.16	80.8	25.04	79.6	24.37	-1.49	-2.68
100	100	61.38	16.03	61.85	15.87	112.9	24.97	113.7	24.43	0.71	-2.16
100	200	74.19	16.66	74.04	16.84	175.7	24.64	178.3	23.98	1.48	-2.68
200	50	57.06	22.84	56.64	22.75	85.1	55.49	84.1	54.72	-1.18	-1.39
200	100	63.39	23.39	63.17	23.51	116.5	54.86	117.9	55.91	1.20	1.91
200	200	74.3	23.19	74.13	23.07	177.4	52.92	173.8	53.83	-2.03	1.72
$130nm$		SPICE		Model		SPICE		Model		%diff	
50	50	169.67	0.81	168.84	0.8	195.4	16.41	193.6	16.24	-0.92	-1.03
50	100	178.77	0.81	177.23	0.81	229.5	16.41	226.8	16.32	-1.17	-0.55
50	200	197.74	0.79	198.45	0.8	298.5	16.42	295.4	16.29	-1.04	-0.79
100	50	169.98	1.49	170.71	1.48	196.5	32.98	192.9	32.82	-1.83	-0.49
100	100	179.07	1.5	178.46	1.51	230.6	32.97	232.7	32.73	0.91	-0.73
100	200	198.01	1.5	197.68	1.52	299.5	32.96	291.8	33.49	-2.57	1.61
200	50	170.95	2.55	169.42	2.54	199	66.57	196.8	67.01	-1.11	0.66
200	100	180.01	2.56	178.92	2.52	233.1	66.53	231.2	66.07	-0.81	-0.69
200	200	198.87	2.52	198.73	2.51	301.9	66.49	297.8	65.87	-1.36	-0.93

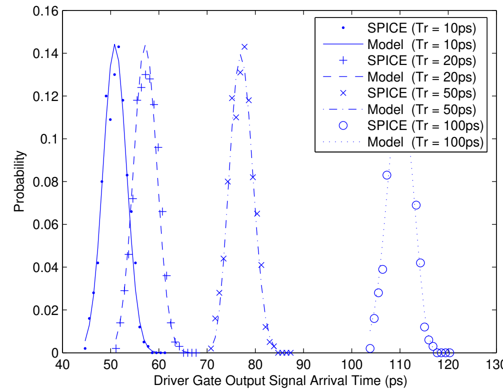

Figure 6: Output signal arrival time distribution for a pair of $1000\mu m$ coupled global interconnect in $70nm$ technolgy given by BPTM with the input signal arrival times in normal distributions $N(0, 10ps)$.

451 resistors and 1637 ground and coupling capacitors. We take a $2ps$ time step between two sampling crosstalk alignments. and compare with 1000 SPICE Monte Carlo simulation runs. The results are shown in Table 2.

We observe that increased input signal arrival time deviations lead to increased driver gate delay and output signal arrival time deviations; while mean driver gate delay decreases with increased input signal transition time. *Over a variety of technology nodes, input signal transition times and arrival time deviations, our method gives the means and the standard deviations of gate output signal arrival times within 2.57% and 3.86% of SPICE Monte Carlo simulation results, respectively.*

6. CONCLUSION

In this paper, we study gate delay variation by load interconnect crosstalk aggressor alignment, i.e., signal arrival time difference at a coupled neighboring interconnect. This is as significant as the multiple-input switching effect on gate delay variation. We present closed-form formulas for probabilistic gate delay calculation based on deterministic delay calculation for sampling crosstalk alignment configurations. After sampling delay calculation, probabilisitic delay calculation and updating take constant time. Our experimental results based on SPICE Monte Carlo simulation verifies our methed, which achieves within 2.57% (3.86%) accuracy for means (standard variations) of gate output signal arrival time, while neglecting crosstalk alignment effect could lead to up to 159.4% (147.4%) mismatch for gate delay means (standard variations), respectively.

Our ongoing research efforts include combination with consideration of other variation sources, e.g., multiple-input switching, wire width variation, and further efficiency improvement techniques in the presence of multiple correlated variations.

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APPENDIX

A. DRIVER GATE DELAY DISTRIBUTION DUE TO CROSSTALK ALIGNMENT

For the input signal arrival time distributions in (2), and the sweep function of driver gate delay in terms of crosstalk alignment in (3), the driver gate delay distribution is as follows.

$$\begin{aligned}
P(D_g=d_0) &= P(t_1<x'<t_2)\\
&= \frac{1}{2}(erf(\frac{t_2-\mu'}{\sigma'})-erf(\frac{t_1-\mu'}{\sigma'}))\\
P(D_g=d_2) &= P(x'<t_0)+B\\
&= \frac{1}{2}erf(\frac{t_0-\mu'}{\sigma'})+B\\
P(D_g=d_1) &= P(x'>t_3)\\
&= 1-erf(\frac{t_3-\mu'}{\sigma'})\\
P(D_g=d, d_0\le d\le d_1) &= A+B\\
P(D_g=d, d_1\le d\le d_2) &= A
\end{aligned} \tag{5}$$

where

$$\begin{aligned}
A &= -\frac{1}{\sqrt{2\pi}\sigma'}\frac{1}{\sigma_{Dga}}e^{-\frac{(-\sigma_{Dga}-a_1-2a_2\mu')^2}{8\sigma'^2a_2^2}}\\
B &= -\frac{1}{\sqrt{2\pi}\sigma'}\frac{1}{\sigma_{Dgb}}e^{-\frac{(-\sigma_{Dgb}-b_1-2b_2\mu')^2}{8\sigma'^2b_2^2}}\\
\sigma_{Dga} &= \sqrt{4a_2(D_g-a_0)+a_1^2}\\
\sigma_{Dgb} &= \sqrt{4b_2(D_g-b_0)+b_1^2}
\end{aligned}$$

B. DRIVER GATE OUTPUT ARRIVAL TIME DISTRIBUTION DUE TO CROSSTALK ALIGNMENT

By approximating the driver gate delay in a piecewise linear function of crosstalk alignment (e.g., for insignificant quadratic terms in (3)), the output signal arrival time is given by convolution of the input signal arrival time and the interconnect delay. Note that the conditional probabilities of the input alignment x' for each input signal arrival time x_1 have different means but the same variance.

$$\begin{aligned}
& P(y)\\
= & \int_{-\infty}^{\infty} P(x_1=y_1-D_g)P(D_g)dD_g\\
= & \int_{t_0}^{t_1} P(x_1=y_1-a_0-a_1x')P(x'|x_1)dx'\\
+ & \int_{t_2}^{t_3} P(x_1=y_1-b_0-b_1x')P(x'|x_1)dx'\\
+ & P(x_1=y_1-d_0)\int_{t_1}^{t_2} P(x'|x_1=y_1-d_0)dx'\\
+ & P(x_1=y_1-d_1)(1-\int_0^{t_3} P(x'|x_1=y_1-d_1)dx')\\
+ & P(x_1=y_1-d_2)\int_0^{t_1} P(x'|x_1=y_1-d_2)dx'\\
= & \frac{1}{\sqrt{2\pi}\sigma_{ya}}e^{-\frac{(y_1-\mu_{ya})^2}{2\sigma_{ya}^2}}\frac{1}{2}(F(y_1,t_1,a_0,a_1,\sigma_{ya})-F(y_1,t_0,a_0,a_1,\sigma_{ya}))\\
+ & \frac{1}{\sqrt{2\pi}\sigma_{yb}}e^{-\frac{(y_1-\mu_{yb})^2}{2\sigma_{yb}^2}}\frac{1}{2}(F(y_1,t_3,b_0,b_1,\sigma_{yb})-F(y_1,t_2,b_0,b_1,\sigma_{yb}))\\
+ & \frac{1}{2}P(x_1=y_1-d_0)(erf(\frac{t_2-\mu_2+y_1-d_0}{\sqrt{2}\sigma'})-erf(\frac{t_1-\mu_2+y_1-d_0}{\sqrt{2}\sigma'}))\\
+ & \frac{1}{2}P(x_1=y_1-d_1)(2-erf(\frac{t_3-\mu_2+y_1-d_1}{\sqrt{2}\sigma'}))\\
+ & \frac{1}{2}P(x_1=y_1-d_2)(erf(\frac{t_0-\mu_2+y_1-d_2}{\sqrt{2}\sigma'})
\end{aligned} \tag{6}$$

where

$$\begin{aligned}
& F(y,t,k_0,k_1,\sigma_{yk})\\
= & erf(\frac{t\sigma_{yk}^2-(1-k_1)(k_0+\mu_2-y)\sigma_1^2+k_1(k_0+\mu_1-y)\sigma'^2}{\sqrt{2}\sigma'\sigma_1\sigma_{yk}})
\end{aligned}$$

$$\begin{aligned}
\mu_{ya} &= \mu_1+a_0-a_1(\mu_1-\mu_2)\\
\sigma_{ya} &= \sqrt{(1-a_1)^2\sigma_1^2+a_1^2\sigma'^2}\\
\mu_{yb} &= \mu_1+b_0-b_1(\mu_1-\mu_2)\\
\sigma_{yb} &= \sqrt{(1-b_1)^2\sigma_1^2+b_1^2\sigma'^2}
\end{aligned}$$