Study of Floating Fill Impact on Interconnect Capacitance

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Abstract

It is well known that fill insertion adversely affects total and coupling capacitance of interconnects. While grounded fill can be extracted by full-chip extractors, floating fill can be reliably extracted by 3D field solvers only. Due to poor understanding of the impact of floating fill on capacitance, designers insert floating fill conservatively. In this paper we study the impact of floating fill insertion on coupling and total capacitance when the fill geometry, and both the interconnects between which the capacitance is measured are on the same layer. We show that the capacitance with same-layer neighboring interconnects is a large fraction of total capacitance, and that it is significantly affected by fill geometries on the same layer. We analyze the effect of fill configuration parameters such as fill size, fill location, interconnect width, interconnect spacing, etc. and consider edge effects and effects occurring due to insertion of several fill geometries in close proximity. Based on our findings, we propose certain guidelines to achieve high metal density while having smaller impact on interconnect capacitance. Finally, we validate the proposed guidelines using representative process parameters and a 3D field solver. On average coupling capacitance increase due to floating-fill insertion decreases by $\sim 53\%$ on using the proposed guidelines.

1. Introduction

Chemical-mechanical polishing (CMP) is the enabling technology to attain high levels of planarization [2]. However, as number of layers increases and line widths shrink, tolerance for topographical imperfections decreases. This is due to tight depth-of-focus variation requirements and high sensitivity of resistance to metal thickness. Despite improvements in CMP technology, layout pattern sensitivities are significant causing certain regions to have higher topographies than others due to differences in underlying densities [9]. Designers and manufacturers use techniques like dummy fill insertion and slotting to respectively increase and decrease the metal density [5]. Dummy fills are non-functional features that do not directly contribute to the logic implementation and can either be grounded or left floating. It is well known that dummy fill insertion can increase the coupling and total interconnect capacitance and consequently deteriorate performance [8, 7].

Traditionally, foundry-supplied design rules have been used by the designers to meet density requirements while not significantly increasing the interconnect capacitance. While fill-insertion design rules have sufficed until now, they are overly conservative and arguably at the end of their life-cycle. Specifically, buffer distance (or keep-off distance) rules have been used to limit the impact of fill on total and coupling capacitance. As crosstalk analysis gains importance and interconnect delay increases, both coupling and total capacitance must be accurately modeled. In absence of reliable fill extraction tools, buffer distance must be increased. Unfortunately this is not feasible since small density variation may not be achievable if buffer distance is large. Hence, there is a need to relax pessimistic buffer distance rules and explicitly model fill impact on capacitance.

Floating fill, in comparison to grounded fill, offers smaller increase in total capacitance and does not require power/ground routes to the fill geometry. However, floating fill increases coupling capacitance that can lead to signal integrity issues. In absence of fast and reliable floating fill extraction tools[1] floating-fill is cautiously used or not used at all (e.g., in analog circuits). Grounded fill, despite its larger impact on total capacitance and high routing costs that often lead to ECOs (engineering change orders), is used as a substitute. Therefore, it is worthwhile to study the impact of floating-fill on interconnect capacitance and to develop its trends to aid the designer.

In [1] a model-library based approach to extract floating-fill was briefly described. Results demonstrating the accuracy of the approach and characterization time were, however, not presented. [6] presented a methodology for full-chip extraction of *total* capacitance in presence of floating-fill and [7] extended their analysis. Their approach adjusts the permittivity and sidewall thickness of dielectric to account for the capacitance increase due to fill. Off-the-shelf extractors can then be used. In our assessment, quantification of the increase in dielectric sidewall thickness and permittivity, and identification of regions where the increase must be applied are the main challenges especially when fill insertion is not performed as regular structures. Unfortunately, these details are lacking. In today's context when the buffer distance rules are under $1\mu m$, the need for accurate floating-fill extraction has been underscored and there is a need for extracting single or small number of fill shapes that may not be arranged regularly between the interconnects.

Previous work has also focused on reducing the capacitance impact of floating-fill without explicitly modeling it. [8] presented a methodology to select optimal floating and grounded fill configurations that satisfy a given thickness variation budget and minimize the increase in interconnect capacitance. In that work very large buffer distances ($> 5\mu m$) were used that are no longer relevant today. Large buffer distances significantly reduce capacitance increase and simplify its estimation. Recently, [4] focused on interconnect design that is aware of the resistive effects of imperfect CMP and capacitance increase due to fill insertion. The paper proposed two useful guidelines (*minimize rows* and *maximize columns*; explained in Section 5) to reduce the floating-fill impact on capacitance. In addition [10] proposed three techniques of fill insertion in order to reduce interconnect capacitance and the number of fills inserted. It also provided with an estimation of the required number

[1]Recent full-chip 3D extraction tools support floating fill extraction. Some of these tools, however, implicitly assume regular fill patterns and large buffer distances. Reliable extraction of floating fill arranged in arbitrary patterns is still, to our knowledge, a topic of active research.

of fill geometries for each of the proposed techniques. However, it fails to report the accuracy and reliability of the methods and estimations for densities greater than 30%.

In this paper we systematically study the impact of various floating-fill configuration parameters such as fill size, fill location, interconnect size, separation from interconnect edges, multiple fill columns and rows, etc. on coupling capacitance. On the basis of our studies, we propose certain guidelines for fill insertion to reduce the capacitance impact of floating-fill while achieving the prescribed metal density. Our results indicate significant reduction in coupling capacitance due to fill insertion on using the proposed guidelines.

We study the effect of floating-fill on capacitance of same layer interconnects only. This restriction simplifies our analyses without significantly compromising the usefulness of our results. We show that: (a) coupling capacitance of an interconnect with same layer interconnects is a large fraction of its total capacitance, and (b) floating-fills on the same layer as two interconnects, significantly increase their coupling capacitance. We perform our experiments on the following three representative interconnect and fill configurations:

1. Medium wire density on layer M, medium wire density on layers $M-1$ and $M+1$.
   We assume layers $M+1$ and $M-1$ to have long parallel wires with area utilization of 33%. Layer M is shown in Figure 1.

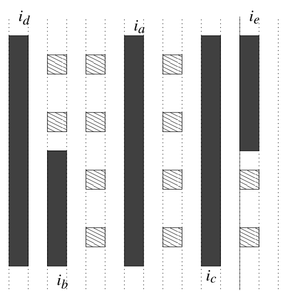


Figure 1: Assumed Layer M for first set of motivation experiments.

2. Medium wire density on layer M, high wire density on layers $M-1$ and $M+1$.
   We use the same layer M configuration as shown in Figure 1. Layers $M+1$ and $M-1$ have 50% area utilization with long parallel wires.

3. Low wire density on layer M, low wire density on layers $M-1$ and $M+1$.
   Layers $M+1$ and $M-1$ have 25% area utilization with long parallel wires and the configuration of layer M is shown in Figure 2.

On all layers square fill shapes of side one track are inserted with a minimum separation of one track from wires and other fills. We do not consider high wire density on layer M because no fill can be inserted then.

Table 1 shows the total capacitance and coupling capacitance with same-layer interconnects before and after fill insertion. We use Synopsys Raphael v-2004.06, a boundary-element method-based 3D field solver, in all our experiments.

The remainder of this paper is organized as follows. Section 2 presents a brief background on why interconnect configurations differ in behavior from an ideal parallel plate capacitor. In Section 3 we present our terminology and assumptions. Section 4 presents certain foundations that we use in our studies in Section 5. Validation for the fill insertion guidelines proposed in Section 5 is done in Section 6. Section 7 concludes with a brief summary of ongoing work.

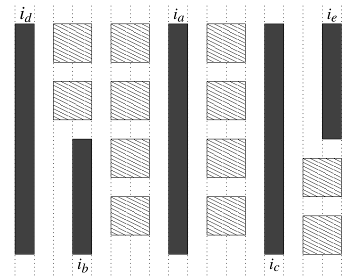


Figure 2: Assumed Layer M for third set of motivation experiments.

2. Background

An ideal parallel plate capacitor is a simple geometry that is similar to the configuration formed by two same-layer interconnects. An ideal parallel capacitor is composed of two large parallel metal plates of equal area (A) and small thickness separated by a small distance (d). The parallel-plate capacitance is given by $\varepsilon A/d$ where ε is the permittivity of the material separating the two plates. Two same-layer interconnects may be viewed as two parallel plates separated by a small distance. However, the height and width of the plates (interconnects) is not large in comparison to the spacing and thus there is a significant divergence from ideal parallel-plate capacitor behavior.

Capacitance of a configuration is directly proportional to the charge accumulated on one of the electrodes ($Q = CV$). The charge density on an electrode depends on the electric field close to the electrode ($E = \sigma/A$). Therefore, the electric field close to an electrode determines the capacitance of a configuration. When a floating plate of thickness t ($t < d$) and the same size as the conductor plates is inserted in the space between the conductors, the capacitance increases to $\varepsilon A/(d-t)$ [11]. I.e., the floating plate effectively reduces the distance between the conductors by its thickness. In case of this configuration, electric field lines are uniform in the space between the plates and normal to them. We call this electric field E_{XX} because it begins from a surface that is normal to the X-axis and ends in one that is also normal to the X-axis. Same-layer interconnect pairs with fill geometries inserted between them, however, have two other components of electric field: (1) E_{ZZ}, the electric field from top (bottom) of one conductor to top (bottom) of another and to the top (bottom) of fill geometries, and (2) E_{XY}, the electric field from the sidewall of a conductor to the orthogonal sidewall of fill. The different components of electric field are illustrated in Figure 3. In configurations where these two electric field components are prominent, capacitance behavior with geometry diverges significantly from ideal parallel-plate capacitance with fill.

3. Terminology and Assumptions

We use the following terminology in this paper:

- The layer of interest on which the floating-fill and coupling interconnects are located is M. $M+1$ and $M-1$ are the layers above and below M respectively. Similarly, $M+2$ and $M-2$ are the layers above $M+1$ and below $M-1$ respectively.
- i_a and i_b are the two wires between which we attempt to study the coupling capacitance C_{ab}. Without loss of generality, we assume that i_a and i_b are vertical.

Table 1: Increase in total capacitance, same-layer coupling capacitance, and coupling capacitance with a neighbor C due to fill insertion.

Deck	Total Capacitance			Same-Layer Coupling			Coupling w/ neighbor (C)		
	Before Fill (fF)	After Fill (fF)	Increase (%)	Before Fill (fF)	After Fill (fF)	Increase (%)	Before Fill (fF)	After Fill (fF)	Increase (%)
1	0.866	0.955	10.28	0.236	0.312	32.20	0.132	0.173	31.06
2	0.888	0.976	9.91	0.220	0.296	34.55	0.125	0.166	32.80
3	0.828	0.973	17.51	0.141	0.268	90.07	0.082	0.152	85.37

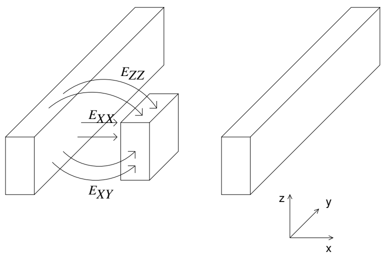


Figure 3: Different electric field components.

- R_{ab} is the rectangle enclosed by i_a and i_b on two sides as shown in Figure 4. If there is no overlap between i_a and i_b in the X-direction, then R_{ab} is undefined. RE_{ab} is R_{ab} extended by the spacing between i_a and i_b on both sides that are orthogonal to i_a and i_b.
- $f_1 \ldots f_n$ are the fill geometries in the region RE_{ab} and the increase in coupling capacitance between i_a and i_b is represented by ΔC_{ab}. We study ΔC_{ab} in all our experiments.
- All sizes are measured in *tracks* and one track is $0.3\mu m$ in keeping with the $90nm$ technology intermediate design rules.

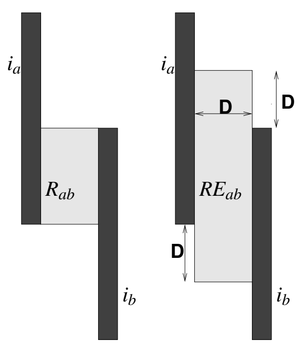


Figure 4: Rectangle enclosed by interconnects i_a and i_b.

In all our experiments we make the following assumptions:

- The two interconnects i_a and i_b are parallel (i.e., are not doglegs).
- We treat layers M+2 and M-2 as ground planes and validate this assumption in the next section.
- Only $f_1 \ldots f_n$ affect C_{ab} (i.e., only the fill geometries in RE_{ab} must be considered while computing C_{ab}). We validate this assumption in the next section.

4. Foundations

In this section we present and validate two foundations that, along with the assumptions, reduce the space of possible fill configurations to analyze.

Table 2: Increase in C_{ab} as a single fill square is moved to the five locations shown in Figure 5.

Location	ΔC_{ab} (aF)
1	0.0353
2	3.7109
3	13.3265
4	14.6215
5	13.2631

4.1 Foundation 1

The coupling capacitance C_{ab} is only affected by the fill geometries lying in the region RE_{ab}. Essentially, we are assuming that the electric field between i_a and i_b is unaffected by fill geometries outside the RE_{ab}. Table 2 shows the increase in C_{ab} for five configurations. In all five configurations, M of Figure 5 is used. There is one fill square of side 2 tracks and the location of it is changed across the five configurations as shown in the figure. Layers M+1 and M-1 are assumed to have 33% density and layers $M-2$ and $M+2$ are assumed to be ground planes (validated in Foundation 2).

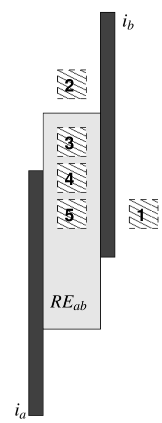


Figure 5: Five configurations used for Foundation 1 experiments.

4.2 Foundation 2

Layers M+2 and M-2 may be treated as ground planes to compute ΔC_{ab} with negligible error. In our validation experiment, i_a and i_b are separated by 4 tracks and both are 18 tracks long. There are three fill squares, each of side 2 tracks, and they are symmetrically placed in RE_{ab}. Layers $M+1$ and $M-1$ have parallel interconnects with area utilization of 33%. ΔC_{ab} is $0.0579fF$ and $0.0520fF$ when the area density on layers $M+2$ and $M-2$ is set to 20% and 33% respectively. The coupling capacitance increase is $0.0447fF$ when layers $M+2$ and $M-2$ are assumed to be ground planes. Most real situations, will have higher $M+1$ and $M-1$ density than 33% which would shield $M+2$ and $M-2$ more making their density's impact smaller. Also, density of $M+2$ and $M-2$ would be higher than 33%. Hence, we expect the error due to assuming $M+2$ and $M-2$ as ground planes to be even smaller.

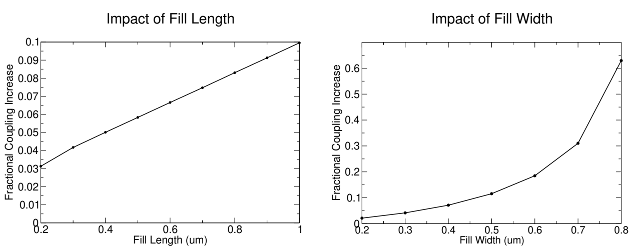
5. Study of Capacitance Impact of Fill

We now present our analyses of impact of floating-fill on coupling capacitance.

5.1 Fill Size

Increasing fill *length* (along the interconnects) increases the number of electric field lines between i_a and i_b that get affected. If we ignore the effect due to the electric field lines to/from the horizontal edges of the fill geometry (E_{XY}, a linear increase in ΔC_{ab} with fill length may be expected. Figure 6(a) shows ΔC_{ab} with fill length. The Y-intercept is due to E_{XY} component of the electric field that is independent of the fill length.

Increasing the fill *width* increases the amount by which electric field lines get affected. In case of an ideal parallel plate capacitor with plates of area A and separated by distance d, when floating metal of area A and thickness t is inserted, the effective capacitance is given by $kA/(d-t)$ (i.e., the floating metal "eats up" a space that is equal to its thickness from between the two capacitor plates.). The increase in C_{ab} is therefore expected to be super-linear due to E_{XX}. Figure 6(b) shows $\Delta C_{ab}/C_{ab}$ when fill width is increased. In our experiments, the spacing between i_a and i_b is fixed at three tracks and the length of wires are set to 17 tracks. Layer $M+1$ and $M-1$ have 33% density while layers $M+2$ and $M-2$ are assumed to be ground planes.

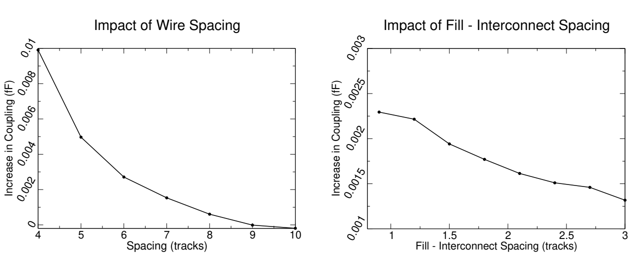


(a) (b)

Figure 6: Impact of fill size on ΔC_{ab}.

5.2 Wire Spacing

We change the spacing between i_a and i_b and study the impact of floating fill on ΔC_{ab}. Wires i_a and i_b are of length 18 tracks and a fill square of side 2 tracks is placed exactly between the wires and mid-way their length (i.e., at the center of the configuration). The spacing between i_a is i_b is increased from 4 tracks to 10 tracks (fill size is not changed). Layers $M+1$ and $M-1$ have a density of 33%, and layers $M+2$ and $M-2$ are ground planes. Figure 7(a) shows the impact of spacing on ΔC_{ab}. When the spacing is large (10 tracks), we observe that ΔC_{ab} becomes negative. This likely happens because the fill square starts coupling i_a and i_b to $M+1$ and $M-1$ wires, effectively reducing C_{ab}.



(a) (b)

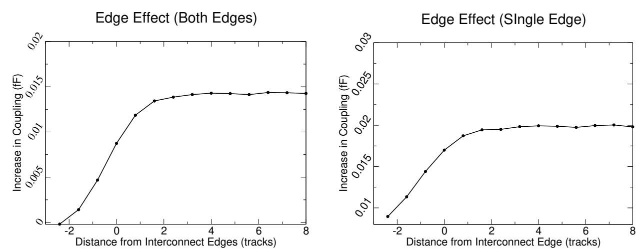
Figure 7: Impact of wire spacing and wire-fill spacing ΔC_{ab}.

5.3 Fill Location

We observe that C_{ab} is unaffected as f_1 is translated along the Y-axis until it starts coming closer to the edge of i_a and/or i_b. We study the edge effects in the next subsection. As the X-coordinate of f_1 is changed, we observe that C_{ab} increases super-linearly. This is likely because as the spacing between f_1 and the nearer wire i_a (without loss of generality) increases, the following two electric fields increase significantly: (1) E_{ZZ}, the electric field between the top (bottom) surface of f_1 and the top (bottom) surface of i_a, and (2) E_{XY}, the electric field between the planes of f_1 to which Y-axis is normal and inside edge of i_a. Figure 7(b) shows ΔC_{ab} as the spacing between f_1 and i_a is reduced. Wires i_a and i_b are of length 17 tracks and spacing 8 tracks, f_1 is 4 tracks long and 2 tracks wide and its spacing from i_a is reduced from 3 tracks to 0.5 tracks. Layers $M+1$ and $M-1$ have 33% density while layers $M+2$ and $M-2$ are ground planes.

5.4 Edge Effects

As the fill geometry f_1 is translated in the vertical direction and it approaches the edge(s) of i_a and/or i_b, we observe edge effects. Primarily, E_{XY}, the electric field between the planes of f_1 to which Y-axis is normal and the inside edge of i_a (and/or i_b), reduces as f_1 approaches closer to the edge(s). On further translation, when f_1 is no longer completely in R_{ab}, ΔC_{ab} dramatically decreases. Figures 8(a) and 8(b) show ΔC_{ab} as f_1 moves closer to and eventually past the edge(s). In Figure 8(a) i_a and i_b are horizontally aligned (i.e., their edges are at the same Y-coordinate). In Figure 8(b) the i_a and i_b are not horizontally aligned and f_1 approaches the edge of i_a while always having i_b on its other side.



(a) (b)

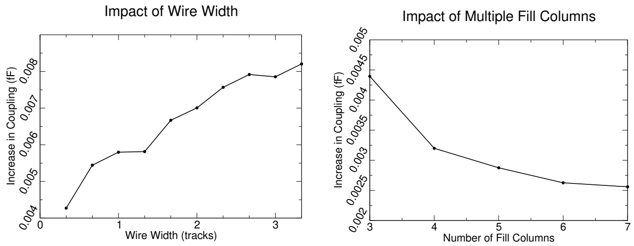
Figure 8: Edge effects in computation of ΔC_{ab}.

5.5 Wire Width

To study the role of wire width, we keep the wire-fill and wire spacing constant and change the width of one wire. We observe that C_{ab} increases with width surrounding the fill shapes increases. In our experiment wires i_a and i_b are of length 18 tracks and spaced by 6 tracks, fill shape f_1 is 4 tracks long and 2 tracks wide and has a spacing of 2 tracks with each of the wires. Layers $M+1$ and $M-1$ have 33% density while layers $M+2$ and $M-2$ are assumed to be ground planes. ΔC_{ab} with wire width is shown in Figure 9 (a). ΔC_{ab} increases rapidly with wire width but saturates at ~ 4 tracks. The electic field component E_{ZZ} likely plays the main role when wire width is increased.

5.6 Multiple Columns

Vertically aligned fill geometries are said to be in a *fill column*. We study the impact of increasing the number of fill columns in a fixed width budget. Our simulation results show that as the number of columns between i_a and i_b increases the coupling capacitance (C_{ab}) reduces. Similar results were reported in [8, 4]. Figure 9(b) illustrates the impact of adding multiple columns on C_{ab}. Wires i_a and i_b are of length 18 tracks and spaced 10 tracks apart. The fill shapes are 2 tracks long by 2 tracks wide. Layers $M+1$ and $M-1$ have 33% density while layers $M+2$ and $M-2$ are considered as ground planes.

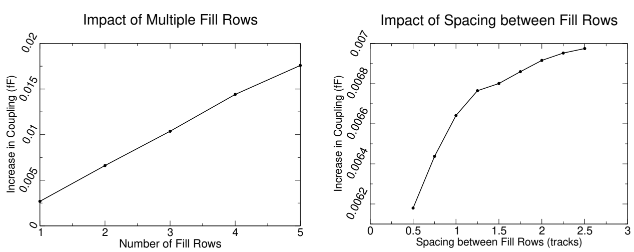


(a) (b)

Figure 9: Impact of wire width and multiple columns on ΔC_{ab}.

5.7 Multiple Rows

In this experiment we increase the number of fill rows which are aligned vertically and observe the impact on the coupling capacitance between i_a and i_b. C_{ab} increases as the number of fill shapes between i_a and i_b increases. As the number of rows is increased, more fill sidewalls are generated that are orthogonal to the interconnect sidewalls and consequently E_{XY} increases. Figure 10(a) shows the impact of adding fill rows on C_{ab}. We also study the impact of the spacing between two consecutive rows on C_{ab}. Figure 10(b) illustrates that as spacing between two fill rows decreases the impact on C_{ab} decreases. We hypothesize that reducing the spacing between two fill rows, reduces the total E_{XY} consequently reducing coupling. Wires i_a and i_b are of length 22 tracks and spaced by 6 tracks. The fill shapes are 2 tracks long and 2 tracks wide. Layers $M+1$ and $M-1$ have 33% density while layers $M+2$ and $M-2$ are assumed to be ground planes.



(a) (b)

Figure 10: Impact of multiple rows and consecutive-row spacing on ΔC_{ab}.

5.8 Fill Insertion Guidelines

On the basis of our studies in the previous section we now prescribe certain guidelines for fill insertion between i_a and i_b such that ΔC_{ab} is small. These guidelines may be selectively applied for interconnects that are timing critical or sensitive to noise. We demonstrate in the next section that the increase in coupling capacitance due to floating fill insertion decreases if these guidelines are followed. The guidelines to reduce C_{ab} in order of their decreasing importance are:

1. *High-impact region.* RE_{ab} is the region in which floating fill insertion impacts C_{ab}. Fill insertion must be avoided in R_{ab}.
2. *Edge effects.* Fill insertion should be preferred at the edges of R_{ab} especially in the region $RE_{ab} - R_{ab}$.
3. *Wire spacing.* Impact on C_{ab} is smaller if spacing between i_a and i_b is large hence fill must be inserted where spacing is large.
4. *Wire width.* Large-width wires are more susceptible to increase in capacitance due to fill. Thinner wire must be preferred as neighbors of fill.
5. *Maximize columns.* The number of columns should be maximized. I.e., fill must be split up subject to the minimum size design rules in a column and spread evenly between i_a and i_b.
6. *Minimize rows.* Fill rows may be merged to reduce C_{ab}.
7. *Increase length not width.* Increasing fill length must be preferred to increasing width to attain the same fill area.
8. *Centralize fill.* Fill or fill configurations when centered between i_a and i_b have a smaller impact on ΔC_{ab}.

6. Validation

In this section we validate the guidelines suggested in the previous section. We consider three layer configurations and insert fill first in a regular grid-like fashion and then with our guidelines to attain the same metal density. The *total* capacitance is measured for the two cases with Raphael. Layers $M+1$ and $M-1$ have long parallel interconnects with metal density of 33% and layers $M+2$ and $M-2$ are ground planes in all three configurations. We follow the following simple design rules:

- Buffer distance is 1 track.
- Minimum fill-to-fill spacing is 1 track.
- Minimum and maximum fill size is 1 and 5 tracks respectively on each side.

Configuration 1

Figure 11 shows the layer M configuration after fill insertion with floating fill inserted in a regular pattern (in (a)), in a staggered pattern (in (b)), and with our guidelines (in (c)). Layer M contains two interconnects, each of length 22 tracks and width 2 tracks, separated by 11 tracks. Without our guidelines, fill is inserted in a grid to attain a density of $\sim 30\%$ in the region illustrated by the dashed rectangle[2]. We use guidelines 2, 5, 6, and 8 to get the configuration shown in Figure 11 (b). We observe that the coupling capacitance increase with respect to regular (staggered) pattern decreases from 62% (64%) to 16%.

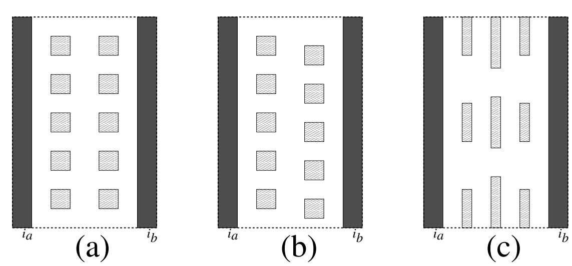


Figure 11: Configuration 1. (a) regular fill pattern, (b) staggered fill pattern, (c) fill insertion with guidelines.

Configuration 2

Figure 12 shows the layer M configuration after fill insertion is performed in a regular pattern (in (a)), in a staggered pattern (in (b)), and with our guidelines (in (c)). Layer M contains two interconnects, each of length 21 tracks and their width changes from 1 to 2 tracks along their length. Without the guidelines, fill is inserted in a grid-like fashion to attain a density of $\sim 48\%$. Guidelines 4 and 6 are used and we observe that the increase in coupling capacitance with respect to regular (staggered) pattern reduces from 41% (41%) to 30%.

Configuration 3

In this configuration we utilize Guidelines 1, 2, 3, 6, and 8. Layer M with fill inserted in regular and staggered fashion is shown in

[2]Tile sizes for density constraints are much larger.

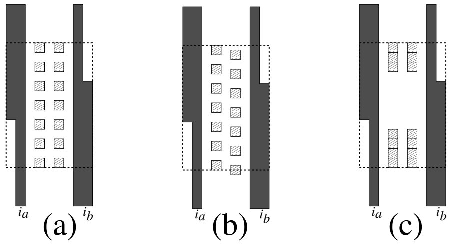


Figure 12: Configuration 2. (a) regular fill pattern, (b) staggered fill pattern, (c) fill insertion with guidelines.

Figures 13(a) and 13(b) respectively. The lengths of interconnects A, B, C, and D are 18, 27, 27 and 27 tracks respectively and their width is 1 track. Wire B has a dogleg of 2 tracks. Fill insertion is performed to attain a metal density of $\sim 42\%$ in the region illustrated by the dashed rectangle. Figure 13(c) shows the configuration after fill insertion is performed with our guidelines. Increase in coupling capacitance is 27%, 27%, and 11% when fill is inserted in a regular pattern, staggered pattern, and with our guidelines respectively. Figure 14 summarizes our results.

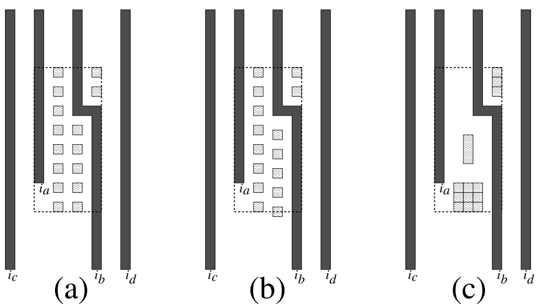


Figure 13: Configuration 3. (a) regular fill pattern, (b) staggered fill pattern, (c) fill insertion with guidelines.

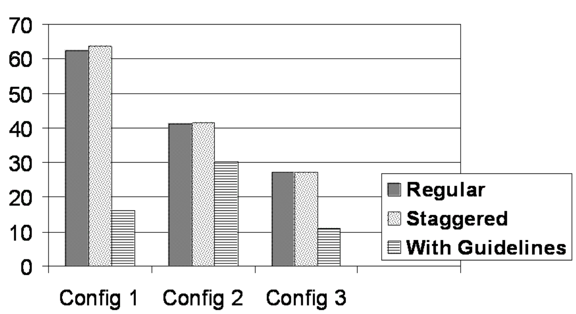


Figure 14: Percentage increase in coupling capacitance for the three configurations when fill insertion is performed in a regular pattern, in a staggered pattern, our guidelines to achieve the same metal density.

7. Conclusions

In this paper we analyzed the increase in coupling capacitance of two same-layer interconnects due to fill insertion on the same layer. We show that same-layer coupling is a large fraction of total capacitance and significantly increases on fill insertion on the same layer. Our studies suggest that the increase in coupling capacitance due to fill insertion:

- is negligible if the fill geometries are outside RE_{ab},
- increases linearly with fill length but has a Y-intercept due to capacitance between the interconnect sidewall and the fill plane that is orthogonal to it (E_{xy}),
- increases super-linearly with fill width,
- decreases super-linearly as interconnect-spacing increases,
- decreases approximately super-linearly as the interconnect-fill spacing is increased,
- remains constant as the fill geometry is translated along the length of the interconnects in R_{ab}, then drops sharply in region RE_{ab} and becomes insignificant outside $RE_{ab} - R_{ab}$.
- increases sharply with interconnect width but saturates when the interconnect width becomes ~ 4 tracks,
- decreases as fill area is distributed over multiple columns,
- increases as fill area is distributed over multiple rows, and
- decreases as the spacing between fill rows is reduced.

Based on our observations, we proposed eight guidelines to reduce floating-fill impact while achieving the prescribed metal density. On our three benchmark configurations coupling capacitance increase due to floating-fill is reduced by $\sim 53\%$ on average with the proposed guidelines.

Ongoing work includes developing analytical models for floating-fill extraction that are conducive for fill-insertion optimizations such as [3].

8. References

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