Statistical Crosstalk Aggressor Alignment Aware Interconnect Delay Calculation

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ABSTRACT

Crosstalk aggressor alignment induces significant interconnect delay variation and needs to be taken into account in a statistical timer. In this paper, we approximate crosstalk aggressor alignment induced interconnect delay variation in a piecewise-quadratic function, and present closed form formulas for statistical interconnect delay calculation with crosstalk aggressor alignment variation. Our proposed method can be easily integrated in a statistical timer, where traditional corner-based timing windows are replaced by probabilistic distributions of crosstalk aggressor alignment, which can be refined by similar delay calculation iterations. Runtime is $O(N)$ for initial delay calculation of N sampling crosstalk aggressor alignments, while pdf propagation and delay updating requires constant time. We compare with SPICE Monte Carlo simulations on Berkeley predictive model 70*nm* global interconnect structures and 130*nm* industry design instances. Our experimental results show that crosstalk aggressor alignment oblivious statistical delay calculation could lead to up to 114.65% (71.26%) mismatch of interconnect delay means (standard deviations), while our method gives output signal arrival time means (standard deviations) within 2.09% (3.38%) of SPICE Monte Carlo simulation results.

Categories and Subject Descriptors

B.8.2 [**Hardware**]: INTEGRATED CIRCUITS—*Design Aids*

General Terms

Algorithms, Performance, Design.

1. INTRODUCTION

With ever-shrinking layout feature sizes, manufacturing process introduces increased variations on layout feature geometry and circuit performance. Manufacturing variations include traditional die-to-die, and emerging intra-die variations. Optical proximity affects feature dimensions, e.g., wire width or transistor channel length; local layout density affects CMP process and varies feature thickness; placement affects defocus. On the other hand, aggressive VLSI designs also induce increased variations on system performance. Integration of increased number of components in a single chip results in increased supply voltage drop and temperature variation; higher operating frequencies observe increased capacitive and inductive couplings on silicon surface and through substrate; aggressive performance optimization could result in a large number of near-critical paths with increased probability of timing failure.

Timing verification evolves from over-pessimistic best/worst case analysis to address increased variability. (1) Traditional minimum/maximum-based timing analysis, which computes minimum and maximum delays separately, and verifies timing requirements between either minimum or maximum path delays, captures die-to-die variations. (2) Corner based timing analysis, which computes both minimum and maximum delays for data paths and clock distribution networks, and allows combined minimum and maximum path delays in timing verification, captures intra-die variations. (3) Statistical static timing analysis (SSTA), which computes delay distribution for each pin (block-based) or path (path-based), provides "timing yield" or probability for a chip to meet timing requirements.

Block-based SSTA [1, 8, 20] represents signal arrival time variation at each pin as a probability distribution function (pdf). Assuming symmetry or normality of signal arrival time distributions, these probability distribution functions are computed based on simple formulas in a breadth-first netlist traversal, which is efficient, incremental, and suitable for optimization. Path-based SSTA [13, 14] provides more accurate statistical analysis on a set of near-critical paths, e.g., in corner-based or Monte Carlo analysis, signal arrival time at a pin could have different distributions in different paths, where correlations due to path-sharing can be better captured. Timing criticality probabilities and correlations of the near-critical paths are computed for signoff analysis.

Correlations come from (1) path-sharing in the presence of reconvergent fanouts, and (2) dependence on common variational parameters. Correlated pdf's can be propagated in conditional probabilities [1]. Correlated parameters can be broken down into uncorrelated random variables in principle component analysis (PCA) [11]. Layout geometrical variations are translated into performance variations by sensitivity-based[3], interval-valued [10], or matrix-perturbation-theory-based [9] analysis through interconnect model order reduction [12, 16].

Crosstalk aggressor alignment induced interconnect delay variation and multiple input switching induced gate delay variation introduce significant timing uncertainty and must be taken into account by a statistical static timing analyzer. Agarwal et al. [2] show that neglecting multiple-input switching effect underestimates mean gate delay by up to 20% and overestimates

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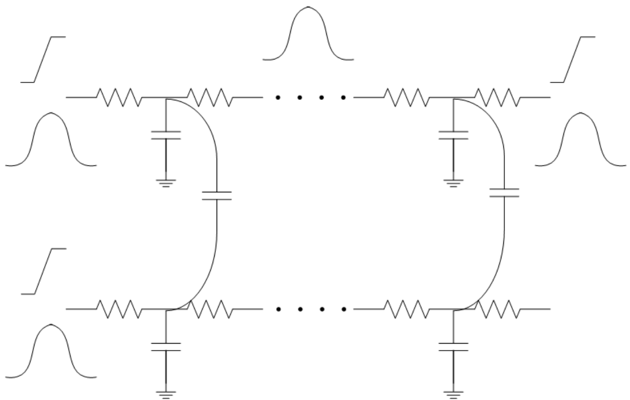

Figure 1: Statistical delay calculation for coupled interconnects: to compute interconnect delay and output signal arrival time variations for given input signal arrival time variations.

gate delay standard deviation by up to 26%. They further derived an empirical model which predicts the gate delay standard deviation as a weighted sum of the input signal arrival time standard deviations [2].

We consider an equally significant source of uncertainty in SSTA, which is the crosstalk aggressor alignment induced interconnect delay variation, in this paper. Effect of process variation, e.g., of wire width, has been taken into consideration [3, 9, 10]. However, to the best of our knowledge, we are the first to include crosstalk aggressor alignment effect into consideration in SSTA.

Our study starts with empirical observations on interconnect delay with different input signal alignments, followed by a piecewise quadratic approximation of interconnect delay as a function of input signal alignment. We give theoretical results of interconnect delay and output signal arrival time variation for given input signal arrival time variations and wire width variation, and verify our theoretical interconnect delay calculation model by SPICE Monte Carlo simulation on BPTM 70*nm* global interconnect structures and instances from 130*nm* technology industry test cases. Our experiments show that crosstalk aggressor alignment oblivious statistical delay calculation could lead to up to 114.65% (71.26%) mismatch of interconnect delay means (standard deviations); while our model gives output signal arrival times means (standard deviations) within 2.09% (3.38%) of SPICE Monte Carlo simulation results.

The rest of this paper is organized as follows. Section 2 presents our theoretical model. Section 3 describes implementation issues, runtime analysis, and iterations needed in SSTA for crosstalk effect. Section 4 presents empirical observations and experimental results which verify the assumptions and the results of our model, and finally Section 5 concludes the paper with a description of our ongoing works.

2. STATISTICAL DELAY CALCULATION FOR COUPLED INTERCONNECTS

We study the following problem (Fig. 1):

PROBLEM 1. *Given a coupled interconnect system,*[1] *their input signal arrival times and wire widths in normal distributions, find the output signal arrival time distributions.*

[1]We consider two coupled interconnects in this paper for illustration; a system of multiple coupled interconnects can be analyzed by superposition since an RLC interconnect is a linear system.

We use the following notations in this paper:

- x_1, x_2 = input signal arrival times
- $x' = x_2 - x_1$ = input signal alignment
- τ_1, τ_2 = interconnect delays
- y_1, y_2 = output signal arrival times
- μ_1, μ_2 = the means of the input signal arrival times
- σ_1, σ_2 = the standard deviations of the input signal arrival times
- $\sigma_{1,2}$ = the correlation between the input signal arrival times
- μ' = the mean of the input signal alignment
- σ' = the standard deviation of the input signal alignment
- $N(\mu, 3\sigma)$ = normal distribution of the mean μ and the standard deviation σ

We present our proposed method in Algorithm 1 and describe each step in detail as follows.

Algorithm 1: Statistical Delay Calculation for Coupled Interconnects

Input: Coupled interconnects in RC networks,
input signal arrival times in normal distributions,
wire width variation in normal distributions
Output: Output signal arrival time variation

1. Interconnect delay calculation for sampled aggressor alignments
2. Approximate interconnect delay in a piecewise-quadratic function of aggressor alignment
3. Propagate signal arrival time distributions by closed-form formulas
4. Combine with other variations

2.1 Inputs

For illustration, we start with a pair of coupled interconnects with statistical input signal arrival times. A statistical signal arrival time can be represented in a polynomial of (normally distributed) random variables as follows [7].

$$\begin{aligned} x_i &= f_i(r_1, r_2, \ldots) \\ r_i &\sim N(\mu_i, \sigma_i) \end{aligned} \qquad (1)$$

For simplicity, we consider first order, i.e., linear approximation of two input signal arrival times in terms of two random variables respectively, s.t., each input signal arrival time is in a normal distribution, and the crosstalk alignment is also in a normal distribution:

$$\begin{aligned} x_1 &\sim N(\mu_1, \sigma_1^2) \\ x_2 &\sim N(\mu_2, \sigma_2^2) \\ x' = x_2 - x_1 &\sim N(\mu' = \mu_2 - \mu_1, \sigma'^2 = \sigma_1^2 + \sigma_2^2 + \sigma_{1,2}^2) \end{aligned} \qquad (2)$$

Our technique can be extended to include multiple random variables in representing a signal arrival time, and to approximate a signal arrival time in higher order polynomials. We can similarly compute closed-form output signal arrival time distributions for higher order, i.e., up to quartic, polynomial approximations which have closed-form roots.

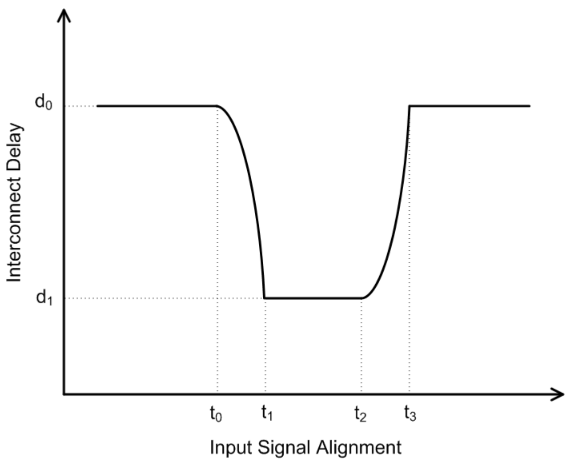

Figure 2: Interconnect delay as a function of input signal alignment.

2.2 Interconnect Delay as a Function of Crosstalk Aggressor Alignment

Traditional crosstalk delay calculation is based on the "timing window" concept, i.e., the time frame defined by the earliest and the latest signal arrival time of a net. If two physically coupled interconnects have overlapped timing windows, crosstalk effect takes place and alters the interconnect delays of the two nets. The effect of crosstalk aggressor alignment is more complex than the simple timing window concept, i.e., crosstalk effect increases gradually as the victim and the aggressor signal arrival times align to each other (Fig. 2). This effect has long been observed, and interconnect delay is adjusted, e.g., by table lookup with index of relative timing window [17], by closed-form expressions based on specific waveform assumption and first-order [18] or second-order [5] Taylor expansion in solving an exponential equation for changed interconnect delay. We compute interconnect delay for different crosstalk aggressor alignments, e.g., by SPICE simulation or any model order reduction based delay calculation method, and approximate interconnect delay variation in a piecewise-quadratic function of crosstalk aggressor alignment as follows.

$$\tau = \begin{cases} d_0 & x' \le t_0 \\ a_0 + a_1 x' + a_2 x'^2 & t_0 \le x' \le t_1 \\ d_1 & t_1 \le x' \le t_2 \\ b_0 + b_1 x' + b_2 x'^2 & t_2 \le x' \le t_3 \\ d_0 & t_3 \le x' \end{cases} \quad (3)$$

2.3 Interconnect Delay Variation Due to Varied Input Signal Alignment

As a piecewise quadratic function (3) of input alignment in a normal distribution (2), interconnect delay has its probability distribution as follows.

$$\begin{aligned} P(\tau = d_1) &= \frac{1}{\sqrt{2\pi}\sigma'} \int_{t_1}^{t_2} e^{-\frac{(x'-\mu')^2}{2\sigma'^2}} dx' \\ &= \frac{1}{2}\left(Erf\left(\frac{t_2-\mu'}{\sigma'}\right) - Erf\left(\frac{t_1-\mu'}{\sigma'}\right)\right) \end{aligned} \quad (4)$$

$$\begin{aligned} P(\tau = d_0) &= 1 - \frac{1}{\sqrt{2\pi}\sigma'} \int_{t_0}^{t_3} e^{-\frac{(x'-\mu')^2}{2\sigma'^2}} dx' \\ &= 1 - \frac{1}{2}\left(Erf\left(\frac{t_3-\mu'}{\sigma'}\right) - Erf\left(\frac{t_0-\mu'}{\sigma'}\right)\right) \end{aligned} \quad (5)$$

For $d_1 \le d \le d_0$, the cdf of interconnect delay is given by

$$\begin{aligned} & P(\tau < d) - P(\tau = d_0) \\ = & \frac{1}{\sqrt{2\pi}\sigma'}\left(\int_{t_a}^{t_1} e^{-\frac{x'-\mu'}{2\sigma'^2}} dx' + \int_{t_2}^{t_b} e^{-\frac{x'-\mu'}{2\sigma'^2}} dx'\right) \\ = & \frac{1}{\sqrt{2\pi}\sigma'}\left(\int_{d_1}^{d} \frac{e^{-\frac{(\sigma_{\tau a} - a_1 - 2a_2\mu')^2}{8\sigma'^2 a_2^2}}}{\sigma_{\tau a}} d\tau + \int_{d_1}^{d} \frac{e^{-\frac{(\sigma_{\tau b} - b_1 - 2b_2\mu')^2}{8\sigma'^2 b_2^2}}}{\sigma_{\tau b}} d\tau\right) \end{aligned} \quad (6)$$

where

$$\begin{aligned} t_a &= \frac{-a_1 - \sqrt{a_1^2 + 4a_2(d - a_0)}}{2a_2} \\ t_b &= \frac{-b_1 - \sqrt{b_1^2 + 4b_2(d - b_0)}}{2b_2} \\ \sigma_{\tau a} &= \sqrt{4a_2(\tau - a_0) + a_1^2} \\ \sigma_{\tau b} &= \sqrt{4b_2(\tau - b_0) + b_1^2} \end{aligned}$$

Taking the derivatives gives the pdf as follows.

$$\begin{aligned} & P(\tau = d, d_1 \le d \le d_0) \\ = & -\frac{1}{\sqrt{2\pi}\sigma'}\left(\frac{1}{\sigma_{\tau a}} e^{-\frac{(-\sigma_{\tau a} - a_1 - 2a_2\mu')^2}{8\sigma'^2 a_2^2}} + \frac{1}{\sigma_{\tau b}} e^{-\frac{(-\sigma_{\tau a} - b_1 - 2b_2\mu')^2}{8\sigma'^2 b_2^2}}\right) \end{aligned} \quad (7)$$

2.4 Output Signal Arrival Time Distribution

For closed-form formulas of output signal arrival time distribution, we approximate interconnect delay in a piecewise linear function of input signal alignment.[2] The output signal arrival time is given by convolution of the input signal arrival time and the interconnect delay as follows. Note that the conditional probabilities of the input alignment x' for each input signal arrival time x_1 have different means but the same variance.

$$\begin{aligned} & P(y_1) \\ = & \int_{-\infty}^{\infty} P_1(y_1 - \tau_1) P_\tau(\tau_1) d\tau_1 \\ = & \int_{t_0}^{t_1} P_1(y_1 - a_0 - a_1 x') P'(x'|x_1) dx' \\ + & \int_{t_2}^{t_3} P_1(y_1 - b_0 - b_1 x') P'(x'|x_1) dx' \\ + & P_1(y_1 - d_0)(1 - \int_{t_0}^{t_3} P'(x'|x_1 = y_1 - d_0) dx') \\ + & P_1(y_1 - d_1) \int_{t_1}^{t_2} P'(x'|x_1 = y_1 - d_1) dx' \\ = & \frac{1}{2\sqrt{2\pi}\sigma_{ya}} e^{-\frac{(y_1 - \mu_{ya})^2}{2\sigma_{ya}^2}} (F(y_1, t_1, a_0, a_1, \sigma_{ya}) - F(y_1, t_0, a_0, a_1, \sigma_{ya})) \\ + & \frac{1}{2\sqrt{2\pi}\sigma_{yb}} e^{-\frac{(y_1 - \mu_{yb})^2}{2\sigma_{yb}^2}} (F(y_1, t_3, b_0, b_1, \sigma_{yb}) - F(y_1, t_2, b_0, b_1, \sigma_{yb})) \\ + & P_1(y_1 - d_0)(1 - \tfrac{1}{2}(Erf(\tfrac{t_3 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}) - Erf(\tfrac{t_0 - \mu_2 + y_1 - d_0}{\sqrt{2}\sigma'}))) \\ + & \tfrac{1}{2} P_1(y_1 - d_1)(Erf(\tfrac{t_2 - \mu_2 + y_1 - d_1}{\sqrt{2}\sigma'}) - Erf(\tfrac{t_1 - \mu_2 + y_1 - d_1}{\sqrt{2}\sigma'})) \end{aligned} \quad (8)$$

[2] Such approximation is accurate in most cases with insignificant quadratic terms in (3), otherwise, better accuracy can be achieved by further segmentation.

where

$$F(y,t,k_0,k_1,\sigma_{yk}) = Erf(\frac{t\sigma_{yk}^2+(k_1-1)(k_0+\mu_2-y)\sigma_1^2+k_1(k_0+\mu_1-y)\sigma\prime^2}{\sqrt{2}\sigma'\sigma_1\sigma_{yk}})$$

$$\mu_{ya} = \mu_1+a_0-a_1(\mu_1-\mu_2)$$
$$\sigma_{ya} = \sqrt{(1-a_1)^2\sigma_1^2+a_1^2\sigma\prime^2}$$
$$\mu_{yb} = \mu_1+b_0-b_1(\mu_1-\mu_2)$$
$$\sigma_{yb} = \sqrt{(1-b_1)^2\sigma_1^2+b_1^2\sigma\prime^2}$$

2.5 Including Other Variation Sources

Variations of signal transition times and process parameters, e.g., wire width, introduce additional interconnect delay variation, which impact generally differs with different input signal alignment. To combine the effects of multiple variation sources, one can (1) enumerate all the conditions, e.g., all possible input signal alignments, (2) compute interconnect delay variation for each condition, and (3) combine the conditional probabilities, as in [2].

For independent variations, e.g., input signal alignment and wire width variations, we achieve better efficiency by computing the coupled interconnect delay variation by superposition.

$$\mu_{total} = \mu_i+\mu_j$$
$$\sigma_{total}^2 = \sigma_i^2+\sigma_j^2 \quad (9)$$

where μ_{total} and σ_{total} are in the presence of simultaneous input signal alignment and wire width variations, μ_i (μ_j) and σ_i (σ_j) are in the presence of only input signal alignment (wire width variation). We give verification of this approach in Section 4.

3. IMPLEMENTATION

3.1 Runtime Analysis

Computing the interconnect delay as a function of input signal alignment takes $O(N)$ time, where N is the number of sampling input signal alignments. We compute each aggressor's effect, which can be superposed due to the linearity of an RLC interconnect. For each input signal alignment, we compute interconnect delay either by the model-order-reduction technique [12, 16], or by SPICE simulation. Fitting takes $O(N)$ time, while computing interconnect delay distribution takes constant time with the closed form formulas. Interconnect delay variation due to varied wire width can be computed using one of the existing techniques as described in [3, 9, 10].

The overall runtime is dominated by N times interconnect delay calculation for different input signal alignments, where $N = MIN(1.5T_r, 6\sigma')/l$ is given by the smaller of (1) 1.5 times input signal transition time (because crosstalk occurs for input signal alignment $-T_r \leq x' \leq \frac{1}{2}T_r$), and (2) the $6\sigma'$s of the input signal alignment (which can be based on the input signal "timing windows"), for a given time step l between sampling input signal alignments. Our method can be implemented in a statistical timing analyzer, where the fitting coefficients can be saved, such that re-calculation of interconnect delay requires only constant time (i.e., in an iteration, as we discuss in the following).

Table 1: Geometries (length L, width W, spacing S and thickness T) and R/C parameters (resistance R, coupling capacitance C_c and ground capacitance C_g) for copper interconnects in $70nm$ and $100nm$ technologies given by BPTM. Inter-layer dielectric (ILD) height is $0.20\mu m$, $k = 2.2$ in $70nm$ technology; ILD height is $0.30\mu m$, $k = 2.8$ in $100nm$ technology.

$70nm$	L (μm)	W (μm)	S (μm)	T (μm)	R (Ω)	C_c (fF)	C_g (fF)
global	1000	0.45	0.45	1.20	40.74	73.22	82.03
intermediate	200	0.14	0.14	0.35	89.80	11.53	6.23
local	30	0.10	0.10	0.20	33.00	1.61	0.67
$100nm$	L (μm)	W (μm)	S (μm)	T (μm)	R (Ω)	C_c (fF)	C_g (fF)
global	1000	0.50	0.50	1.20	36.67	88.37	82.93
intermediate	200	0.20	0.20	0.45	48.89	13.65	7.56
local	30	0.15	0.15	0.30	14.67	2.05	0.86

3.2 Multiple Iterations

In traditional mininum/maximum-based STA, delay calculation for coupled interconnects goes through an iteration of pessimism reduction and timing window refinement. The iteration starts with the worst-case assumptions that signals could arrive at any time for each interconnect, and all neighboring interconnects have possible cross-coupling effects. Timing windows are computed to bound signal arrival times at each interconnect. If the timing windows do not overlap for two neighboring interconnects, cross-coupling effects between them need to be taken out of consideration and their delays need to be re-calculated to give updated timing windows and reduced pessimism.

In SSTA, iterations of pessimism reduction can also be applied. This is because STA proceeds in a topological order of the netlist, which guarantees that all inputs of a gate are computed before the output of the gate. However for physically coupled interconnects, their inputs may not be given at the time of delay calculation. A pessimistic distribution can be assumed to be refined later during iteration.

4. EXPERIMENTS

4.1 Test Instances

Our experimental test cases include coupled interconnect instances which are extracted from $130nm$ industry designs, and typical coupled interconnect structures in $100nm$ and $70nm$ technologies given by the Berkeley Predictive Technology Model (BPTM) [4]. Table 1 shows the geometries and the resistances, ground capacitances, and coupling capacitances of $1000\mu m$ global, $200\mu m$ intermediate, and $30\mu m$ local copper interconnects in $100nm$ and $70nm$ technologies given by BPTM, respectively.

4.2 Interconnect Delay as a Function of Input Signal Alignment

We apply two signal transitions to a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM. Fig. 3 shows the interconnect delay as a function of input signal alignment for different input signal transition times for two signals in the same direction, where interconnect delay decreases when crosstalk effect occurs. For two signals in the opposite directions, interconnect delay increases when crosstalk effect occurs.

We observe that increased input signal transition time leads to increased interconnect delay. Crosstalk effect occurs when the

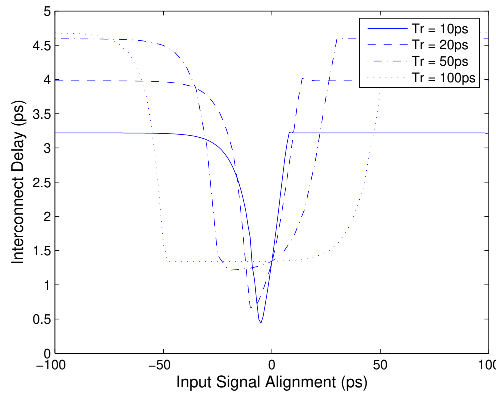

Figure 3: Coupled interconnect delay as a function of input signal alignment for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM.

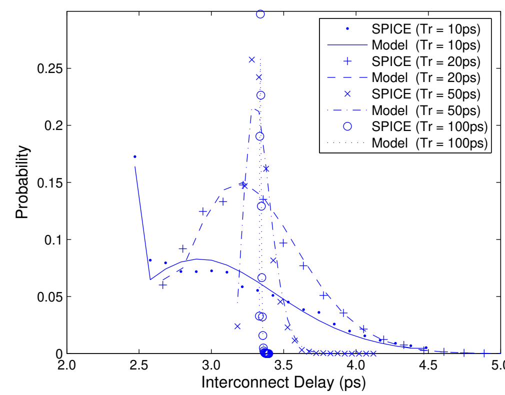

Figure 4: Interconnect delay distributions for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM. Input signal transition time is 10, 20, 50, or $100ps$. Input signal alignment is in a normal distribution $N(0,10ps)$.

Table 2: Coefficients and standard deviations of quadratic fits of interconnect delay (ps) as a function of input signal alignment for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM.

Tr	a_0	a_1	a_2	std. dev.	b_0	b_1	b_2	std. dev.
10	-1.26	-0.36	-7.47E-3	0.38	1.35	0.22	4.93E-3	0.10
20	-2.49	-0.41	-6.79E-3	0.55	1.34	0.13	5.61E-3	0.05
50	-4.51	-0.34	-3.10E-3	0.80	1.22	0.03	2.70E-3	0.04
100	-8.53	-0.31	-1.81E-3	1.04	1.66	-0.04	1.41E-3	0.07

input signal transitions overlap (i.e. from $-T_r$ to $\frac{1}{2}T_r$), which leads to reduced interconnect delay in this case with two rising signal transitions. The maximum delay variation occurs if the aggressor signal completes its transition when the victim signal reaches the 50% delay threshold (i.e. at $-\frac{1}{2}T_r$).

For signals with large transition times (i.e. $\geq 50ps$ here), interconnect delay is less sensitive to signal transition time variation, either with or without crosstalk effect. It is also less sensitive to most of the possible input signal alignments when a crosstalk effect occurs, i.e., although crosstalk effect occurs over a larger range of input signal alignment with a larger signal transition time, interconnect delay is only sensitive to a certain range of input signal alignment (see the nearly identical slope of the rising and falling edges in Fig. 3).

We approximate the coupled interconnect delay as a piecewise-quadratic function of input signal alignment. Table 2 gives the coefficients and the variance of the quadratic fits of the interconnect delay in Fig. 3.

4.3 Interconnect Delay Variation due to Varied Input Signal Alignment

Based on the piecewise-quadratic approximation of interconnect delay as a function of input signal alignment, we compute interconnect delay variation due to varied input signal alignment, and compare with SPICE Monte Carlo simulation results in Fig. 4.

As we showed in Section 2.3, *an interconnect delay distribution with normally distributed input signal arrival times may not be a normal distribution; the accuracy of approximating an interconnect delay distribution by a normal distribution depends on the variance of the input signal alignment, e.g., the "timing windows" of the input signals.* For small timing windows and large signal transition times, the input signal alignment is more likely to fall within a region of the piecewise-quadratic function (in Fig. 3) where an insignificant quadratic term is found, and the coupled interconnect delay is more likely to resemble a normal distribution. If the input signal alignment falls in more than one regions of the piecewise-quadratic function, e.g., for $T_r = 10ps$ in Fig. 4, the coupled interconnect delay distribution deviates from a normal distribution.

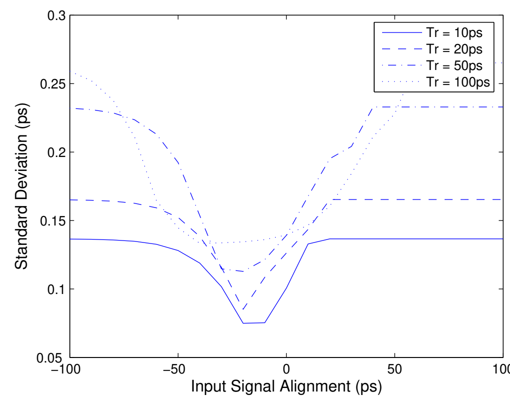

Figure 5: Interconnect delay standard deviation due to varied wire width as a function of input signal alignment for a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM. The transition times of two rising input signals are 10, 20, 50, or $100ps$. Wire width variation is in a normal distribution $N(0,0.1Width)$.

4.4 Wire Width Variation

We study the effect of wire width variation on coupled interconnect delay for each input signal alignment with a given signal transition time. We assume a 100% width correlation among local wire segments [15], and compute interconnect resistances and capacitances using closed form formulas [4] for normally distributed wire widths in SPICE Monte Carlo simulation. We ob-

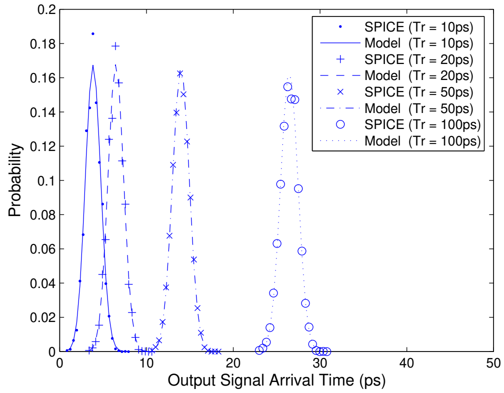

Figure 6: Output signal arrival time distribution for a pair of $1000\mu m$ coupled global interconnect in $70nm$ technolgy given by BPTM with the input signal arrival times in normal distributions $N(0, 6ps)$.

serve that *wire width variation induced interconnect delay variance is in a pulse function of input signal alignment* in Fig. 5, which differs with multiple input switching gate delay variance that is in a ramp function [2]. For input signals which take transitions in the same (opposite) direction(s), interconnect delay variance due to varied wire width decreases (increases) when crosstalk effect occurs.

We separate the effects of wire width variation with input signal alignment variation on coupled interconnect delay. Table 3 demonstrates that *results of our model based on superposition of the two effects match within* 1.96% *with SPICE Monte Carlo simulation results in the presence of wire width variation and input signal alignment variation.* This validates the superposition approach in the presence of independent variation sources.

We compare the impact of wire width variation in our proposed crosstalk aggressor alignment aware statistical delay calculation, and crosstalk aggressor alignment oblivious statistical delay calculation. In the latter case, we consider the worst case scenario, i.e., the maximum interconnect delay takes place when there is no crosstalk, and all coupling capacitors are grounded in our test case. Table 3 shows that *crosstalk aggressor alignment oblivious statistical delay calculation results in up to* 114.65% *mismatch in mean interconnect delay, and up to* 71.26% *underestimate in standard deviation of interconnect delay in this case.*

4.5 Output Signal Arrival Time Variation

We compare our computed output signal arrival time distribution with SPICE Monte Carlo simulation results for a typical BPTM global interconnect structure in Fig. 6.

We apply our model to a variety of input signal transition times and input signal arrival time deviations from 50, 100, to $200ps$. To cover different technology nodes, our test cases include (I) a pair of $1000\mu m$ coupled global interconnects in $70nm$ technology given by BPTM, and (II) a pair of coupled interconnects which are extracted from a $130nm$ industry design with 451 resistors and 1637 ground and coupling capacitors. We take a $2ps$ time step between two sampling input signal alignments, so that the number of delay calculation for different input signal alignment $N = MIN(1.5T_r, 6\sigma')/2$. We compare with 1000 SPICE Monte Carlo simulation runs. The results are shown in Table 4.

We observe that increased input signal arrival time deviations lead to increased interconnect delay and output signal arrival time

Table 3: The means (μ) and the standard deviations (σ) of interconnect delay (ps) (1) for fixed wire width and input signal arrival time, (2) with wire width variation, (3) with input signal alignment variation, (4) with both wire width and input signal alignment variations, (5) with wire width variation and grounded coupling capacitors (in crosstalk aggressor alignment oblivious delay calculation), all by SPICE Monte Carlo simulation, and (6) our model's estimates with both wire width and input signal alignment variations. Input signal transition times T_r are $10ps, 20ps$, or $50ps$. Mean input signal alignment $\mu' = -10ps, 0ps$, or $10ps$.

		(1)	(2)	(3)	(4)	(5)	(5) - (4)	(6)	(6) - (4)
$T_r = 10ps$		none	width	skew	both	w/o xtalk	%diff	model	%diff
$\mu' = -10$	μ	3.08	3.08	3.12	3.13	5.65	80.51	3.12	-0.64
	σ	-	0.08	0.37	0.38	0.17	-55.94	0.38	-0.10
$\mu' = 0$	μ	3.27	3.27	3.37	3.38	5.63	66.57	3.38	0.00
	σ	-	0.10	0.56	0.58	0.17	-71.26	0.57	-1.96
$\mu' = 10$	μ	5.00	5.00	4.85	4.85	5.64	16.29	4.85	-0.00
	σ	-	0.13	0.28	0.31	0.17	-47.01	0.31	-0.23
$T_r = 20ps$		none	width	skew	both	w/o xtalk	%diff	model	%diff
$\mu' = -10$	μ	2.92	2.92	3.12	3.14	6.52	114.65	3.12	-0.96
	σ	-	0.11	0.35	0.37	0.19	-47.51	0.37	1.29
$\mu' = 0$	μ	3.61	3.61	3.66	3.67	6.53	77.93	3.66	-0.00
	σ	-	0.13	0.45	0.47	0.19	-58.62	0.47	-0.99
$\mu' = 10$	μ	5.22	5.23	5.23	5.22	6.52	24.90	5.22	0.00
	σ	-	0.14	0.52	0.55	0.19	-64.96	0.54	-1.48
$T_r = 50ps$		none	width	skew	both	w/o xtalk	%diff	model	%diff
$\mu' = -10$	μ	3.44	3.44	3.45	3.46	7.19	108.38	3.45	-0.29
	σ	-	0.12	0.05	0.13	0.13	1.97	0.13	0.77
$\mu' = 0$	μ	3.68	3.68	3.70	3.71	7.19	93.80	3.70	-0.27
	σ	-	0.14	0.12	0.19	0.13	-27.91	0.18	-0.13
$\mu' = 10$	μ	4.22	4.22	4.26	4.27	7.18	68.15	4.27	-0.23
	σ	-	0.17	0.28	0.32	0.13	-58.70	0.32	-0.27

deviations; mean interconnect delay decreases with increased input signal transition time, because more input signal alignments bring crosstalk effect which reduces interconnect delay. *Over a variety of technology nodes, input signal transition times and arrival time deviations, our model gives the means and the standard deviations of output signal arrival times within* 2.09% *and* 3.38% *of SPICE Monte Carlo simulation results, respectively.*

5. CONCLUSION

Interconnect crosstalk brings significant timing uncertainty which must be taken into account in a statistical timing analyzer. In this paper, we studied interconnect delay as a function of input signal alignment and propose to approximate interconnect delay in a piecewise quadratic function. We present a closed form theoretical model which gives interconnect delay and output signal arrival time variation for given input signal arrival times in normal distributions. We include effects of independent variation sources, e.g., wire width variation, by superposition; and propose iterations in SSTA for pessimism reduction in the presence of crosstalk effect, similar to that in deterministic timing analysis. Our proposed method can be fitted into an existing SSTA tool, and runs in $O(N)$ time for a coupled interconnect, where N is the number of sampling input signal alignments; recalculation of interconnect delay requires constant time. The effect of multiple aggressors can be superposed due to the linearity of an RLC interconnect system. We verify our theoretical model

Table 4: The means (μ) and the standard deviations (σ) of interconnect delays and output signal arrival times (ps) for (I) a $1000\mu m$ interconnect of typical $70nm$ BPTM global structure and (II) a coupled interconnect extracted from a $130nm$ industry design with 451 resistors and 1637 ground and coupling capacitors. Input signal arrival time deviation 3σ and transition time T_r are $50ps$, $100ps$, or $200ps$.

input		delay				output					
3σ	$T_r(ps)$	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
(I) $70nm$		SPICE		Model		SPICE		Model		%diff	
50	50	3.83	0.85	3.82	0.83	29.44	16.25	29.67	16.65	0.78	2.46
50	100	3.39	0.16	3.41	0.12	53.77	16.33	53.70	16.65	-0.13	1.96
50	200	3.34	0.00	3.34	0.00	103.57	16.49	103.48	16.52	-0.09	0.18
100	50	4.59	1.23	4.59	1.19	30.44	32.87	30.97	33.48	1.74	1.86
100	100	3.82	0.92	3.84	0.83	54.75	32.85	55.58	33.96	1.52	3.38
100	200	3.35	0.07	3.38	0.04	103.94	32.91	104.23	33.63	0.28	2.19
200	50	5.30	1.18	5.25	1.14	31.43	65.97	31.69	66.17	0.83	0.30
200	100	4.70	1.34	4.64	1.25	56.04	65.91	56.91	66.58	1.55	1.02
200	200	3.78	0.96	3.78	0.82	105.18	65.90	106.30	66.99	1.06	1.65
(II) $130nm$		SPICE		Model		SPICE		Model		%diff	
50	50	4.29	0.16	4.31	0.16	29.53	16.40	29.41	16.52	-0.41	0.73
50	100	4.29	0.16	4.30	0.15	54.52	16.39	53.38	16.06	-2.09	-0.05
50	200	4.13	0.08	4.17	0.09	104.39	16.43	104.29	16.41	-0.10	-0.12
100	50	4.33	0.17	4.34	0.17	29.81	32.94	29.66	33.03	-0.50	0.27
100	100	4.30	0.18	4.30	0.17	54.76	32.89	54.12	32.95	-1.17	0.18
100	200	4.19	0.18	4.21	0.14	104.68	32.89	104.40	32.88	-0.27	-0.03
200	50	4.39	0.16	4.42	0.14	30.33	65.96	29.81	65.94	-1.71	-0.03
200	100	4.33	0.18	4.31	0.17	55.27	65.93	54.64	65.97	0.06	0.06
200	200	4.25	0.18	4.25	0.16	105.18	65.89	104.89	66.12	-0.28	0.35

by SPICE based Monte Carlo simulation on BPTM $70nm$ global interconnect structures and instances from $130nm$ technology industry test cases. Our experiments show that crosstalk aggressor alignment oblivious statistical delay calculation could lead to up to 114.65% (71.26%) mismatch of interconnect delay means (standard deviations); while our model gives output signal arrival times means (standard deviations) within 2.09% (3.38%) of SPICE Monte Carlo simulation results.

Our proposed method can be extended to include input signal transition time variation in interconnect delay variation analysis, e.g., by training, fitting, and probability computation with possible correlation consideration. Our ongoing research efforts include efficiency improvement and correlation analysis techniques in the presence of multiple variation sources.

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