

Fast and Efficient Phase Conflict Detection and Correction in Standard-Cell Layouts

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Abstract

Alternating-Aperture Phase Shift Masking (AAPSM), a form of strong Resolution Enhancement Technology (RET), will be used to image critical features on the polysilicon layer at smaller technology nodes. This technology imposes additional constraints on the layouts beyond traditional design rules. Of particular note is the requirement that all critical features be flanked by opposite-phase shifters, while the shifters obey minimum width and spacing requirements. A layout is called phase-assignable if it satisfies this requirement. Phase conflicts between shifters have to be removed to enable the use of AAPSM for layouts that are not phase-assignable. Previous work has sought to detect a suitable set of phase conflicts to be removed, as well as correct them as well as correct them.

This paper has two key contributions: (1) a new computationally efficient approach to detect a minimal set of phase conflicts, which when corrected will produce a phase-assignable layout; (2) a novel layout modification scheme for correcting these phase conflicts in standard-cell blocks. Unlike previous formulations of this problem, the proposed solution for the conflict detection problem does not frame it as a graph bipartization problem. Instead, a simpler and more computationally efficient reduction is proposed. This simplification greatly improves the runtime, while maintaining the same improvements in the quality of results. An average runtime speedup of 5.9x is achieved using the new flow. A new layout modification scheme for correcting phase conflicts in large standard-cell blocks is also proposed. The proposed layout modification scheme can handle all phase conflicts in large standard-cell blocks with small increases in area. Our experiments show that the percentage area increase for making typical standard-cell blocks phase-assignable ranges from 3.4-9.1%.

1 Introduction

As advanced technologies in wafer manufacturing push the patterning processes toward lower k_1 sub-wavelength printing, reticle based resolution enhancement techniques (RET) have played a critical enabling role. Alternating-Aperture Phase Shift Masking (AAPSM) is a form of strong RET that uses phase modulation at the mask level to enhance the resolution limit of current lithography equipment. At smaller technology nodes, it will be widely used to image features of the polysilicon layer. Among several variants of AAPSM, **Bright-Field** AAPSM is the most viable technology for the polysilicon layer [1]. In a simple model of Bright-Field AAPSM, each critical feature, which is a shape in the design whose width is below a certain threshold value, must be flanked by two phase shifters of opposing phases in order to create destructive interference between them. There are additional constraints of size and spacing that the shifters must obey in order to ensure a manufacturable mask.

Given a layout with shifters inserted around each critical feature, it is **phase-assignable** if and only if there is a phase-assignment solution which satisfies the following requirements:

1. Shifters on opposite sides of every critical feature are assigned opposite phases (0° and 180°); and

2. Shifters that are separated by less than the minimum required shifter spacing should be merged and assigned the same phase. Two shifters separated by less than the minimum shifter spacing will be referred to as **overlapping shifters**.

Two shifters are in **phase conflict** if they violate the above conditions in a phase assignment solution in which each shifter is assigned a phase. Figure 1 illustrates an example where the above conditions are violated by a cyclic sequence of shifters that cannot be properly mapped. The **Phase Conflict Detection Problem** seeks to find a minimum set of phase conflicts, which when corrected will result in a phase-assignable layout. The **Phase Conflict Correction Problem** corrects a given set of phase conflicts by layout/mask modification with minimum increases in area or mask complexity.

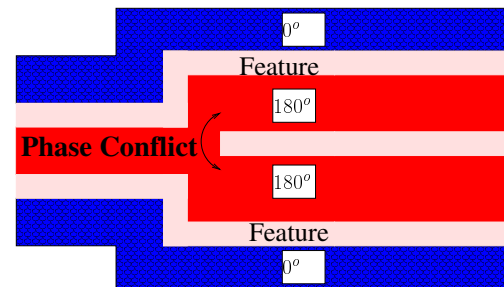


Figure 1. Example of Phase Conflict.

Our contributions are summarized as follows:

- A new and computationally efficient algorithm for detecting phase conflicts, which when corrected will render the given layout phase-assignable. Unlike all previous work in this area which reduces the detection problem to a graph bipartization problem, we formulate the conflict detection problem as a minimum-weight conflict cycle removal problem. This leads to a substantial reduction in the size of the constructed graphs and thereby produces significant runtime speedups averaging 5.9x over previous methods, while maintaining the same quality of results as the best results available today [2].
- A novel layout modification algorithm for correcting a selected set of phase conflicts that achieves small area increase and good scalability for large standard-cell blocks. Compared to the approach in [2], which presents the only available results on layout modification for correcting bright-field phase conflicts in standard-cell blocks, our new approach can reduce the maximum area increase from $>100.0\%$ to 9.1% for large designs.

The paper is organized as follows: Section 2 briefly reviews the previous work in phase conflict detection and correction. In Section 3, we provide a detailed discussion of the new theory underlying the proposed phase conflict detection flow. Section 4 discusses

our new phase conflict correction algorithm. Experimental results are presented in Section 5. We end with conclusions and directions for future work in Section 6. The proofs of all the theorems introduced in the paper are given in the Appendix.

2 Previous Work

The phase conflict detection problem is addressed in [2, 3, 4, 5, 6]. The basic underlying principle in these works is to translate the phase conflict detection problem to a graph bipartization problem of a suitably constructed graph. Thus, conflict detection would involve identifying a set of edges such that the modified graph obtained after deleting the edges is bipartite. The work in [5, 6] formulates the phase conflict detection problem as a minimum-weight graph bipartization problem to minimize the amount of layout modification necessary to render the layout phase-assignable. It is assumed that the constructed graphs will always be embedded planar graphs¹ and an optimal solution is provided for that case. The most recent work in this area is presented in [2]. This algorithm works on general layouts and is a generalization of the scheme presented in [6]. The layout is represented as a graph called the *phase conflict graph*. A new bipartization algorithm that does not require the graph constructed from the layout to be an embedded planar graph is proposed. The algorithm creates a planar sub-graph of the given graph, applies a computationally efficient version of the optimal bipartization algorithm [6] on the planar sub-graph to get an optimal solution and then combines this solution with a greedy solution for the edges deleted during planarization. The quality of results (in terms of number of conflicts selected for correction and runtime numbers) was significantly better than previous work in this area. This phase conflict detection algorithm will be used as our reference for comparison.

Previous work in phase conflict correction falls into two major categories. Mask modification based methods directly modify the mask to correct phase conflicts by introducing cuts in the shifters corresponding to the conflicts [7]. Since this solution can significantly complicate the mask creation process, there is a great deal of interest in layout modification based correction methods. Layout modification based approaches remove the conflicts by increasing spacing between features or widening critical features [2, 3, 4, 5, 6, 8, 9]. Most of these works focus on dark-field AAPSM². The first layout modification scheme for correcting bright-field phase conflicts for standard-cell blocks is presented in [2]. The key idea in this work is to add a minimal number of end-to-end spaces in the layouts to separate all shifter pairs corresponding to the phase conflicts by the desired spacing. While this technique is suitable for standard cells and some macro blocks with a relatively small number of conflicts, experimental results show that it is highly unsuitable for standard-cell blocks with a large number of phase conflicts for correction.

There are also some cell-based solutions that propose to add blank space around each cell to avoid introducing phase conflicts between neighboring cells or introduce an additional requirement that all the boundary elements should have the same phase [10]. No results are presented in the context of standard-cell blocks. However, we believe these methods are conservative and could lead to

¹An embedded planar graph is one that has no line crossings when embedded in a plane.

²In dark-field AAPSM, phases are assigned to the critical features themselves. This form of AAPSM is not likely to be used on the polysilicon layer.

unnecessary area increases since most phase conflicts between features of neighboring cells can be solved by using the correct phase assignment.

3 Proposed Phase Conflict Detection Scheme

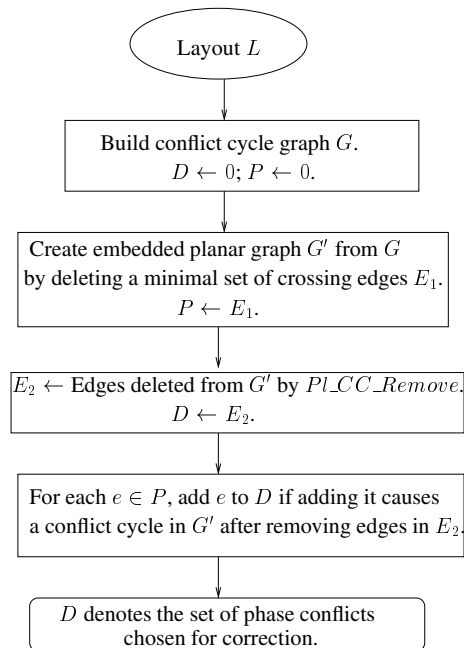


Figure 2. Phase Conflict Detection Flow.

In this section, the proposed phase conflict detection scheme is presented. The new conflict detection flow is shown in Figure 2. Unlike previous formulations of the problem, the proposed solution does not reduce the problem to a bipartization problem. Instead, the phase conflict detection problem is reduced to a new problem called the minimum-weight conflict cycle removal problem (the problem will be introduced formally in the next section). This new reduction enables the construction of a much leaner graph from the layout. The new graph, called the *conflict cycle graph (CCG)*, removes all superfluous edges that were introduced in previous graph representations that required the graphs to be bipartite for phase-assignable layouts. This simplification enables a significant reduction in the number of edges compared to previous representations, like the *phase conflict graph* [2]. An average reduction of 31% in the number of edges is achieved using the new graph.

A further advantage of this new formulation is that an optimal polynomial-time algorithm exists for the minimum-weight conflict cycle removal problem when the input graph is an embedded planar graph. The optimal algorithm, referred to as `PL_CC_Remove` in the third step of Figure 2, is used as a subroutine in the proposed phase conflict detection algorithm. The use of the optimal algorithm ensures that the quality of results returned by our phase conflict detection algorithm is comparable to the best results returned by previous work [2], since a substantially large planar sub-graph of the input graph is solved using the optimal algorithm.

In addition, the new theory enables the removal of certain edges that are marked undeletable and cannot be selected by the phase conflict detection algorithm. This results in substantial reductions in the size of some intermediate constructions. This combined with the fact that the layout is represented using a leaner graph

results in significant speed-ups of the phase conflict detection algorithm. Experimental results on representative examples show average speedups of 5.9x using the proposed approach, while maintaining the same quality of results as the method in [2].

To summarize, the key features that distinguish the proposed phase conflict detection scheme from previous methods are:

- Representation of the layout as a CCG (to be defined later) and the establishment of its relationship to phase-assignability of its corresponding layout.
- Reduction of the phase conflict detection problem to a minimum-weight conflict cycle problem (to be defined later) on the CCG and an optimal polynomial-time algorithm for the problem, when the CCG is an embedded planar graph.

Together, these two factors provide significant runtime advantages without sacrificing solution quality. The following sections include a detailed discussion of these items.

3.1 CCG Construction

The first step of the conflict detection algorithm is to build a **CCG**. Given a layout L , the **CCG** $G = (N, E \cup F)$ consists of shifter nodes N , conflict edges E and feature edges F .

1. For each shifter in L , create an edge shifter node $n \in N$.
2. For two overlapping shifters³ s_1 and s_2 , create a **conflict edge** $e \in E$ connecting n_1 and n_2 . Here n_1 and n_2 are the edge shifter nodes for s_1 and s_2 , respectively.
3. Create a **feature edge** $f \in F$ between the two shifters that are on opposite sides of a critical feature.

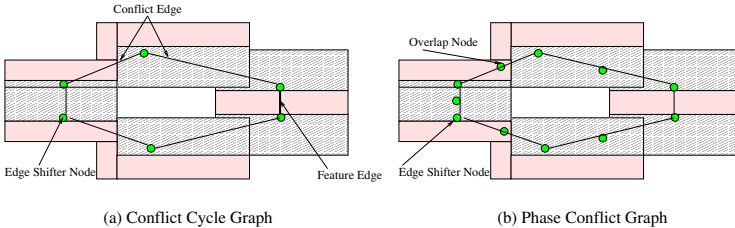


Figure 3. (a) CCG. (b) Phase Conflict Graph.

Figure 3(a) shows an example of a CCG for the layout shown earlier in Figure 1. The CCG has 6 nodes and 6 edges. By comparison, the phase conflict graph (shown in Figure 3(b)) of the same layout has 11 nodes and 11 edges. Experimental results in a later section show a substantial reduction in the edge count using the new graphs, which contributes to the runtime improvements. However, unlike the phase conflict graph, the CCG does not equate phase-assignability of its corresponding layout to bipartiteness. So, a CCG may be bipartite even though its corresponding layout is not phase-assignable. For instance, even though the layout in Figure 3(a) is not phase-assignable, its corresponding CCG is bipartite. Thus, a new criterion is needed for detecting phase conflicts using the CCG.

It should be further clarified that in the CCG, the feature edges and conflict edges play different roles: nodes connected by feature edges should be assigned different phases and nodes connected by conflict edges should be assigned the same phase. Later in this section, we discuss how the feature edges are used only to appropriately classify the cycles they belong to and can be dropped

³Two shifters that are separated by less than the minimum shifter spacing are called **overlapping shifters**.

during some intermediate graph constructions, thereby producing more speed-ups.

In the rest of this section, we present the theory for phase conflict detection using the CCG.

Definition 1 A **conflict cycle** is a cycle which contains an odd number of feature edges.

Theorem 1 A layout is phase-assignable if and only if the corresponding CCG has no conflict cycles.

Proof: See Appendix for proof.

In order to make the layout phase-assignable, it is necessary to remove all conflict cycles from the CCG by deleting edges. The deleted edges directly correspond to phase conflicts that have to be corrected. Each edge in the CCG can be assigned a weight to reflect the cost of correcting the phase conflict corresponding to it. A large cost of the phase conflicts selected for correction would imply large changes to the layout and/or mask, which is highly undesirable. Hence, it is essential to minimize the sum of weights of the edges to be deleted during conflict cycle removal.

The minimum-weight conflict cycle removal problem is defined as follows: Given a CCG $G = (V, E)$, remove a minimum-weight set of edges E' such that the modified graph $G' = (V, E \setminus E')$ does not have any conflict cycles.

It can be easily proved that this problem is NP-hard for general graphs by doing a simple reduction to the minimum-weight bipartization problem. However, an optimal polynomial-time algorithm exists when the graph is an embedded planar graph. This optimal algorithm is referred to as **PL_CC_Remove** in Figure 2 and will be discussed in detail in the next section.

3.2 Optimal Minimum-Weight Conflict Cycle Removal Algorithm

Let G denote a CCG that is also an embedded planar graph. The minimum-weight conflict cycle removal problem on G is reduced to a minimum-weight perfect matching problem on a suitably constructed graph \mathcal{G} through an intermediate reduction to an **T-join** problem [11].

Definition 2 A **conflict face** of G is a face corresponding to a conflict cycle in G . A face of G that is not a conflict face is a **legal face**.

Definition 3 The **dual graph** G^D of a CCG G is constructed by representing every face of G with a node in G^D . An edge e which belongs to faces g_1 and g_2 in G (whose corresponding nodes in G^D are v_1 and v_2 , respectively) is represented with an edge $e' = \{v_1, v_2\}$ in G^D . A node $v \in G^D$ corresponding to a conflict face $g \in G$ is called a **conflict node**. A node that is not a conflict node is a **legal node**.

Theorem 2 Removing an odd number of edges from every conflict face and an even number of edges from every legal face will generate a graph with no conflict cycles.

Proof: See Appendix for proof.

The problem of deleting a minimum-weight set of edges such that an odd number of edges are deleted from every conflict face and an even number of edges are deleted from every legal face of G translates to the following problem on its dual graph G^D :

Find the minimum-weight set of edges S to be deleted in $G^D = (V, E)$ such that: (a) an odd number of edges in S are incident on every conflict node $u \in V$; (b) an even number of edges in S are incident on every legal node $v \in V$.

This is exactly the same as the **T-join** problem on a graph which can be optimally solved. The **T-join** problem of a graph seeks a minimum-weight edge set S such that a node u is incident to an odd number of edges of S if and only if u belongs to the node subset T of the given graph. Our problem reduces to the **T-join** problem if the set of all conflict nodes in G^D is denoted as the set T . Unlike the reductions in [2] in which T is the set of all nodes with odd degrees, our set T may include nodes with odd or even degrees.

Next, we describe how our particular **T-join** problem can be reduced to a perfect matching problem on a suitably constructed gadget graph \mathcal{G} . Previous work [5] shows that the specific construction of the gadget graph can greatly impact the runtime of the perfect matching algorithm. The authors in [2] introduce a new gadget graph construction that provides speed-ups over previous work in this area. However, their gadget construction works only for the case when T denotes the set of odd-degree nodes.

Our gadget graph construction, henceforth referred to as *Construct_Gadget*, consists of the following steps:

1. Each node v in the dual graph G^D corresponds to a set of nodes in \mathcal{G} , which is denoted as G_v^4 . Each edge e connecting v and v' in the dual graph is arbitrarily assigned to either v or v' . If e is assigned to v , it will appear as a *true node* t_e^v in G_v . If e is not assigned to v , it will appear as *ghost node* g_e^v in G_v . The ghost nodes are not explicitly represented in \mathcal{G} but are merely pointers to their respective true nodes. The assignment is done according to the following rules:
 - (a) For each conflict node u , the parity of the number of ghost nodes in G_u is different from the parity of its node degree.
 - (b) For each legal node v , the parity of the number of ghost nodes in G_v is equal to the parity of its node degree.

It is easy to ensure that the conditions are always satisfied since it is always possible to turn a ghost node g_e^v into a true node t_e^v and add an additional edge of weight $w(e)$ between t_e^v and $t_e^{v'}$ to meet the parity requirement at the cost of increasing the node number in \mathcal{G} by one.

2. The nodes in G_v are connected to each other by weighted edges as follows:
 - (a) An edge of 0 weight is added between t_e^v and $t_{e'}$.
 - (b) An edge of weight $w(e')$ is added between t_e^v and $g_{e'}^v$.
 - (c) An edge of weight $w(e)$ is added between g_e^v and $t_{e'}$.
 - (d) An edge of weight $(w(e) + w(e'))$ is added between g_e^v and $g_{e'}$.

Figure 4 illustrates the construction of the gadget graph from the dual graph. Note that the assignment of the edges (indicated by edges pointing toward the node) follows the rules specified in Step 1 of the construction.

Theorem 3 *The T-join problem for a graph $G^D = (V, E, w, T)$, where T denotes the set of all conflict nodes in V , can be reduced to a minimum-weighted perfect matching on the gadget graph $\mathcal{G} = (V', E', w')$ constructed using Construct_Gadget.*

⁴ G_v is referred to as a gadget of v and hence \mathcal{G} which is a collection of G_v s is called a gadget graph.

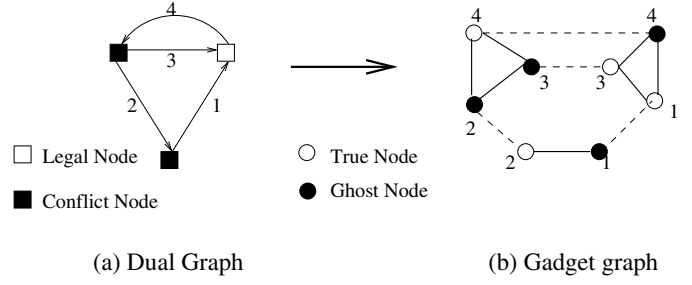


Figure 4. Gadget Graph Construction from Dual Graph.

Proof: See Appendix for proof.

The perfect matching problem can be optimally solved in polynomial time. In our implementation, the code of Cook and Rohe [12] is integrated.

It should be noted that using the proposed CCG and our particular T-join formulation implies that the classification of a face does not rely on its edge number. Therefore, further simplifications can be done on the dual graph, when it is converted to the gadget graph that is input to the perfect matching problem. For instance, feature edges are only needed to classify the faces as conflict faces or legal faces and can be dropped during the dual graph construction if they cannot be picked by the phase conflict detection algorithm (in the next section we discuss why this might be the case). This simplification results in a further reduction in the number of nodes and edges in the gadget graph \mathcal{G} without affecting the correctness of the above reductions. However, this simplification could not be done with the previous bipartite formulation in [5, 6, 2], which contributes to the increased complexity of their gadget graphs.

4 Proposed Phase Conflict Correction Algorithm

The primary task of AAPSM-specific layout modification is to correct the phase conflicts selected by the conflict detection algorithm. Phase conflicts can be corrected either by adding space between shifters corresponding to a conflict (equivalent to correcting a conflict edge) or by widening critical features (equivalent to correcting a feature edge). However, widening critical features may introduce significant timing problems and hence feature edges are not picked by the current conflict detection scheme. In this work, we assume that phase conflicts corresponding to conflict edges, that can be corrected by increasing the spacing between features such that their corresponding shifters are separated by the required shifter spacing, are the only ones being corrected.

It should be noted that merely increasing the spacing between the shifters corresponding to the phase conflict may cause DRC violations as well as introduce new phase conflicts as the relative locations of the neighboring features may change. The work presented in [2] solved this problem by adding end-to-end spaces throughout the layout. The spaces are inserted such that only the length of the polysilicon interconnect is increased. This technique could only be applied to standard cells and macro blocks with a low density of phase conflicts. Experiments indicate that this method when applied directly to standard-cell blocks can cause large increases in area.

Our layout modification algorithm exploits the fact that

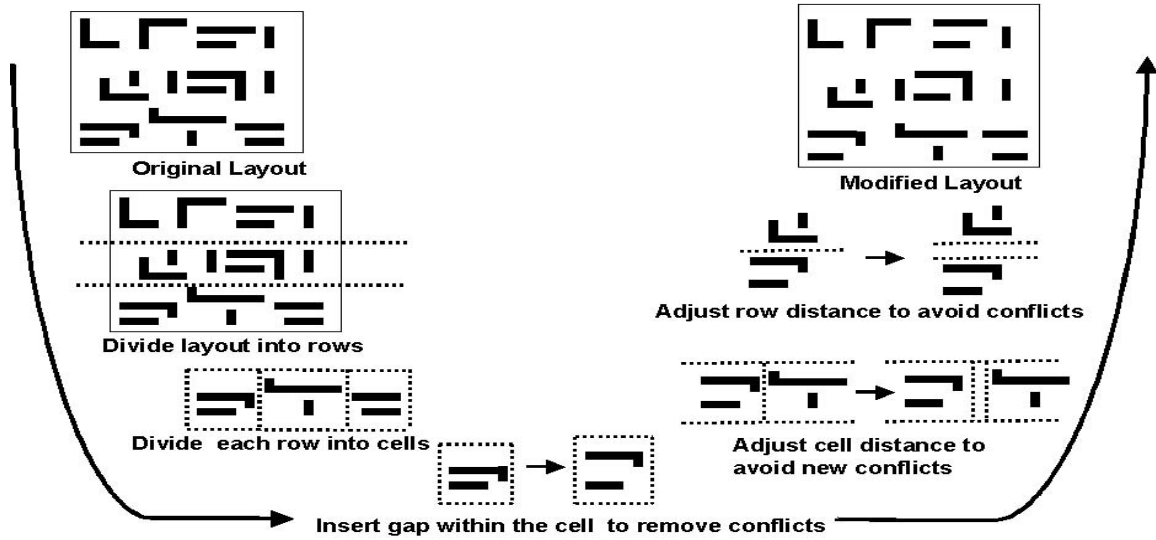


Figure 5. Details of Layout Modification Algorithm.

standard-cell blocks can be naturally partitioned into rows and that phase conflicts in each row can be corrected independently. The overall flow of the algorithm is presented in Figure 5. The algorithm consists of the following steps:

1. First the standard-cell block is partitioned into rows and its constituent cells. The rows are identified by the locations of the cell placement rows.
2. Next the phase conflicts that are strictly between features of a cell are corrected by adding a minimal number of end-to-end spaces in the cell. A minimum-weight set-covering problem (similar to the one proposed in [2]) is used to determine the locations and the widths of the end-to-end spaces. The vertical conflicts (i.e., conflicts corrected by adding vertical end-to-end spaces) are assigned a much lower weight than horizontal conflicts (i.e., conflicts corrected by adding horizontal end-to-end spaces), since it is less disruptive to increase the width of the standard cells than their height.
3. The modified cells in a row are now assembled such that no phase conflicts exist between any two features of adjacent cells. It is only necessary to check the features near the boundary of adjacent cells to determine the right amount of space to be added. The height of each row is equal to the height of the tallest cell (in reality, all the cells in the row are stretched to the new height) and the width is equal to the sum of the widths of the standard cell plus the widths of the inserted spaces between the standard cells. The spaces that are occupied by filler cells are made available at this step to avoid any unnecessary area increase.
4. The final step consists of assembling the modified rows. Here, again horizontal space is added only as needed. Space is added only if there is an existing conflict between features of cells on adjacent rows or if relative locations of the features in adjacent rows are changed from the original configuration (this can only happen if vertical space is added at different locations on adjacent rows).

Hence, in this algorithm, end-to-end spaces are only added within a cell. The spaces between the cells and between the rows

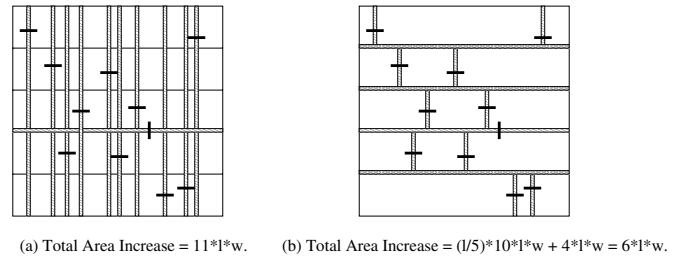


Figure 6. Comparing the area increases produced by the layout modification scheme in [2] with the proposed scheme.

are smartly managed such that no phase conflicts remain or are introduced after the changes to the individual cells. This results in much smaller area increases for correcting phase conflicts when compared to the method in [2].

Figure 6 compares our layout modification algorithm with the one presented in [2] on a hypothetical example. The layout is a square and is composed of 5 rows of standard cells. Let l denote the length of each side of the layout. The shaded rectangles denote the spaces added in the layout and the bold dark lines are used to represent the locations of the phase conflicts being corrected. Let w denotes the width of horizontal and vertical spaces added (assumed to be the same for simplicity). The area increase with the scheme in [2] is $11lw$, whereas the area increase with our scheme is only $6lw$.

The proposed layout modification algorithm can be applied as an additional processing step during post-placement optimizations used today. It should be noted that the relative locations of the pins are unchanged by these modifications. Furthermore, the inserted spaces are integer multiples of the M1 routing pitch. Hence, the modifications introduced by the proposed flow do not introduce any additional complications for the router. This is also a difference from the method in [2] that does not match the inserted spaces to the routing pitch. This solution needs to be applied even if the placement is done with phase-assignable standard cells, i.e. cells that have no phase conflicts. This is because phase conflicts

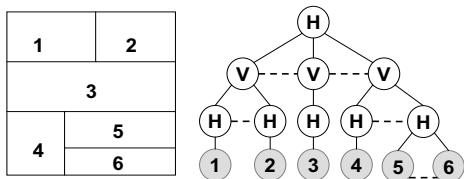


Figure 7. Hierarchical Layout and its Partition Tree.

can exist between features of neighboring cells. The only difference is that Step 2 of the layout modification algorithm may be omitted.

Our proposed algorithm can also be easily extended to correct phase conflicts in hierarchical layouts. As shown in Figure 7, a hierarchical layout can be represented using the *partition tree*, where each leaf node represent a layout region. The *H* (or *V*) node represents a region which is partitioned into several child regions using horizontal (or vertical) cut lines; there is a dashed line between any two neighboring child nodes which represents the cut line. The layout modification problem can be solved using a bottom-up algorithm. First, the phase conflicts are corrected within each leaf node by inserting end-to-end spaces. Then for each upper level, new phase conflicts are avoided by inserting gaps along the cut lines. The algorithm shown in Figure 5 is the special case when the input layout can be represented as a two-level tree.

5 Experimental Results

This section presents the experiments we conducted to test the benefits of the proposed ideas. The experiments were run on a 4X400 Mhz Ultra-Sparc II with 4.0 GB of RAM. The examples are 90 nm designs and were generated using a commercial place and route tool. Typical values of threshold width for critical features, shifter dimensions and shifter spacing were used in the experiments. This work focuses mainly on phase conflicts that can be corrected by increasing the spacing between features in the layout. Thus, phase conflicts caused by T-shapes are not handled. These can be corrected by feature widening or mask splitting [7]. Phase conflicts caused by local line-end conflicts between neighboring features are also not considered as they can be efficiently detected and corrected during layout generation [13].

5.1 Phase Conflict Detection Results

Table 1 compares the runtime and the quality of results (number of edges deleted, or in other words, number of phase conflicts selected for correction) of the proposed method with other state-of-the-art approaches. The conflict detection method presented in [2] is our main comparison point since their results are best in terms of the number of phase conflicts chosen for correction and runtimes, when compared to other state-of-the-art approaches [5, 6]. Columns 1 and 2 give the design names and design statistics (like number of polygons and number of shifter overlaps), respectively. The results obtained after applying the method in [2] are grouped under the sub-heading *Bipartization Method in [2]*. The results obtained using our phase conflict detection method are grouped under *Proposed Method*. Columns *Runtime(5)* and *Runtime(9)* compare the runtimes (in seconds) of the method in [2] and our proposed method, respectively⁵. The results indicate that our runtimes are

⁵It should be noted that only the time spent in solving the perfect matching problem is reported in both cases as this is the most compute-intensive portion of

significantly better than those obtained using the method in [2]. An average improvement of 5.9x is obtained. This can be primarily attributed to a significant reduction in the number of edges in the CCG compared to the phase conflict graph [2] (the numbers are shown in Columns *#edges(3)* and *#edges(7)*) and the removal of undeletable edges (in our case, feature edges) during intermediate graph constructions. These two factors together produced a significant reduction in the number of nodes and edges of the gadget graph constructed during perfect matching, when compared to the ones constructed in [2] (the numbers are shown in *#nodes/edges GG(4)* and *#nodes/edges GG(8)*). This accounts for the speedups obtained by the proposed method. We believe these runtime advantages will be more pronounced in larger designs.

The table also shows that the quality of our results (in terms on number of phase conflicts chosen for correction) is better than the results obtained using the method in [2] (Column *#Conflicts(6)* shows the results obtained using the method in [2] and Column *#Conflicts(10)* shows the results obtained with our method). This improvement is primarily due to the fact that the number of edges deleted during planarization of the CCG (second step in Figure 2) is smaller since there are fewer edges in the CCG. Hence, the optimal algorithm can be applied to a larger sub-graph of the original graph.

5.2 Phase Conflict Correction Results

Table 2 reports the results of using the proposed layout modification scheme for correcting the phase conflicts chosen by the detection step on the same layouts. Column *Area* reports the area of the designs in square microns. Column *Conflict* specifies the number of phase conflicts selected for correction by the detection algorithm for each design (the numbers are slightly different from the number of conflicts in Table 1 for each design due to the use of different weighting schemes). Column *Outside* provides the number of phase conflicts that are selected for correction and occur between features of neighboring cells. The results indicate that these conflicts account for a small fraction of the total number of phase conflicts in any design. This strengthens our view that it might be too conservative to leave blank space around all the cells or force the boundary features of each cell to have the same phase and could cause unnecessary area increases. The fifth column (*% Area Inc.*) reports the percentage area increase for these layouts as a result of the added spaces. The area increase for these layouts ranges from 3.4-9.1%, with an average increase of 6.3%. The area increase goes up slightly with the size of the layout. For comparison, the layout increase caused by the method in [2] is also reported in the last column (*% Area Inc. [2]*). The numbers indicate the area increases caused by the method proposed in [2] are indeed very large, thereby making it unsuitable for large industrial designs.

6 Conclusions

A new theory for Bright-Field phase conflict detection was presented in this paper. The proposed method enabled the representation of the layout using a significantly leaner graph called the conflict cycle graph (CCG). The phase conflict detection method was reduced to a new problem called the minimum-weight conflict cycle removal problem. An optimal algorithm for solving the

the algorithm. The gadget graph construction was also sped-up by 2x using the new graph, but the perfect matching times has a greater contribution to the total run-time.

Design(1)	# Plgns/#Shft Ovlps(2)	Bipartization Method in [2]				Proposed Method			
		#edges(3)	#nodes/#edges GG(4)	Runtime (5)	# Conflicts (6)	#edges(7)	#nodes/#edges GG(8)	Runtime(9)	# Conflicts(10)
Design1	10274/24580	84508	46756/153291	2.53	631	59939	15562/26943	0.38	624
Design2	13630/32257	112599	62480/203971	1.90	963	79672	20910/36403	0.22	946
Design3	21868/53749	182809	103912/338810	3.33	1558	128836	34806/61227	0.55	1534
Design4	20425/50059	173319	98834/320499	3.18	1678	121546	33266/57705	0.48	1664
Design5	25784/63760	216691	122324/397999	3.87	1854	152655	40614/70853	0.60	1839
Design6	48787/157668	484999	355760/1147057	12.17	6330	325769	126112/231717	2.78	5989
Design7	44121/142707	436297	339538/1084677	12.30	5010	295001	112152/207784	2.47	4865
Design8	72101/237557	729980	567532/1817272	20.05	10275	489922	189986/351007	4.23	9631
Design9	105882/376707	1133279	949064/2997548	41.35	18148	757581	303408/565217	7.95	17463
Design10	159070/552767	1667581	1415620/4437522	66.40	27308	1115928	444082/829898	11.58	26354

Table 1. Phase Conflict Detection Results.

Design	Area	Conflict	Outside	% Area Inc.	% Area Inc. [2]
Design1	25173.96	641	148	3.4	18.1
Design2	16397.82	995	197	5.4	23.1
Design3	31416.21	1589	284	5.8	26.8
Design4	25715.23	1724	238	6.1	28.8
Design5	40409.68	1720	322	4.7	32.12
Design6	61705.52	6257	770	5.8	57.47
Design7	58414.06	5100	586	6.1	59.1
Design8	94178.09	10141	512	7.3	80.2
Design9	148231.77	18657	2672	9.1	>100.0
Design10	249210.41	28121	4224	9.0	>100.0

Table 2. Layout Modification Results for Standard-Cell Blocks.

minimum-weight conflict cycle removal problem in CCGs that are embedded planar graphs was also presented. The optimal algorithm was used as a sub-routine within the conflict detection algorithm so that a minimal solution could be obtained for non-planar CCGs. Supporting experimental results illustrated significant improvements in the runtime (average runtime improvement of 5.9x), while maintaining the same quality of results (in terms of number of phase conflicts chosen for correction) as the best available previous work in this area.

A novel layout modification algorithm for making standard-cell blocks phase-assignable was also presented. Experimental results confirm that the new method produced much smaller increases in area than previous work in this area. The small area increases produced by the proposed method (average area increase of 6.3%) make it practical for use as a post-placement optimization step. It can also be applied to attain phase-assignability of standard-cell blocks done with phase-assignable standard cells. The proposed layout modification method can be extended to allow feature widening for certain phase conflicts that cannot be corrected by increasing the spacing between features. Another possible extension of this work would be to integrate with a timing engine to make the layout modifications more timing-aware.

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APPENDIX

Theorem 1 A layout is phase-assignable if and only if the corresponding CCG has no conflict cycles.

Proof: (→) Assume L is phase-assignable. Let all the edge shifter nodes be colored with the same phases as the shifters in L . It is true that the node colorings of G satisfy the following two conditions: nodes connected by a feature edge have different colors and nodes connected by a conflict edge have the same color. Let us assume further that there exists a conflict cycle C and let $\{n_1, n_2, \dots, n_k, n_1\}$ be a closed walk along C . By the definition of a conflict cycle, there are an odd number of feature edges in

C . Hence, starting from n_1 , the node phases will flip an odd number of times in C . Therefore, the node n_1 will be assigned two different phases, which is impossible. Hence our assumption that G , whose corresponding layout L is phase-assignable, has a conflict cycle is wrong.

(\leftarrow) Assume G does not contain any conflict cycles. WLOG, assume G is connected (if G is not connected, the proof can be done for each of connected components of G). Assume further that L is not phase-assignable. Then, there exists at least two shifters s_1 and s_2 that do not satisfy the conditions for phase assignment. Let n_1 and n_2 be the edge shifter nodes corresponding to s_1 and s_2 , respectively. Let the edge connecting them be denoted as e . Let C be a cycle that contains e and let n_0 be an intermediate node in C (any node other than n_1 and n_2).

There are two possible cases:

1. Shifters s_1 and s_2 are on opposite sides of a critical feature and have same color: Since the phases are only changed across feature edges, if n_1 has the same phase as n_0 , then there must be an even number of feature edges from n_0 to n_1 . By assumption, n_2 has the same phase as n_1 , and hence as n_0 . Thus, there must be an even number of feature edges from n_0 to n_2 . Then, C must contain an odd number of feature edges and hence C is a conflict cycle.
2. Overlapping shifters s_1 and s_2 have different colors: If n_1 and n_0 have the same phase, then there must be an even number of feature edges on the path from n_1 to n_0 . By assumption, n_2 has an opposite phase from n_1 and hence an opposite phase from n_0 . Thus, the path from n_0 to n_2 must have an odd number of feature edges. Hence C must contain an odd number of feature edges and hence C is a conflict cycle.

This contradicts our initial assumption that G has no conflict cycles. Hence, our assumption that L is not phase-assignable is wrong. \square

Definition 4 Two faces are **neighboring faces** if they share at least one common edge.

Definition 5 Two neighboring faces can form a **merged face** by deleting at least one common edge.

Lemma 1 The parity of the number of feature edges of the merged face of two neighboring faces is equal to the parity of the sum of the numbers of feature edges of two faces.

Proof: Let the two faces have m_1 and m_2 feature edges and they share m_3 feature edges. Then the merged face has $m_1 + m_2 - 2m_3$ feature edges, which has the same parity as $m_1 + m_2$. \square

Lemma 2 A planar embedded graph G has no conflict cycles if and only if all faces are legal.

Proof: For a planar embedded graph, any cycle is the result of merging n faces. If all faces are legal, we know that the number of feature edges in the merged face is even from Lemma 1. Therefore, by definition, the graph has no conflict cycles. It is obvious that if the original graph has no conflict cycles, then every face is legal (by definition). \square



Figure 8. Deleting all common edges (in this case, only one) results in a merged face.

Theorem 2 Removing an odd number of edges from every conflict face and an even number of edges from every legal face will generate a graph with no conflict cycles.

Proof: Assume that an odd number of edges are removed from all conflict faces and an even number of edges are removed from every legal face of

G . As shown in Figure 8, the deletion of one or more common edges results in the creation of a merged face. Let G' be the graph obtained after the edge deletion. Any face in G' must be the result of merging a set S of faces in G . Let $S = S_1 \cup S_2$, where S_1 is the set of all conflict faces in S and S_2 is the set of all legal faces in S . The sum of the numbers of deleted edges of all the faces in S must be even, since any deleted edge belongs to two faces of S and is counted twice. The sum of the numbers of deleted edges of all the faces in S_2 is even since an even number of edges are removed from any legal face. Hence, the sum of the numbers of deleted edges of all the faces in S_1 should also be even. Since an odd number of edges are removed from any conflict face, the number of faces in S_1 must be even. Thus, the sum of the numbers of feature edges of all the faces in S_1 is even. It is obvious that the sum of the numbers of feature edges of all the faces in S_2 is even since every legal face has an even number of feature edges. Therefore, the sum of the numbers of feature edges of all the faces in S is even. By Lemma 1, the number of feature edges of the merged face is also even. So the merged face is legal. This is true of any face in G' . Thus, G' has no conflict cycles (Lemma 2). \square

Theorem 3 The **T-join** problem for a graph $G^D = (V, E, w, T)$, where T denotes the set of all conflict nodes in V , can be reduced to a minimum-weighted perfect matching on the gadget graph $\mathcal{G} = (V', E', w')$, constructed using Algorithm ConstructGadget.

Proof: (\rightarrow) Mapping perfect matching solution of the gadget graph \mathcal{G} to a valid solution of the **T-join** problem on G^D : For any node $v \in G^D$ whose gadget is G_v ,

1. If t_e^v is matched within G_v , $e \in S$;
2. If t_e^v is not matched within G_v , then $e \notin S$;
3. If g_e^v is matched within G_v , then $e \notin S$;
4. If g_e^v is not matched within G_v , then $e \in S$;

The set S thus constructed is a valid solution to the **T-join** problem. Assume a ghost nodes are matched within G_v , b ghost nodes are not matched with G_v , c true nodes are matched within G_v and d true nodes are not matched within G_v . In any perfect matching solution, the number of nodes matched within G_v , $(a + c)$, is even. The parity of $(a + b)$ is the same as the parity of $(a + b + a + c)$, whose parity is the same as the parity of $(b + c)$. Here, $(b + c)$ is the number of edges $\notin S$ and $(a + b)$ is the number of ghost nodes in G_v . For conflict nodes, we require that the parity of the number of ghost nodes in G_v , $(a + b)$, to be different from the parity of the node degree. Therefore, the parity of the number of edges $\notin S$, $(b + c)$, is also different from the parity of the node degree. Hence, the number of edges $\in S$ is odd for a conflict node. Similarly, it can be shown that for legal node, the number of edges $\in S$ is even. Therefore, the solution S is a valid solution of the **T-join** problem.

(\leftarrow) Mapping a solution S of the **T-join** problem to a solution of the perfect matching problem of \mathcal{G} can be done as follows: For any node v in the dual graph G^D , divide the edges connecting node v into four sets:

- $S_1 = \{e | g_e^v \in G_v \text{ and } e \in S\}$.
- $S_2 = \{e | g_e^v \in G_v \text{ and } e \notin S\}$.
- $S_3 = \{e | t_e^v \in G_v \text{ and } e \notin S\}$.
- $S_4 = \{e | t_e^v \in G_v \text{ and } e \in S\}$.

Let the cardinality of S_1 , S_2 , S_3 and S_4 be a , b , c and d , respectively. The a ghost nodes and the c true nodes are matched within G_v and the remaining nodes are matched outside G_v . Since S is a valid solution of the **T-join** problem, the parity of $(b + c)$ is the same as the parity of the number of ghost nodes $(a + b)$ (by construction). Thus, $((a + b) + (b + c)) = (a + c) + 2b$ is even. Hence, $(a + c)$ is even, which is the number of nodes to be matched within G_v . This is always possible since G_v is a complete graph. \square