Supply Voltage Degradation Aware Analytical Placement *

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Abstract

Increasingly significant power/ground supply voltage degradation in nanometer VLSI designs leads to system performance degradation and even malfunction. Existing techniques focus on design and optimization of power/ground supply networks. In this paper, we propose supply voltage degradation aware placement, e.g., to reduce maximum supply voltage degradation by relocation of supply current sources. We represent supply voltage degradation at a P/G node as a function of supply currents and effective impedances (i.e., effective resistances in DC analysis) in a P/G network, and integrate supply voltage degradation in an analytical placement objective. For scalability and efficiency improvement, we apply random-walk, graph contraction and interpolation techniques to obtain effective resistances. Our experimental results show an average 20.9% improvement of worst-case voltage degradation and 11.7% improvement of average voltage degradation with only 4.3% wirelength increase.

1 Introduction

Nanometer VLSI designs observe increased voltage drop along power supply networks because (1) shrinking layout feature sizes lead to increased interconnect resistance, (2) increasing device density leads to increased supply current, and (3) higher clock frequency leads to more significant inductance effect which brings additional supply voltage drop. On the other hand, decreased supply voltage approaches transistor threshold voltage and leaves a smaller noise margin for signal transition, which makes a transistor more vulnerable to supply voltage degradation. Less severe supply voltage degradation still leads to transistor performance degradation, e.g., a 10% supply voltage degradation could be responsible for 10% performance degradation, and the effect is super-linear [22]. Therefore, power/ground (P/G) supply networks in nanometer VLSI systems must be carefully designed to guarantee supply signal integrity.

A P/G supply network can be modeled as a distributed RLC netlist and characterized by interconnect model order reduction techniques [17, 16]. However, P/G networks are unique in their non-tree topology, large instance sizes, numerous voltage/current sources and observation points (output nodes), which bring tremendous efficiency and scalability challenges for application of conventional interconnect analysis techniques [19, 26]. For efficiency and scalability improvement, P/G network analysis techniques include random walk [19], multigrid-like [13, 14], and hierarchical [25] approaches. Random walk exploits locality of AC supply voltage drop, gives better scalability, and is ideal for parallel computing.

There are three types of supply voltage degradation: (1) DC IR drop, which is observed when a P/G supply network is modeled as a resistive network with DC supply current sources; (2) AC IR drop, which appears in a RC P/G network with AC supply current sources; and (3) LdI/dt supply voltage drop due to inductive effect. Correspondingly, P/G network optimization techniques include: (1) wiresizing or edge augmentation of a P/G network for reduced interconnect resistance or supply current along a supply current path, and (2) adding large decoupling capacitors close to supply voltage degradation hot spots, which serve as "charge reservoirs" and form shortcut supply current paths (hence reduce supply voltage drop). For high frequency designs, a number of decoupling capacitors need to be added at different P/G network hierarchy levels to cancel inductance effect and lower P/G network impedance over a wide range of frequency [18]. Supply voltage degradation can also be reduced by (1) circuit detuning for reduced simultaneous supply current, and (2) placement or P/G supply pad allocation [24] which moves large supply current modules closer to P/G supply pads or to be more evenly distributed.

Certain placement and floorplanning related techniques have been proposed for supply voltage reduction. Local placement adjustment helps decoupling capacitor insertion which is limited by available empty space in a placement

*Work partially supported by the MARCO Gigascale Systems Research Center and NSF MIP-9987678. A. B. Kahng is currently with Blaze DFM, Inc., Sunnyvale, CA 94089

[21, 27]. Mixed integer linear programming is proposed for finding the locations of P/G supply pads [24]. Network flow is proposed for P/G supply network construction and supply voltage degradation is included in a floorplan objective [4]. However, to the best of our knowledge, no supply voltage degradation reduction placement technique is presented.

In this work, we propose supply voltage degradation aware placement, e.g., relocating supply current sources for maximum supply voltage drop reduction. Our contributions are as follows.

1. We represent supply voltage degradation at a P/G node as a function of supply currents effective impedances in a P/G network. For DC IR drop analysis, we apply random walk, graph contraction and interpolation techniques for efficiency improvement in finding effective resistances.
2. We present greedy algorithms which achieve optimum placement with minimized supply voltage degradation at a given node or minimized total supply voltage degradation over all P/G nodes. We also show that it is NP-hard to find a placement which minimizes maximum supply voltage degradation.
3. We propose supply voltage degradation aware placement, by integrating the supply voltage degradation metric in an analytical placement objective via a smooth approximation function that enables differentiation of the maximum function.

We test our method on two industry designs with respect to voltage degradation, placed wirelength and runtime criteria. Our experimental results show an average 20.9% improvement of worst-case voltage degradation and 11.7% improvement of average voltage degradation, with only 4.3% wirelength increase.

The rest of this paper is organized as follows. We introduce motivations and problem formulation in Section 2, and present theoretical analysis on placement for supply voltage drop reduction in Section 3. We introduce an analytical placer and its integration with supply voltage drop reduction in Section 4. Our experimental results are presented in Section 5, and we conclude in Section 6.

2 Problem Formulation

A P/G supply network connects P/G supply sources (pads) to active devices which draw supply currents as signal transitions occur, and cause supply voltage degradation at active devices, due to the inherent resistance and inductance of the P/G supply network. We model a P/G supply network as an RLC interconnect, with P/G sources modelled as DC voltage sources, and active devices modelled as time-varying current sources which inject worst-case supply currents (e.g., "maximum current envelopes" [2]). Such a worst-case supply current waveform comes from simulation [1], a special tool [2], or static timing analysis (e.g., through worst-case slew rate and arrival "timing window" report).

Existing supply voltage drop reduction techniques focus on optimization of P/G supply network designs, e.g., by wiresizing, edge augmentation, and decoupling capacitor insertion. However, supply voltage degradation occurs not only due to a poor P/G supply network design, but also due to unexpected large supply currents at specific time steps and specific locations, which suggests application of circuit design and placement techniques for supply voltage degradation reduction. For example, circuit de-tuning spreads the supply currents in the time domain to reduce the maximum supply current at a particular time step.

We now explore placement techniques for supply voltage degradation reduction, e.g., by relocating current sources to achieve reduced worst-case supply voltage drop, without significant loss of placement quality in terms of existing placement metrics such as wirelength, area and timing.

Problem 1 *Given a routed P/G supply network, and worst-case supply currents for each component, find a placement with reduced supply voltage degradation while maintaining comparable placement wirelength, area, and timing performance.*

We study DC supply voltage degradation in this paper. A DC supply current can serve as a bound for an AC supply current, or, an *a priori* bound for a supply current which varies with placement due to wirelength difference.[1] Our technique can be extended to time domain transient analysis, by finding a placement which minimizes the maximum supply voltage degradation over all time steps.

We will use the following notation.

- (i, j) = edge between nodes i and j
- E = set of edges in a P/G network
- T_i = subtree which is rooted at node i
- $P(i, j)$ = path between nodes i and j in a tree
- $R_{i,j}$ = resistance between nodes i and j
- I_i = supply current at node i
- $V_{drop}(i)$ = supply voltage degradation at node i
- $Z(i, j)$ = effective impedance for a current source at node i and an observation node j
- $R(i, j)$ = effective resistance for a current source at node i and an observation node j
- G = the conductance matrix
- V = the node voltage vector
- I = the source current vector

[1] Alternatively, wirelength estimation can be included in supply voltage analysis during placement.

3 Analysis and Observations

In this section, we present supply voltage degradation as a function of supply currents, and study the problem of locating the supply current sources (cells) to minimize supply voltage degradation. We present greedy algorithms which achieve optimum placement with minimized total supply voltage degradation over all P/G nodes or minimized supply voltage degradation at a given P/G node, and demonstrate that it is NP-hard to achieve a placement with minimized maximum supply voltage degradation. We integrate the proposed supply voltage degradation metric in an analytic placement objective in Section 4.

3.1 P/G Network in a Tree Structure

For a given resistive tree-structure P/G supply network with DC supply current sources at each node, finding supply voltage degradation resembles Elmore delay calculation. I.e., by replacing ground capacitances by current sources:

$$\begin{aligned} V_{drop}(t) &= \sum_{(i,j)\in P(s,t)} R_{i,j}(\sum_{k\in T_j} I_k) \\ &= \sum_{k\in T_s} R(k,t)I_k \\ R(k,t) &= \sum_{(i,j)\in P(s,t)\cap P(s,k)} R_{i,j} \end{aligned} \quad (1)$$

where a P/G supply pad s is the root of the P/G supply tree, $P(s,t)$ is the path in the tree between node s and node t, each edge (i,j) has a resistance of $R_{i,j}$, each node has a supply current of I_k, and T_j is the subtree rooted at node j.

Problem 2 *For a given resistive tree-structure P/G supply network, locate the DC supply current sources, such that*
(a) the maximum supply voltage drop,
(b) the total supply voltage drop, or
(c) supply voltage drop at a given node
is minimized.

Observation 1 *The minimized maximum supply voltage drop placement (Problem 2(a)) with a tree-structure P/G network keeps a partial ordering, i.e., a node has current no larger than that of its parent node,*

$$i \in T_j \Rightarrow I_i \leq I_j \quad (2)$$

For the case of a single P/G supply line, the optimal placement strategy is to greedily locate the largest supply current source closest to the P/G supply source. In the presence of a branch in the P/G network, optimal placement implies a partition, i.e., to partition supply current sources I_t into two sets, with weights of path resistance $\sum_{(i,j)\in P(s,t)} R_{ij}$ from the source s to each child node t of the branching point, which is NP-hard.

Observation 2 *It is NP-hard to find a placement which minimizes the maximum voltage degradation in a tree-structure P/G supply network (Problem 2(a)).*

3.2 P/G Network in a General Structure

In a general-structure P/G network, each current source k contributes to voltage drop at node t as follows:

$$V(t) = \sum_k Z(k,t)I_k \quad (3)$$

where $Z(k,t)$ is the effective impedance for a current source at node k to inject a noise voltage at node t.

Problem 3 *For a given P/G supply network, locate the supply current sources, such that*
(a) the maximum supply voltage drop,
(b) the total supply voltage drop, or
(c) supply voltage drop at a given node
is minimized.

We propose two greedy algorithms for assigning effective resistances to current sources to optimize the total supply voltage degradation or the supply voltage degradation at a given P/G network node.

Observation 3 *The optimum placement which minimizes the total supply voltage drop in a P/G supply network (Problem 3(b)) is given by a greedy algorithm, i.e., by locating a large current I_k to have a small impedance $\sum_t Z(k,t)$.*

Observation 4 *The optimum placement which minimizes the voltage drop at a given node t in a P/G supply network (Problem 3(c)) is given by a greedy algorithm, i.e., by locating a large current I_k to have a small impedance $Z(k,t)$.*

3.3 Finding an Effective Resistance

An effective impedance $Z(k,t)$ (or, resistance $R(k,t)$ in a purely resistive P/G network) is given by the voltage at node t when the P/G network is driven by a single unit source current at node k. Direct modified nodal analysis gives effective resistance as

$$\begin{aligned} GV &= I \\ V &= G^{-1}I \end{aligned} \quad (4)$$

where G is the conductance matrix, V is the voltage vector, I is the current source vector, and $G^{-1}(k,t)$ gives $R(k,t)$. Matrix inversion has $O(n^3)$ time complexity and is not feasible for practical P/G networks. For better efficiency, we propose to compute $R(k,t)$ by random walk. If we construct two random walk paths that respectively start from nodes k and t and end at a supply pad, then $R(k,t)$ is given

by the resistance of the common part of the two paths, as in a tree-structure supply network. A random walk path is generated with the following transition probability from node p to node q

$$Prob(p,q) = \frac{R_{p,q}^{-1}}{\sum_{(p,i)\in E} R_{p,i}^{-1}} \quad (5)$$

so that a random walk path follows the corresponding current distribution probability. Averaging over a large number of probabilistic instances gives increased accuracy.

For scalability and efficiency improvement, we also apply multi-grid and interpolation techniques. We contract a P/G netlist by merging nodes and computing parallel resistances. Resistances are computed directly for a subset of the nodes, while resistances at the other nodes are computed by interpolation. Note that interpolation is applicable for resistance computation, because effective resistance of a node is bounded by those of its neighboring nodes, even though its voltage may not be bounded by those of its neighboring nodes.

4 Voltage Degradation Aware Placement

We now propose supply voltage degradation aware placement based on the analyses and observations of Section 3. We propose a hybrid analytical placement objective which includes supply voltage degradation in a smooth approximation function, and discuss implementation details.

4.1 Introduction of Analytical Placement

Analytical placement methods have received increased attention from both academia and industry in recent years [6, 7, 8, 11, 15, 23]. Specifically, recent work has implemented *APlace*, a general analytic placement framework [9, 11, 12], which has high solution quality and strong extensibility. In this section, we briefly introduce the APlace analytic placement framework, which forms the foundation of our proposed voltage degradation aware placement.

APlace takes global placement as a *constrained nonlinear optimization problem*: e.g., to minimize total half-perimeter wirelength (HPWL) while maintaining an equalized module area in each global cell. A formal problem formulation is as follows:

$$\begin{array}{ll} min & HPWL(\mathbf{x},\mathbf{y}) \\ s.t. & D_g(\mathbf{x},\mathbf{y}) = D \quad \text{for each global cell } g \end{array} \quad (6)$$

where $(\mathbf{x},\mathbf{y})$ is the center coordinates of modules, $HPWL(\mathbf{x},\mathbf{y})$ is the total HPWL of the current placement, $D_g(\mathbf{x},\mathbf{y})$ is a density function that equals the total module area in a global cell g, and D is the average module area over all global cells.

APlace applies smooth approximations of the HPWL and density functions and solves the constrained optimization problem in Eqn. 6 using the simple *quadratic penalty method*. I.e., the placer solves a sequence of unconstrained minimization problems of the form

$$min \quad HPWL(\mathbf{x},\mathbf{y}) + \tfrac{1}{2\mu}\textstyle\sum_g (D_g(\mathbf{x},\mathbf{y}) - D)^2 \quad (7)$$

for a sequence of values $\mu = \mu_k \downarrow 0$ and use the solution of the previous unconstrained problem as an initial guess for the next one. A *Conjugate Gradient* (CG) solver is employed to optimize for the objective function in Eqn. 7. The conjugate gradient method is quite useful in finding an unconstrained minimum of a high-dimensional function. Also the memory required is only linear in the problem size, which makes it adaptable to large-scale placement problems. The general APlace framework has been extended to address a variety of placement tasks across many aspects of physical implementation, such as mixed-size placement, timing-driven placement, power-aware placement and I/O-core co-placement, and is shown to be competitive in a wide variety of contexts [9, 10, 5].

4.2 Supply Voltage Degradation Aware Placement

We now propose smooth functions for average and worst-case supply voltage degradation evaluation and their integration in an analytical placement objective.

4.2.1 Average Supply Voltage Degradation

We rewrite Eqn. 3 to give supply voltage degradation at an observation P/G node g due to a supply current source v:

$$V_g = \sum_v I_v R_g(x_v, y_v) \quad (8)$$

where $R_g(x_v, y_v)$ is the effective resistance for a current source at the power node g to generate a voltage-drop at the node to which module v is currently connected. During global placement, with module v moving constantly, the effective resistance $R_g(x_v, y_v)$ becomes a function of the module's position.

Average voltage degradation over P/G network nodes is given as:

$$V_{avg} = \frac{1}{N}\sum_g \sum_v I_v R_g(x_v, y_v) \quad (9)$$

where N is the total number of observation nodes.

For efficiency improvement, we compute effective resistances $R_g(x_v, y_v)$ for a subset of P/G nodes (i.e., the observation nodes); and apply bi-linear interpolation to obtain

effective resistance at continuous positions.

$$\begin{aligned} R_g(x,y) &= \frac{x_2-x}{x_2-x_1}\cdot\frac{y_2-y}{y_2-y_1}\cdot R_g(x_1,y_1) \\ &+ \frac{x-x_1}{x_2-x_1}\cdot\frac{y_2-y}{y_2-y_1}\cdot R_g(x_2,y_1) \\ &+ \frac{x_2-x}{x_2-x_1}\cdot\frac{y-y_1}{y_2-y_1}\cdot R_g(x_1,y_2) \\ &+ \frac{x-x_1}{x_2-x_1}\cdot\frac{y-y_1}{y_2-y_1}\cdot R_g(x_2,y_2) \end{aligned} \quad (10)$$

The partial differentials of the effective resistance function at continuous positions are given as follows.

$$\begin{aligned} \frac{\partial R_g}{\partial x} &= \frac{1}{x_2-x_1}\cdot\frac{y_2-y}{y_2-y_1}\cdot(R_g(x_2,y_1)-R_g(x_1,y_1)) \\ &+ \frac{1}{x_2-x_1}\cdot\frac{y-y_1}{y_2-y_1}\cdot(R_g(x_2,y_2)-R_g(x_1,y_2)) \\ \frac{\partial R_g}{\partial y} &= \frac{x_2-x}{x_2-x_1}\cdot\frac{1}{y_2-y_1}\cdot(R_g(x_1,y_2)-R_g(x_1,y_1)) \\ &+ \frac{x-x_1}{x_2-x_1}\cdot\frac{1}{y_2-y_1}\cdot(R_g(x_2,y_2)-R_g(x_2,y_1)) \end{aligned} \quad (11)$$

4.2.2 Worst-Case Supply Voltage Degradation

Worst-case supply voltage degradation over all P/G network nodes is given as follows.

$$V_{worst} = \max_g\{V_g\} \quad (12)$$

However, the $\max$ function in Eqn. 12 can not be efficiently minimized using nonlinear optimization techniques, since it is not smooth or differentiable. We apply a **log-sum-exp** method to capture the worst-case voltage degradation while simultaneously obtaining the desirable characteristic of continuous differentiability.

$$V_{worst} = \alpha \cdot ln(\sum_g e^{V_g/\alpha}) \quad (13)$$

where α is a smoothing parameter: V_{worst} is strictly convex, continuously differentiable and converges to the worst-case voltage degradation as α converges to 0. The log-sum-exp formula picks the maximum voltage degradation among the voltage degradation of all the power nodes; it has been previously used in physical design applications such as transistor sizing and wirelength-driven placement [20, 11, 3].

Intuitively, the smoothing parameter α in Eqn. 13 can also be regarded as a "significance criterion" for choosing P/G network nodes with large voltage degradation to minimize. Only power nodes with a voltage degradation which has a small difference from the maximum voltage degradation relative to α will introduce significant differentials of modules' positions, as shown in the following equation.

$$\frac{\partial V_{worst}}{\partial V_g} = \frac{1}{\sum_t e^{(V_t-V_g)/\alpha}} \quad (14)$$

In the experiments, we set α to one-tenth of the maximum voltage degradation.

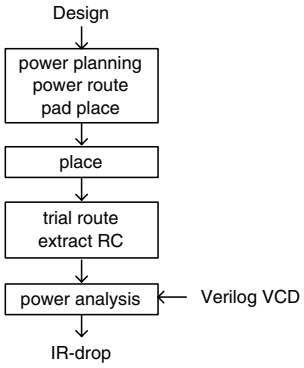

Figure 1. Flow for evaluating voltage-degradation-aware placement techniques.

4.2.3 Implementation

We combine supply voltage degradation with existing placement metrics, e.g., wirelength, congestion, and timing, in an analytical placer. For example, combining wirelength and supply voltage degradation extends Eqn. 6 as follows.

$$\begin{array}{lll} min & HPWL(\mathbf{x},\mathbf{y}) + & W_v \cdot V_{worst}(\mathbf{x},\mathbf{y}) \\ s.t. & D_g(\mathbf{x},\mathbf{y}) = D & \text{for each global cell } g \end{array} \quad (15)$$

where W_v is the weight of the voltage degradation objective. We compute the voltage degradation weight W_v according to the gradients derived from the wirelength and voltage degradation terms so that the scaled voltage degradation gradients are comparable to the wirelength gradients:

$$W_v = \beta \cdot \frac{\sum_{x_i,y_j}(|\frac{\partial WL}{\partial x_i}|+|\frac{\partial WL}{\partial y_j}|)}{\sum_{x_i,y_j}(|\frac{\partial V_{worst}}{\partial x_i}|+|\frac{\partial V_{worst}}{\partial y_j}|)} \quad (16)$$

where the voltage degradation ratio β decides the ratio of the voltage degradation gradients to the wirelength gradients, and provides a trade-off knob between voltage degradation and wirelength objectives for the placer.

5 Experiments

We apply our supply-voltage-degradation-aware placement on industry designs in a complete flow and compare with existing wirelength-driven analytical placement [9, 11].

Experimental Setup. The experimental flow is shown in Figure 1. Design inputs include synthesized netlists, technology libraries, timing constraints and floorplans. We run Cadence SoC Encounter to create power/ground rings/rails, conduct power routing, and specify power pad locations.

Placements with or without voltage-degradation-awareness are then generated using our placer or the

Table 1. Characteristics of test cases.

Design	# Cells	# Blocks	# Rows	Tech	Utilization
AES	13397	0	129	$90nm$	0.60
PCI	7128	5	251	$180nm$	0.43

Table 2. Results of worst-case voltage-degradation aware placements with a variety of voltage degradation ratios (β's).

Design	Placer	Vdrop Ratio β	Vdrop Analysis				Place		
			Avg Vdrop		Max Vdrop		HPWL		CPU
			(V)	(%)	(V)	(%)	(e8)	(%)	(s)
AES	APlace	0.00	0.233	0.00	0.406	0.00	9.48	0.00	224
	Ours	0.05	0.217	6.61	0.354	12.74	9.58	-1.10	287
		0.10	0.219	6.02	0.356	12.41	9.57	-0.94	266
		0.15	0.214	8.07	0.331	18.49	9.67	-1.95	240
		0.20	0.208	10.67	0.318	21.59	9.68	-2.09	227
		0.25	0.209	10.22	0.314	22.65	9.78	-3.17	218
PCI	APlace	0.00	0.026	0.00	0.051	0.00	19.95	0.00	121
	Ours	0.05	0.025	3.18	0.048	5.54	20.14	-0.93	172
		0.10	0.025	5.84	0.046	9.75	20.25	-1.50	166
		0.15	0.024	9.27	0.044	13.67	20.53	-2.92	156
		0.20	0.023	11.52	0.042	16.65	20.72	-3.87	145
		0.25	0.023	13.08	0.041	19.02	21.01	-5.33	146

existing wirelength-driven APlace. After placement, we perform fast global and detail routing by Cadence TrialRoute, extract RC and analyze steady-state voltage-drops by Cadence VoltageStorm.

Our voltage-degradation-aware placer takes as input (1) the LEF/DEF files exported by SoC Encounter which include P/G network geometries, (2) the equivalent resistance between each pair of observation nodes computed by random walk as is described in Section 3.3, and (3) the average current drain of each module generated by VoltageStorm.

We conduct our experiments on two industry designs, which characteristics are shown in Table 1. Both designs have six metal layers, a power/ground ring at the top two layers and four power pads located near the center of the four boundary lines. The AES test case has five power stripes at METAL2. The PCI test case has four power stripes at METAL6 and five large fixed macros in the layout.

Experimental Results. Tables 2 and 3 summarize the worst-case and average voltage-degradation aware placement results, respectively, after completing the experimental flow for the two industrial test cases. We compare our voltage-degradation-aware placer with wirelength-driven APlace. For each design, we perform the voltage-degradation-aware placement with five different voltage degradation ratios ranging from 0.05 to 0.25.

The fourth and sixth columns of Table 2 and Table 3 show the average and maximum voltage degradation of each placement. We also show the improvements in percentage in the fifth and seventh columns. In both tables, the average and maximum voltage degradation results of our placer decreases with the increasing voltage degradation ratio. Either voltage degradation placement objective benefits both metrics at the same time, but with different emphases.

Table 3. Results of average voltage-degradation aware placements with a variety of voltage degradation ratios (β's).

Design	Placer	Vdrop Ratio β	Vdrop Analysis				Place		
			Avg Vdrop		Max Vdrop		HPWL		CPU
			(V)	(%)	(V)	(%)	(e8)	(%)	(s)
AES	APlace	0.00	0.233	0.00	0.406	0.00	9.48	0.00	224
	Ours	0.05	0.219	6.13	0.361	11.12	9.50	-0.23	284
		0.10	0.210	9.79	0.343	15.48	10.04	-5.88	273
		0.15	0.209	10.19	0.341	16.07	10.12	-6.76	319
		0.20	0.201	13.68	0.320	21.24	10.28	-8.46	312
		0.25	0.192	17.64	0.302	25.70	10.40	-9.74	286
PCI	APlace	0.00	0.026	0.00	0.051	0.00	19.95	0.00	121
	Ours	0.05	0.025	4.94	0.047	6.75	20.22	-1.35	160
		0.10	0.024	9.14	0.044	13.06	21.04	-5.44	175
		0.15	0.019	26.03	0.035	29.80	22.83	-14.45	206
		0.20	0.018	31.02	0.033	35.14	23.18	-16.18	234
		0.25	0.016	39.54	0.028	43.99	25.16	-26.10	285

The impact of voltage-degradation-aware placement in terms of HPWL and runtime of the placer are shown in the eighth to tenth columns of Table 2 and Table 3. Voltage-degradation-aware placement usually has a negative impact on these metrics. Placed HPWL increases with the increasing voltage degradation ratio.

We observe that the worst-case voltage degradation objective leads to better voltage degradation improvements than the average voltage degradation objective, with roughly the same wirelength increase. For example, for the AES test case, the worst-case voltage-degradation aware placement obtains a 10.2% improvement on the average voltage degradation with 3.2% wirelength increase, but the average voltage-degradation aware placement achieves roughly the same average voltage degradation improvement (10.2%) with larger wirelength increase (6.8%). The same phenomenon happens for the PCI test case. The reason is that during worst-case voltage-degradation aware placement, a power node with a larger voltage degradation leads to a larger weight for the gradients of modules' coordinates, as discussed in Section 4.2.2. I.e., large voltage degradations are among the first to be reduced, which benefits the average voltage degradation more than trying to reduce all the voltage degradations with the same efforts.

The voltage degradation ratio (β) can be used as a knob to trade-off voltage degradation and wirelength. As shown in Tables 2 and 3, the voltage degradations generally decrease with the voltage degradation ratio increasing; wirelength generally increases with the voltage degradation ratio. A proper value can be chosen according to the practical requirement.

In summary, compared to the reference run using wirelength-driven APlace, our voltage-degradation-aware placer improves the worst-case voltage degradation by 22.7% (19.0%) and the average voltage degradation by 10.2% (13.1%), with only 3.2% (5.3%) increase of HPWL for the AES (PCI) test case. Such supply voltage degradation reductions lead to more significant performance improvements due to the superlinear relationship between performance and supply voltage.

6 Conclusion

We have proposed placement for supply voltage degradation reduction, e.g., by relocating supply current sources for maximum supply voltage degradation reduction. We characterize the contribution of each supply current source to the voltage degradation at a P/G node by an effective impedance, which is reduced to an effective resistance in DC analysis, and propose random walk, contraction and interpolation techniques to efficiently find an effective resistance between two nodes. We also integrate supply voltage degradation into an analytical placement objective in a smooth function. Our experimental results show in average 20.9% improvement of worst-case voltage degradation and 11.7% improvement of average voltage degradation with only 4.3% wirelength increase, and imply further performance improvements.

Our ongoing research efforts address, among other goals, transient supply voltage degradation optimization via decoupling capacitor insertion techniques.

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