Enhanced Resist and Etch CD Control by Design Perturbation

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ABSTRACT

Etch dummy features are used in the mask data preparation flow to reduce critical dimension (CD) skew between resist and etch processes and improve the printability of layouts. However, etch dummy rules conflict with SRAF (Sub-Resolution Assist Feature) insertion because each of the two techniques requires specific spacings of poly-to-assist, assist-to-assist, active-to-etch dummy and dummy-to-dummy. In this work, we first present a novel SRAF-aware etch dummy insertion method (*SAEDM*) which optimizes etch dummy insertion to make the layout more conducive to assist-feature insertion after etch dummy features have been inserted. However, placed standard-cell layouts may not have the ideal whitespace distribution to allow for optimal etch dummy and assist-feature insertions. Since placement of cells can create forbidden pitch violations, the placer must generate assist-correct and etch dummy-correct placements. This can be achieved by intelligent whitespace management in the placer. We describe a novel dynamic programming-based technique for etch-dummy correctness (*EtchCorr*) which can be combine with the SAEDM in detailed placement of standard-cell designs. Our algorithm is validated on industrial testcases with respect to wafer printability, database complexity and device performance.

1. INTRODUCTION

Across-chip line-width variation (ACLV) induced by photo-lithography and etch processes has been a major barrier in ultra-deep submicron manufacturing. In dry etch processes such as plasma, ion and reactive ion etch (RIE), different doses of etchants with different pitches cause different critical dimension (CD) behaviors between photo and etch processes. This etch micro-loading effect (referred to as etch proximity in this paper) increases the skew between resist and etch CDs. Etch dummy features have been introduced into the layout to reduce the CD distortion induced by the etch proximity. The etch dummies are placed at the outside of active layers so that leftmost and rightmost gates on active-layer regions are protected from ion scattering during the etch process. However, etch dummy rules conflict with SRAF insertion because each of the two techniques requires specific spaces from poly. In such a regime, the assist-feature correction (*AFCorr*) placement methodology devised by [Gupta et al.[6]] is no longer applicable. We present a novel SRAF-aware etch dummy insertion method (SAEDM) which applies flexible etch dummy rules according to the distance from active edge to leftmost (or rightmost) poly. As a result, the layout will be more conducive to assist-feature insertion after etch dummy features have been inserted. In addition, we introduce a dynamic programming-based technique, EtchCorr, to achieve etch dummy correctness in the detailed placement of standard-cell designs. For benchmark industrial designs, forbidden pitch count between polysilicon shapes of neighboring cells after the SAEDM is reduced by 57%-97% with across a range of utilizations. After EtchCorr, the forbidden pitch count of resist CD is reduced by 90% - 100%, and etch skew is reduced by 73%-97%. Edge placement error (EPE) count is also reduced by 91%-100% in resist CD and 72%-98% in etch CD. EtchCorr facilitates additional SRAF and etch dummy insertions by up to 10.8% and 18.6%, respectively.

1.1. Contributions of This Work

This paper first presents various analyses of photo and etch process printability within the context of the standard-cell design methodology. Our goal is to minimize CD variation error, minimize skew between resist and etch CDs, and enhance feature printability and reliability. Our main contributions are as follows.

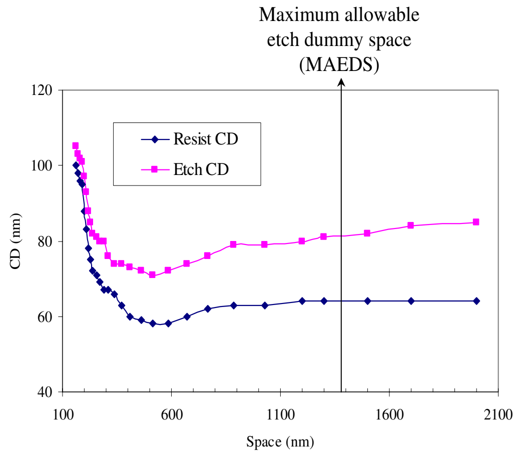

Figure 1: Different proximity behaviors between photo and etching processes with pitch.

- We first present an SRAF-aware etch dummy insertion method (*SAEDM*) which optimizes etch dummy insertion to make the layout more conducive to assist-feature insertion after etch dummy features have been inserted.
- We propose a novel post-detailed placement perturbation algorithm for *Etch-Dummy Correctness (Etch-Corr)*, which uses efficient dynamic programming method to remove forbidden pitches of resist CD and to reduce the skew between resist and etch CDs. In conjunction with intelligent process-aware library layout, this technique can achieve improvements in depth of focus (DOF) margin and CD control.

1.2. Organization of The Paper

The remainder of this paper is organized as follows. In Section 2, we review SRAF and etch dummy techniques, and describe the etch dummy correction problem. Section 3 introduces our SRAF-aware etch dummy insertion method and post-placement perturbation technique. Evaluation flows to validate the impact of our proposed methods on photo and etch process manufacturability, along with experimental results, are described in Section 4. We conclude in Section 5 with directions for ongoing research.

2. SUB-RESOLUTION ASSIST FEATURES AND ETCH DUMMIES

Sub-resolution assist features (SRAFs) provide an absolutely essential technique for CD control and process window enhancement in subwavelength lithography. SRAFs are extremely narrow lines that do not actually print on the wafer. The maximum SRAF width is typically two times thinner than the to-be-printed primary pattern*. Therefore, certain minimum assist-to-poly and assist-to-assist spacings are required to prevent SRAFs from printing in the maximum allowable defocus for manufacturing.

Insertion of etch dummy features has been introduced to reduce the CD difference between resist and etch processes for 90nm and below technology nodes. In dry etch processes such as plasma, ion, and reactive ion etch (RIE), different consumptions of etchants with different pattern density lead to etch skew between dense and isolated patterns. For example, all available etchants in areas with low density are consumed rapidly, and thus the etch rate then drops off significantly. In areas with high density of patterns, the etchants are not consumed as quickly. As a result, the proximity behavior of photo process differs from etch process as shown in Figure 1. In general, the etch skew of two processes increases as pitch increases. When etch dummies are placed adjacent to primary patterns, a relatively isolated primary line will behave more like a dense line, and thus the etch dummies can reduce the etch skew. Moreover, the maximum relevant pitch is reduced through

*SRAF width is given as 60nm and 40nm for the 130nm and 90nm technology nodes, respectively.

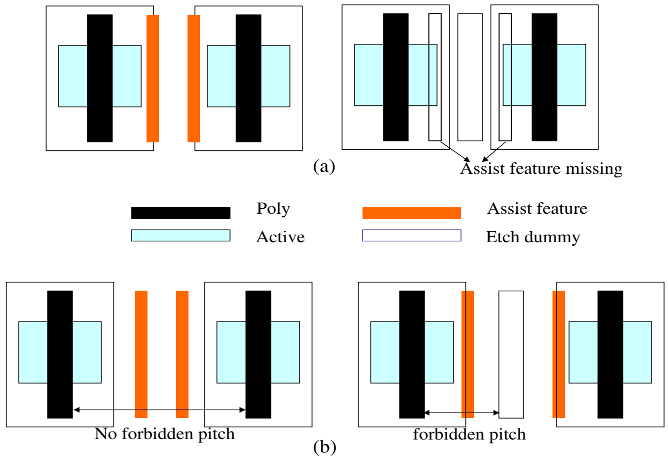

Figure 2. Conflict between SRAF and etch dummy rules: (a) assist feature missing and (b) forbidden pitch occurrence.

etch dummy insertion. This is an important consideration with respect to model-based OPC, which calculates the proximity effect of all patterns within a given proximity range, such that larger proximity range increases OPC runtime. Granik[5] observes that the proximity range of the etch process is around 3μm, which prevents conventional model-based OPC from delivering a good OPC mask within feasible turnaround time.

Etch Dummy Insertion Problem. Given a layout, find an etch dummy placement such that the following conditions are satisfied:

- Condition (1): Etch dummies are inserted between primary patterns with certain spacing to reduce etch skew between resist and etch processes, and proximity range.
- Condition (2): Etch dummies are placed outside of active-layer regions.

The maximum allowable etch dummy space (MAEDS) in Condition (1) is determined by the allowable CD skew of resist and etch processes. However, forbidden pitch correction in the resist process is still required after inserting etch dummy because the etch dummy cannot be placed too close to primary patterns due to Condition (2). The fact of etch dummy insertion can make printability of resist process worse in particular pattern configurations. Figure 2 shows examples such as (a) assist features missing and (b) forbidden pitch occurrence. Assist features can be missed due to lack of space between primary pattern and etch dummy, even when there is enough space to insert multiple SRAFs before etch dummy insertion. New forbidden pitches for assist feature can occur in the spacing between poly and etch dummy due to mismatch between rules for assist feature and etch dummy corrections. Therefore, the EtchCorr problem is as follows.

Etch Dummy Correction Problem. Given a standard-cell layout, determine perturbations to inter-cell spacings so as to simultaneously insert SRAFs in forbidden pitches and insert etch dummies within MAEDS.

3. ETCH DUMMY CORRECTION METHODOLOGY

3.1. SRAF-Aware Etch Dummy Generation

To reduce etch proximity, at most one etch dummy for each active geometry is needed since the etch skew depends on pattern-to-pattern spacing regardless of local pattern density,[10] i.e., etch skew decreases as the spacing is reduced. SRAFs and etch dummies have been generated by rule-based methods with look-up tables (LUTs) since simulation tools are much slower than rule-based tools. Typically, etch dummy rules consist of etch dummy-to-active space (DAS), etch dummy width (EW) and etch dummy-to-dummy space (DDS) with respective values of 120nm, 100nm and 200nm being typical for 90nm technology. Let ES denote the space between active geometry in the left and right cells as shown in Figure 3. Let ED_1 and ED_2 denote

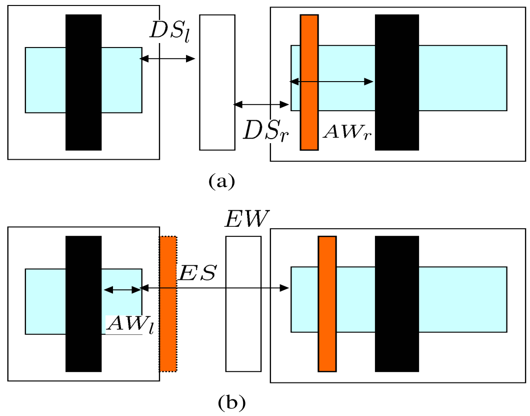

Figure 3: (a) Typical etch dummy generation. (b) SRAF-aware etch dummy generation.

Etch dummy rules		Typical method		SAEDM	
	ES (X)	DS_l	DS_r	DS_l	DS_r
#ED = 0	$0 \leq X < ED_1$				
#ED = 1	$ED_1 \leq X < ED_2$	$(ES$ -$EW)/2$	$(ES$ - $EW)/2$	$AS_l + DAS$	$AS_r + DAS$
#ED = 2	$X \leq ED_2$	DAS	DAS	$AS_l + DAS$	$AS_r + DAS$

Table 1. Comparison of etch dummy rules with typical etch dummy method and SAEDM. Note that AS_l + AS_r = ES - ED_l

the required spaces to insert one and two etch dummies in ES, respectively. For typical methods of etch dummy insertion, minimum space rules for one and two etch dummies are ED_1 =$2 * DAS$+EW and ED_2 = $2 * DAS$+$2 * EW$+DDS, respectively. The first etch dummy in the typical etch dummy rule is always placed at the center of the space between two active geometries, while the active-to-etch dummy space for the second etch dummy is always according to the space rule, DAS.

Once etch dummies have been inserted for only etch proximity control, the spacing between poly and etch dummy may not be appropriate for SRAF insertion. Figure 3(a) shows an example where the left-hand side SRAF cannot be inserted due to lack of poly-to-etch dummy spacing. Let AW_l and AW_r denote the widths of active geometries located at left- and right-cells, respectively. Let $AF = AF_1, \ldots, AF_m$ denote a set of "assist-correct" spacings, i.e., if the spacing between two gate poly shapes belongs to the set AF, then the required number of assist features can be inserted between the two poly geometries. AF_j denotes the j^{th} member of the set of assist-feature correct spacings AF. Let AS_l and AS_r denote additional spacings needed for assist-correctness in the left- and right-cells, respectively. To avoid missing SRAFs and occurrence of forbidden pitches, we propose a new *SRAF-Aware Etch Dummy Method* (SAEDM) considering active width (AW) during insertion of etch dummy, as follows:

$$\begin{array}{ll} Minimize & \text{index values of } j \text{ and } k \text{ in a set } AF \\ s.t. & AS_l = AF_j - (AW_l + DAS) \text{ and } AS_r = AF_k - (AW_r + DAS), \\ & \text{and } (AS_l + AS_r) \leq (ES - ED_1) \end{array} \quad (1)$$

SAEDM searches assist-correct spacing with minimum index values in a set AF, so that the sum of the additional spacings AS_l and AS_r corresponding to assist-correct spacings is less than $(ES - ED_1)$. Let DS_l and DS_r denote the left- and right-spaces from etch dummy to border active geometries in left- and right-cells, respectively. Thus, new etch dummy spaces of $DS_l = AS_l + DAS$ and $DS_r = AS_r + DAS$ are both assist-correct and etch dummy-correct. Note that the etch dummy after SAEDM is no longer located at the center of an active-to-active space since DS_l differs from DS_r, as shown in Figure 3(b). Table 1 compares DS_l and DS_r values returned by the typical etch dummy method and by SAEDM.

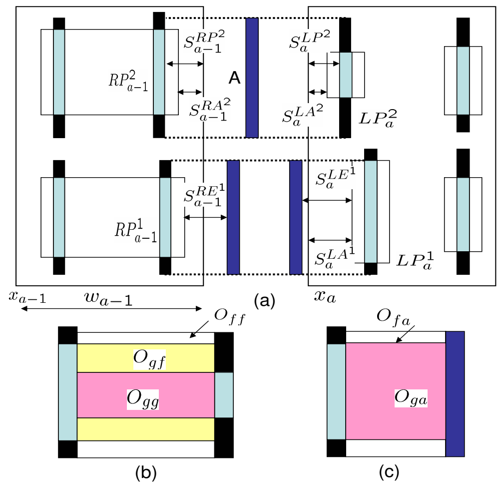

Figure 4. The placement perturbation problem of assist and etch dummy. (a) Multiple interactions of gate-to-dummy and field-to-dummy. (b) Overlapped area in the region A of (a) as there is no etch dummy. (c) Overlapped area in the region A of (a) as there is etch dummy.

3.2. Etch Dummy Correctness

Assist-correct pitch rules are violated if there is not enough space to insert AS_l and AS_r. We now describe a novel *EtchCorr* placement perturbation algorithm which achieves intelligent whitespace management for both assist-correct and etch-correct placements. Our EtchCorr formulation is similar to the previous AFCorr method that corrects forbidden pitches in the photo process.[6, 8] However, EtchCorr differs from AFCorr as follows: (1) EtchCorr is based on the active-to-cell outline spacing while AFCorr is poly-to-cell outline spacing. (2) EtchCorr calculates the virtual positions of etch dummy in order to both insert SRAF in assist-correct spacing and etch dummy in etch dummy-correct spacing.

In the following, we describe the single-row EtchCorr perturbation algorithm, using a 2D EtchCorr problem which is solved one cell row at a time. Let w_a denote the width of cell C_a and let x_a denote its placement coordinate (leftmost point) in the given standard cell row, indexed from left to right. Let $s_a^{RP_i}$ and $s_a^{RA_j}$ respectively denote the spacing between the right outline of the cell and the i^{th} right border poly, and the spacing between the right outline of the cell and j^{th} active geometry. $s_a^{RE_i}$ is the spacing from right border poly to etch dummy as shown in Figure 4. Let δ denote a cell placement perturbation to adjust the spacing between cells. ES, the space between border actives, is $x_a - x_{a-1} - w_{a-1} + s_{a-1}^{RA_i} + s_a^{LA_i}$. We restrict the perturbation of any cell to $SRCH$ placement sites from its initial location. Then the etch dummy-correct placement perturbation problem is:

$$\text{Minimize } \sum \mid \delta_i \mid \text{ such that}$$

$$\begin{cases} \text{If } (ES < ED_1) \\ \delta_a + x_a - x_{a-1} - \delta_{a-1} - w_{a-1} + s_{a-1}^{RP^i} + s_a^{LP^i} \in AF \\ \delta_a + x_a - x_{a-1} - \delta_{a-1} - w_{a-1} + s_{a-1}^{RA^i} + s_a^{LA^i} \in EDS \\ \text{s.t. } -SRCH \leq \delta_{a-1} \text{ and } \delta_a \leq SRCH \\ \\ \text{otherwise} \\ S_{a-1}^{RP^i} - S_{a-1}^{RA^i} + S_{a-1}^{RE^i} + \delta_{a-1} \text{ and } S_a^{LP^i} - S_a^{LA^i} + S_a^{LE^i} + \delta_a \in AF \\ S_{a-1}^{RE^i} + \delta_{a-1} \text{ and } S_a^{LE^i} + \delta_a \in EDS \\ S_{a-1}^{RE^i} + \delta_{a-1} \text{ and } S_a^{LE^i} + \delta_a < \text{MAEDS} \\ \text{s.t. } -SRCH \leq \delta_{a-1} \text{ and } \delta_a \leq SRCH \end{cases} \qquad (2)$$

Etch dummy-correct spacing (EDS) is defined as inter-device spacing with etch skew having less than 10% of minimum line width. Our goal is for the inter-device spacing to become both assist-correct and etch dummy-correct. The objective can be made aware of cells in timing-critical paths by a weighting function. Since the available number of allowable spacings for assist and etch dummy insertions is very small, obtaining a completely correct solution is usually not possible in a fixed cell row width context. Therefore, a more tractable objective is to minimize the expected CD error at a predetermined defocus level. We solve this "continuous" version of the above problem by a dynamic programming approach.

$Cost(a, b)$ is the cost of placing cell a at placement site b. λ is a factor which specifies the relative importance of preserving the initial placement and the final AFCorr benefit achieved.[6] The terms $AFCost$ and $EDCost$ denote assist feature and etch dummy costs, respectively. $AFCost$ depends on the difference between the current nearest-neighbor spacing of the polys and the closest assist-correct spacing. The methods of computing $AFCost$ and $EDCost$ are shown in Figure 5. O_{gg}, O_{ff} and O_{gf} correspond to the length of overlapped area in the cases of gate-to-gate, field-to-field and gate-to-field poly as shown in Figure 4. O_{ge} and O_{fe} correspond to the overlapped length of gate-to-dummy and field-to-dummy. In addition, c_{gg}, c_{ff}, and c_{gf} are proportionality factors which specify the relative importance of printability for gate and field poly. W_1 and W_2 are user-defined weights for $AFCost$ and $EDCost$, respectively.

$$\begin{aligned} Cost(1, b) = \;& \mid x_1 - b \mid \\ Cost(a, b) = \;& \lambda(a) \mid (x_a - b) \mid + \\ & Min_{i=x_{a-1}-SRCH}^{x_{a-1}+SRCH}\{Cost(a-1, i) + W_1 AFCost(a, b, a-1, i) + W_2 EDCost(a, b, a-1, i)\} \end{aligned} \tag{3}$$

4. EXPERIMENTS AND DISCUSSION

4.1. Experimental Setup

We synthesize the $alu128$ benchmark design from *Opencores* in *Artisan TSMC 0.09μm* libraries using *Synopsys Design Compiler v2003.06-SP1.* $alu128$ synthesizes to 11.1K cells in 90nm technology. The synthesized netlists are placed with row utilization ranging from 50% to 90% using *Cadence First Encounter v3.3.* All designs are trial routed before running timing analysis. On the lithography side, we use *KLA-Tencor Prolith* to generate resist and etch models for OPC. *Mentor Graphics Calibre* is used for model-based OPC, SRAF OPC and optical rule checking (ORC). Resist simulation is performed with wavelength λ = 193nm and NA = 0.75 for 90nm. An annular aperture with σ = 0.85/0.65 is used. The target etch process consists of three etch steps: 10 second breakthrough etch step to get through the BARC, 60 second main etch step, and 36 second overetch step. The breakthrough and main etch steps in the model produce a fair amount of deposition, taking the resist profiles of 100nm. The overetch step trims this back to the 90nm range. Deposition is treated in the model as a negative horizontal etch rate. A set of etch parameters is shown in the Table 2. We only consider the first etch step to remove Si Nitride because second etch, step to etch gate poly, does not impact CD variation with pitch. Figure 7 shows the calibrated vertical profile of dense patterns after resist and etch processes. To account for new geometric constraints that arise due to SRAF and etch dummy in physical design, we add forbidden pitch extraction, CD slopes of resist and etch process with pitch, and CD skew induced by etch process. In addition, post-placement optimization is added into the current ASIC design methodology. Figure 8 shows the modified design flows in the regime of forbidden pitch extraction and etch dummy insertion.

4.2. Experimental Results

Proximity plots with SRAF OPC and Etch OPC for 90nm technology are illustrated in Figure 6. Exposure dose focuses on the pattern in the minimum pitch of 160nm. CD degradation increases in through-pitch as the defocus level increases. Resist CDs after SRAF OPC are evaluated with the worst case defocus model of 0.3μm. Resist and etch CDs vary with location of the SRAF insertion, and resist CDs violate the allowable CD tolerance[†] as distance between SRAF and poly increases. The trend of etch CD follows the variation of

[†]Allowable CD tolerance is assumed to be 10% of minimum line width as the worst defocus level is assumed to be 0.3μm.

Cost(a,b,a-1,i) of Cell C_a

Input:

User-defined weights for poly-to-poly: c_{gg}, c_{ff}, c_{gf}
User-defined weights for poly-to-dummy: c_{ge}, c_{fe}
Origin (left) x coordinate and length of cell C_a = b
Origin (left) x coordinate and length of cell C_{a-1} = i
Width of cell $C_a = w_a$
Width of cell $C_{a-1} = w_{a-1}$

Output:

Value of $AFCost$ and $EDCost$

Algorithm:

Let $AFspace(h,k)$ denote the horizontal spacing between RP_{a-1}^h and LP_a^k.
Let $ES(h,k)$ denote the horizontal spacing between RA_{a-1}^f and LA_a^g.
Let $AFslope(j)$ be defined as delta resist CD difference over delta pitch between AF_j and AF_{j+1}.
Let $EDslope(j)$ be defined as delta etch CD difference over poly-to-dummy space.

Case $a = 1$: $AFCost(1,b) = EDCost(1,b) = 0$
Case $a > 1$ **Do**
J:= cardinality of set RP_{a-1}
L:= cardinality of set LP_a
/* Calculate overlap weight between RP_h^{a-1} and LP_k^a */
For $(h = 1 ; h = J ; h = h + 1)${
  For $(k = 1 ; k = L ; k = k + 1)$ {
    If $(AFspace(h,k) < ED_1)$ {
      $AFweight(h,k) = AFslope(j) \times (AFspace(h,k) - AF_j)$
        $\times (c_{ff}O_{ff}(h,k) + c_{gf}O_{gf}(h,k) + c_{gg}O_{gg}(h,k))$
        s.t. $AF_{j+1} > AFspace(h,k) \geq AF_j$
      $EDweight(h,k) = EDslope(AFspace(h,k))$
        $\times (c_{ge}O_{ge}(h,k) + c_{fe}O_{fe}(h,k))$
    }
    Else {
      $AFweight(h,k) = AFslope(j) \times (AW_l(h,k) + DS_l(h,k) - AF_j)$
        $\times (c_{ge}O_{ge}(h,k) + c_{fe}O_{fe}(h,k))$
      $AFweight(h,k) += AFslope(l) \times (AW_r(h,k) + DS_r(h,k) - AF_l)$
        $\times (c_{ge}O_{ge}(h,k) + c_{fe}O_{fe}(h,k))$
      $EDweight(h,k) = (EDslope(AW_1(h,k) + DS_l(h,k)) + EDslope(AW_r(h,k) + DS_r(h,k))$
        $\times (c_{ge}O_{ge}(h,k) + c_{fe}O_{fe}(h,k))$
    }
    $AFCost(a,b,a-1,i)$ += $AFweight(h,k)$
    $EDCost(a,b,a-1,i)$ += $EDweight(h,k)$
  }
}

Figure 5: The algorithm for $AFCost$ and $EDCost$ calculations.

Stage	Etch time (sec)	Material	Vertical etch rate (sec)	Horizontal etch rate (sec)	Faceting Parameter Parameter
1	10	ArF Sumitomo	10.66	-0.6	0.5
		AZ BarLi-2	10.52	-0.7	0.0
		Si Nitride	10.28	-0.7	0.0
2	60	ArF Sumitomo	0.3	-0.12	0.5
		AZ BarLi-2	3.4	-0.2	0.0
		Si Nitride	30.4	-0.3	0.0
3	36	ArF Sumitomo	10.65	0.9	0.5
		AZ BarLi-2	0.25	1.0	0.0
		Si Nitride	0.0	1.5	0.0

Table 2: Process conditions for etch simulator in 90nm technology.

resist CD. A set of forbidden pitches in resist process is obtained as follows: [0.3, 0.41), [0.45, 0.57), [0.64, 0.73), and [0.78, 0.89) (microns). The skews of resist and etch CDs continuously increase with pitch and are not saturated by 1.1μm as shown in Figure 6. All etch dummy should be placed within MAEDS (900nm) to control etch skew within 9nm, 10% of minimum line width. We generated SRAF rules with results in Table 3. SRAF width and SRAF-to-pattern space are 40nm and 120nm, respectively. In addition, dummy-to-active space, etch dummy width, and etch dummy-to-dummy space correspond to 120nm, 100nm and 200nm respectively. However, the spacing between active and etch dummy is varying because SAEDM changes the space with the active width. The EtchCorr placement optimization with the SAEDM is performed with forbidden pitch rules and CD slopes of resist and etch processes. After EtchCorr placement perturbation, we obtain a new placement wherein the coordinates of cells minimize the occurrence of forbidden pitches of resist and etch processes. Total

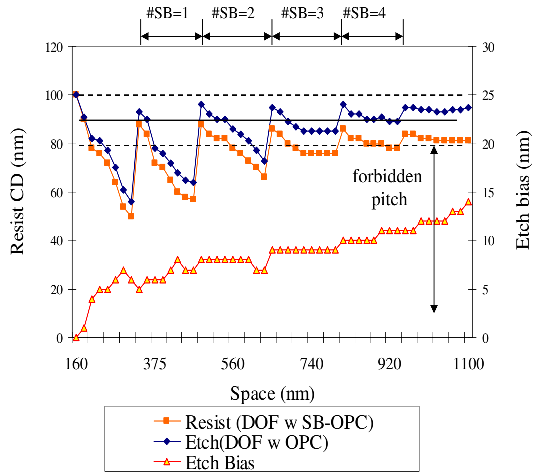

Figure 6. Evaluations of proximity plots and etch skew in through-pitch: worst defocus with SRAF OPC and worst defocus with etch OPC (left Y-axis), and etch skew (right Y-axis).

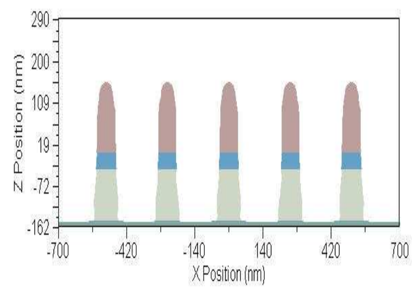

Figure 7: Calibrated vertical profile after photo and etch processes.

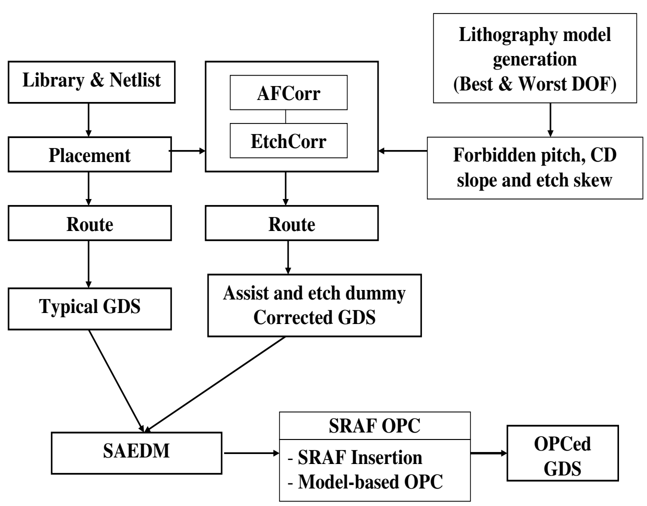

Figure 8. The modified design flows. Note the added steps of (1) obtaining forbidden pitch, CD slopes of resist and etch, and skew between resist and etch CDs, and (2) post-placement optimization, into the traditional ASIC implementation flow.

	AF Pitch($X : \mu m$)	Slope	Forbidden Pitch($X : \mu m$)
#SRAF = 0	$0 \le X < 0.41$	0.284	$0.3 \le X < 0.41$
#SRAF = 1	$0.41 \le X < 0.57$	0.22	$0.45 \le X < 0.57$
#SRAF = 2	$0.57 \le X < 0.73$	0.105	$0.64 \le X < 0.73$
#SRAF = 3	$0.73 \le X < 0.89$	0.07	$0.78 \le X < 0.89$

Table 3: SRAF rules and forbidden pitches in 90nm lithography.

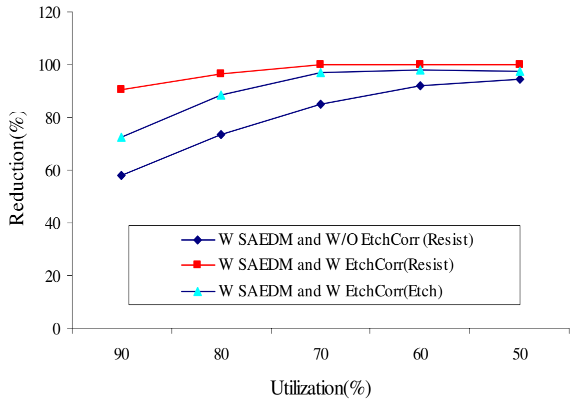

Figure 9. Reductions of forbidden pitches with various etch dummy insertion methods for each of five different utilizations.

cost of EtchCorr is calculated using specific weights of resist and etch costs (in the results reported, we use respective weights $W_1 = 0.9$ and $W_2 = 0.1$). Note that our post-placement perturbation problem reduces to the previously-studied AFCorr problem if $W_2 = 0$.

To validate on industrial testcases, we use three printability quality metrics. *Forbidden Pitch Count* of photo process is the number of border poly geometries estimated as having greater than 10% CD error through-focus. Forbidden pitch violation of etch process represents 10% etch skew error between photo and etch processes. $EPECount$ of photo and etch processes is the number of edge fragments on border poly geometries having greater than 10% edge placement error at the worst defocus level. This is estimated by ORC. *SB Count* and *Dummy Count* are the total number of scattering bars and etch dummies, respectively. We evaluate the reduction of Forbidden Pitch Count in resist and etch processes as shown in Table 4. Forbidden Pitch Count of photo process after SAEDM can be reduced by 57% - 94% with various utilizations because the etch dummy-to-poly spacings become assist-correct. However, Forbidden Pitch Count of the etch process may increase in certain layout configurations (up to between 4% - 6%) because the SAEDM increases the poly-to-etch dummy spacing.

EtchCorr technique in conjunction with SAEDM presents additional reduction of forbidden pitches. EtchCorr can reduce the Forbidden Pitch Count of resist by up to 100% at 50% utilization. Forbidden Pitch Count of etch process is considerably reduced by 73% - 97% as shown in Figure 9. 92 pitches cannot be reduced at 50% and 60% utilization due to poly-to-etch dummy spacings increased by the SAEDM. In other words, the active width is too large to reduce poly-to-etch dummy spacing. Figure 10 shows that - as one would expect - the total number of inserted SRAFs and etch dummies increases as the utilization decreases. The benefit of EtchCorr decreases with lower utilization since the design already has enough whitespace for SRAF and etch dummy insertions. We also see that the EPE Count metric is reduced by 91%-100% in resist process and 72%-98%

	Utilization (%):	90	80	70	60	50
Photo	W/O SAEDM and W/O EtchCorr	37433	31314	29216	26765	21282
	W SAEDM and W/O EtchCorr	15743	8330	4423	2075	1198
	W SAEDM and W EtchCorr	3566	1116	51	0	0
Etch	W/O SAEDM and W/O EtchCorr	15816	8812	4656	4345	3530
	W SAEDM and W/O EtchCorr	16418	9729	5282	5002	4209
	W SAEDM and W EtchCorr	4321	1032	143	92	92

Table 4: Forbidden pitch results with various etch dummy insertion methods in resist and etch processes.

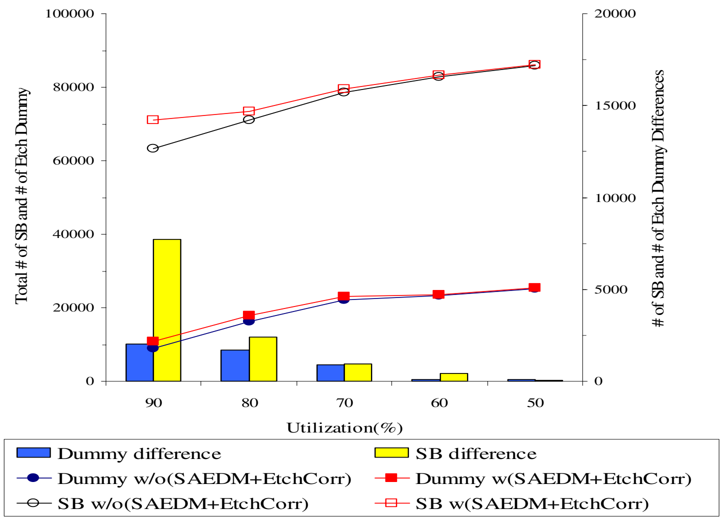

Figure 10. Number of inserted SRAF and etch dummy features with various etch dummy insertion methods for each of five different utilizations.

	Util.(%):	90		80		70		60		50	
	Flow:	Typical	EtchCorr	Typical	EtchCorr	Typical	EtchCorr	Typical	EtchCorr	Typical	EtchCorr
Photo	# EPE	42102	3723	32434	1243	29349	98	28721	13	23134	2
	#Forbidden	37433	3566	31314	1116	29216	51	26765	0	21282	0
	# SB	63349	71051	71101	73501	78513	79432	82820	83230	85991	86026
Etch	# EPE	17209	4812	9213	1200	4820	182	4821	109	3890	109
	#Forbidden	15816	4321	8812	1032	4656	143	4345	92	3530	92
	# Dummy	8876	10911	16240	17920	22088	23001	23390	23499	25237	25309
Other	Runtime (s)	6835	7011	7451	7535	7529	7632	7685	7698	7943	7944
	GDS (MB)	41.1	42.3	41.2	43.2	42.2	42.3	42.9	42.8	43.6	43.6
	Delay (ns)	2.478	2.305	2.458	2.602	2.522	2.47	2.867	3.176	3.113	3.046

Table 5. Summary of EtchCorr results. Runtime denotes the runtime of SRAF and etch dummy insertion, as well as model-based OPC. The EtchCorr perturbation runtime ranges from 10 to 11 minutes for all testcases. GDS size is the post-OPC data volume.

in etch process. In addition, SB Count improves by 0%-10.8% for resist process. Dummy Count increases by 0%-18.6% for etch process. Note that these numbers are small as they correspond to the entire layout rather than just the border poly geometries. The change in estimated post-trial route circuit delay ranges from 3.9% to 4.2%. The increases of data size and OPC running time overheads of EtchCorr are within 3% and 4%, respectively. Finally, the runtime of EtchCorr placement perturbation is negligible ($\sim$ 5 minutes) compared to the running time of OPC ($\sim$ 2.5 hours). All of these results are summarized in Table 5.

5. CONCLUSIONS AND ONGOING WORK

In this work, we have presented novel methods to optimize etch dummy insertion rules and detailed standard-cell placements for improved etch dummy and assist-feature insertion. The *SAEDM* method optimizes etch dummy insertion to make the layout more conducive to assist-feature insertion after etch dummy features have been inserted. We also introduce a dynamic programming-based technique, *EtchCorr*, to achieve etch dummy insertion correctness in the detailed placement step of standard-cell based chip implementation. EtchCorr with SAEDM leads to reduced CD variation and increased insertion of assist features and etch dummies. Forbidden pitch count after SAEDM is reduced by 57%-94% across various utilizations. After EtchCorr with SAEDM, Forbidden Pitch Count of the photo process is reduced by 90% - 100% while Forbidden Pitch Count of the etch process is reduced by 73%-97%. EPE Count is also reduced by 91%-100% in resist CD and 72%-98% in etch CD. AFCorr facilitates additional SRAF insertion by up to 10.8%. Dummy Count also increases by 18.6%. The increases of data size and OPC running time of EtchCorr are within 3% and 4%, respectively, and the observed maximum delay overhead of 6% is within the inherent noise of the P&R tool.[11] The runtime of EtchCorr placement perturbation is negligible ($\sim$ 5 minutes) compared to the running time of OPC ($\sim$ 2.5 hours).

We are currently engaged in further experimental validation and research. Our ongoing research is in the following directions.

- Restricted design rules are gaining support in the industry. Part of our ongoing work analyzes "correct-by-construction" standard-cell layouts which are always EtchCorrect in any placement scenario. We intend to compare such an approach with EtchCorr placement perturbation in terms of design as well as manufacturability metrics.
- Certain devices and cells may be able to tolerate more process variation than others in the design. We are investigating techniques to bias the AFCorr and EtchCorr solution in favor of such devices to reduce timing and power impact and increase overall parametric yield.

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