On the Intrinsic Rent Parameter and Spectra-Based Partitioning Methodologies*

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Abstract

The complexity of circuit designs has necessitated a top-down approach to layout synthesis. A large body of work shows that a good partitioning hierarchy, as measured by the associated Rent parameter, will correspond to an area-efficient layout. We define the intrinsic *Rent parameter of a netlist to be a lower bound on the Rent parameter of any partitioning hierarchy for the netlist. Experimental results show that spectra-based ratio cut partitioning methods yield partitioning hierarchies with the lowest observed Rent parameter over all benchmarks and over all algorithms tested. For examples where the intrinsic Rent parameter is known, spectral ratio cut partitioning yields a Rent parameter essentially identical to this theoretical optimum. We provide additional theoretical results supporting the close relationship between spectral partitioning and the intrinsic Rent parameter. These results have deep implications with respect to the choice of partitioning algorithms and new approaches to layout area estimation.*

1 Introduction

As VLSI system complexity and the number of implementation alternatives continue to increase, top-down approaches have been widely adopted for layout synthesis. This need for effective high-level partitioning algorithms has gained visibility in many arenas. Certainly, early design decisions in system partitioning will constrain all subsequent decisions, and good solutions to the placement, global routing and detailed routing problems often depend on the user having selected a high-quality partitioning algorithm.

Partitioning essentially tries to discover the natural circuit structure, i.e., a hierarchy of subcircuits which minimizes connectivity between subcircuits. A simple observation is that wires tend to be longer at higher levels of the physical hierarchy, so that strong hierarchical organization of the design can lead to less wiring area in the layout. Within this context, traditional wireability analysis and area prediction both essentially entail finding a partitioning algorithm that can consistently discern the "intrinsic netlist structure", and more specifically, the intrinsic netlist structure with respect to embedding in a planar layout region.

Previous work in the field of area estimation has shown that the so-called Rent parameter [12] is an accurate indicator of the wiring requirements for a given partitioning hierarchy. In particular, given a choice between two recursive bipartitioning hierarchies, the one with lower Rent parameter will require less wirelength and correspond to a denser final layout. Thus, one aspect of our present work compares various partitioning algorithms with respect to the Rent parameters of their induced partitioning hierarchies, with the goal of identifying the partitioning strategy whose hierarchy is closest to optimal. To this end, we introduce the notion of an *intrinsic* Rent parameter of a given netlist: the intrinsic Rent parameter is a lower bound on the Rent parameter of any partitioning hierarchy for the netlist. Such a lower bound gives a measure of the *required* layout area, independent of layout strategy. This affords a new methodology for comparing the utility of partitioning algorithms which is independent of possible differences between their individual objective functions.

Extensive experimental results show that so-called spectra-based (that is to say, based on computing eigenvalues and eigenvectors of particular netlist-derived matrices) partitioning algorithms are significantly superior to traditional iterative methods such as the Fiduccia-Mattheyses k-opt approach. We have found that an algorithm which recursively partitions an eigenvector-based linear ordering of the modules, subject to the *ratio cut* objective, yields a partitioning hierarchy which has Rent parameter uniformly better than that of any other method. Moreover, with each example for which the the intrinsic Rent parameter was known, the spectra-based ratio cut partitioning method yielded a Rent parameter essentially *identical* to this theoretical LB.

This result has key implications in two areas. First, it provides strong confirmation of previous work by Wei and Cheng [17], who were the first to propose the ratio cut partitioning objective; it also confirms work of Hagen and Kahng [6], who proposed using the spectral approach for ratio cut partitioning. Second, a natural application of our work lies in the development of better predictive layout tools, which

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are critical to efficient search of the layout solution space. Most approaches are based on a mix of so-called constructive and analytic techniques [11], i.e., they meld a partial "top-down" netlist partitioning structure with "bottom-up" estimates for each of the leaves of the partitioning hierarchy, based on statistical models for particular place/route strategies. Our work has deep consequences for both aspects of this estimation process: (i) it suggests that the traditional Fiduccia-Mattheyses bisection approach might well be replaced by spectral ratio cut partitioning, and (ii) it affords entirely new analytic techniques based on spectral computations.

Given that spectral ratio cut partitioning is a demonstrably preferable approach to building the layout hierarchy, our second avenue of inquiry pursues a theoretical relationship between the spectral properties and the intrinsic Rent parameter of a given netlist. We describe Rent's relationship as a natural outgrowth of ratio cut partitioning and the ratio cut cost function. Based on this relationship, we show that Rent's parameter can be analytically related to the theoretically derived lower bound on the ratio cut metric presented in [6]. Extensive experiments confirm this relationship, with our results again suggesting new spectra-based approaches to wireability analysis and layout area estimation.

2 Rent's Rule

Rent's rule is an empirical relation observed in "good" layouts; it reflects a power-law scaling of the number of external terminals of a given subcircuit with the number of modules in the subcircuit. Specifically,

$$T = k \cdot C^p \tag{1}$$

where T is the average number of external terminals (pins) in a subcircuit or partition; k is *Rent's constant*, a scaling constant which empirically corresponds to the average number of terminals per module; C is the number of modules in the subcircuit (or partition); and p is the *Rent parameter* or *Rent exponent*, with $0 \leq p \leq 1$.

This relation was first observed by E. F. Rent of IBM in the late 1960s and independently by several others. Landman and Russo [12] performed an extensive study of the relation via partitioning experiments on large "real-life" circuits, and observed Rent parameter values p between 0.47 and 0.75.[1] Following Mandelbrot [14], one may view Rent's rule as a dimensionality relationship between pinout of a module and the number of gates in the module. This is in some sense a surface area to volume relationship where, for example, "intrinsically 2-dimensional" circuits such as memory arrays, PLAs, or meshes will have optimal layouts with $p = 1/2$. Kurdahi and Parker [10] have noted that a Rent parameter value $p > 0.5$ implies that wires *must* grow longer as circuit size increases; in other words, such a circuit cannot be embedded in two dimensions without "dilation", and the *relative* contribution of wiring to layout area will grow with the size of the circuit. For example, a 3-dimensional mesh topology requires a layout having $p \geq 2/3$ [9], and indeed such a topology cannot be embedded in the plane without the introduction of long wires. Note that the tractability of the intrinsic Rent parameter analysis for meshes will allow us to use 2-D and 3-D meshes as supplementary benchmarks for which the intrinsic Rent parameter is known.

The value of the Rent parameter strongly affects the layout area of a given circuit. Donath and Feuer [1] and [3] proposed and experimentally verified relationships between the Rent parameter and the average wire length. Their work shows that a lower Rent parameter will result in lower average wire length, which in turn generally implies smaller wiring area and less congestion in the layout.[2] These results motivate our use of the Rent parameter for a given partitioning hierarchy as a measure of the quality for the corresponding partitioning algorithm.

Landman and Russo in [12] also made the fundamental observation that the Rent parameter will depend upon both the structure of the circuit and the partitioning algorithm chosen. This observation leads to the notion of an *algorithm-dependent* Rent parameter, which we may denote as $p_H(C)$ to indicate that the Rent parameter p is a function of both the circuit design C and the partitioning heuristic H. In other words, realizations of a given design will have differing Rent parameters depending on the underlying partitioning approach; correspondingly, any hierarchical partitioning algorithm will yield a family of Rent parameter values over the space of logic designs. With this in mind, the present work proposes the notion of an *intrinsic Rent parameter*, denoted by p^*, which is the *minimum* Rent parameter attained over all hierarchical decompositions of a given circuit. The intrinsic Rent parameter $p^*(C)$ is thus the infimum of the set of all possible $p_H(C)$ values.

A motivating hypothesis for our work is that the algorithm-dependent Rent parameter can be used to characterize the quality of a given partitioning heuristic H with respect to the given input. As will be seen below, different partitioning algorithms indeed yield widely varying Rent parameters for any given circuit, implying that the wirelength depends considerably on the choice of the partitioning algorithm used in the layout process. Moreover, our experimental results demonstrate that the relative ordering of algorithm-dependent Rent parameters is very consistent across

[1] In a subsequent paper [15], Russo concluded that, for a given fixed partitioning algorithm, p tends to be high for high performance circuits, and low for low performance circuits. As simple examples, consider that $p = 0$ for a shift register in which data is loaded serially, and $p = 1$ for a latch circuit where data is loaded in parallel.

[2] Cf. the practical wirelength estimation approaches of Donath [1] and Feuer [3] which involve Rent-based analysis. Wirelength estimates are intimately tied to layout wireability analysis [7], and moreover form the basis of analytic area estimation methods, e.g., El Gamal, Kurdahi, and Sastry [2] [10] [16], which are typically used to complement constructive approaches [11].

a variety of benchmark circuits. The Rent parameter can thus be used to objectively select among partitioning heuristics for use in a hierarchical layout approach. Before presenting experimental results, we briefly review a taxonomy of those partitioning algorithms which are of interest in the dual contexts of hierarchical layout and rapid area estimation.

3 A Partitioning Taxonomy

Two widely used formulations for circuit partitioning are:

- **Minimum-Cut Bisection:** Given $G = (V, E)$, find the partition of V into disjoint U and W, with $|U| = |W|$, such that $e(U, W)$, i.e., the number of edges in $\{(u, w) \in E | u \in U \text{ and } w \in W\}$ is minimized.
- **Minimum Ratio Cut:** Given $G = (V, E)$, find the partition of V into disjoint U and W such that $\frac{e(U,W)}{|U| \cdot |W|}$ is minimized.

Because minimum-cut bisection divides module area evenly, it is a popular objective for hierarchical layout approaches. However, the area bisection requirement is unnecessarily restrictive and can preclude finding natural structure within the circuit. With this in mind, the ratio cut formulation [17] allows a tradeoff between nets cut and evenness in the partition: the numerator captures the minimum-cut criterion while the denominator favors near-bisection. It is well known that both minimum-cut bisection and minimum ratio cut are NP-complete [5], (the latter by reduction from Bounded Min-Cut Graph Partition) so heuristic methods must be used. Previous approaches fall into several classes, as surveyed in [6] [13].

The greedy iterative paradigm is popular either as a stand-alone strategy or as a postprocessing refinement to other methods. Iterative methods are based on local perturbation of the current solution and typically entail variations of the Kernighan-Lin method [8], particularly the algorithmic speedup of Fiduccia and Mattheyses [4]. Practical implementations will use a number of random starting configurations and return the best result [13] [17] in order to adequately search the solution space and give predictable performance, or "stability". For example, Wei and Cheng [17] propose a ratio cut heuristic that adapts the shifting and group swapping methods of [4] and returns the best of 20 runs. It should be noted that current wireability analysis algorithms rely almost exclusively on Fiduccia-Mattheyses partitioning. This is due to such reasons as: (i) the long history of Kernighan-Lin k-opt methods in physical layout, (ii) the natural use of bisection in hierarchical decomposition, and (iii) the simplicity of the algorithm implementation. However, certain limitations loom as problem sizes grow large. These include theoretical results on the weakness of local-search methods, as well as instability and the lack of error bounds; all of these factors seem endemic to *local* strategies.

With respect to the present work, an important class of partitioning algorithms consists of "spectral" methods which use eigenvalues or eigenvectors of matrices that are derived from the netlist graph. The circuit netlist may be represented by a simple undirected graph $G = (V, E)$ with $|V| = n$ vertices $v_1, \ldots, v_n$, and we use the $n \times n$ *adjacency matrix* $A = A(G)$, where $A_{ij} = 1$ if $\{v_i, v_j\} \in E$ and $A_{ij} = 0$ otherwise. If G has weighted edges, then A_{ij} is equal to the weight of $\{v_i, v_j\} \in E$, and by convention $A_{ii} = 0$ for all $i = 1, \ldots, n$. If we let $d(v_i)$ denote the degree of node v_i (i.e., the sum of the weights of all edges incident to v_i), we obtain the $n \times n$ *diagonal matrix* D defined by $D_{ii} = d(v_i)$. The eigenvalues and eigenvectors of such matrices are the subject of the field of graph theory dealing with *graph spectra*.

Early theoretical work connecting graph spectra and partitioning as surveyed in [13] formulate the partitioning problem as the assignment or placement of nodes into bounded-size clusters or chip locations. The problem is then transformed into a quadratic optimization, and Lagrangian relaxation is used to derive an eigenvector formulation. In [6], Hagen and Kahng established a close relationship between the optimal ratio cut cost and the second-smallest eigenvalue of the matrix $Q = D - A$, where D and A are as defined above:

Theorem 1 (Hagen-Kahng): Given a graph $G = (V, E)$ with adjacency matrix A, diagonal degree matrix D, and $|V| = n$, the second smallest eigenvalue λ of $Q = D - A$ gives a lower bound $c \geq \frac{\lambda}{n}$ on the cost c of the optimal ratio cut partition. □This result suggests that the eigenvector x corresponding to λ, i.e., the solution of the matrix equation $Qx = \lambda x$, be used to guide the partitioning. For ratio cut partitioning, [6] used x to induce a linear ordering of the modules, and the best "split" in terms of ratio cut cost was returned. To be more specific, the n components x_i of the eigenvector may be sorted to yield an ordering $v = v_1, \ldots, v_n$ of the modules which we call the *spectral ordering*. The splitting rank r, $1 \leq r \leq n - 1$, is then found which yields the best ratio cut cost when modules with rank $> r$ were placed in U and modules with rank $\leq r$ were placed in W. This straightforward construction achieved very significant improvements over previous iterative methods, and also exhibited several desirable traits, including speed, provability, and stability. The spectral method is appealing for its use of global rather than local information, and it also provides an *inherently spatial* embedding of the circuit graph. Because the spectral approach significantly outperforms iterative Fiduccia-Mattheyses style methods [6], Section 4 uses the spectral ordering as the basis for ratio cut partitioning variants.

4 The Intrinsic Rent Parameter: Experimental Results

Within the preceding taxonomy, the main classes of partitioning algorithms of interest for top-down layout generation are greedy iterative methods (in particular, Fiduccia-Mattheyses minimum-cut bisection) and methods that are based on the spectral ordering. Within these classes, we parametrize the algorithms of

interest by (i) their objective function: net cut metric or ratio cut metric; and (ii) the balance restrictions in the output bipartition: exact bisection, 1/4 - 3/4 range limited, or no limits on range. The following algorithms were used in our experiments:

- SpecRC-Full: spectral ordering; partition the ordering at best splitting point by ratio cut metric.
- SpecRC-1/4: spectral ordering; partition the ordering at best splitting point by ratio cut metric, subject to the constraint that maximum partition size is $\leq \frac{3}{4} \cdot |V|$.
- Spec-Bis: spectral ordering; bisect the ordering. In other words, "spectral bisection".
- FM-1/4: Fiduccia-Mattheyses minimum net-cut partitioning, with maximum partition size $\leq \frac{3}{4} \cdot |V|$.
- FM-Bis: the "standard" Fiduccia-Mattheyses minimum net-cut bisection.[3]

As a control, we also considered three variants of random circuit partitioning; it is easy to see tat random partitioning hierarchies will have expected Rent parameter equal to 1 [15].

- RandMC-1/4: random linear ordering; partition at best splitting point by minimum net cut metric, with maximum partition size $\leq \frac{3}{4} \cdot |V|$.
- RandRC-1/4: random linear ordering; partition at best splitting point by ratio cut metric, with maximum partition size $\leq \frac{3}{4} \cdot |V|$.
- Rand-Bis: random linear ordering; bisect the ordering.

The partitioning strategies were tested on three circuits from the MCNC benchmark suite: Primary1, Primary2, and Struct. The sizes of these circuits vary from 800 modules (Primary1) to close to 3000 modules (Primary2). Struct is a particularly interesting circuit since it is an array multiplier with a mesh-like topology, meaning that its intrinsic Rent parameter is likely to be 1/2. In addition, we tested the partitioning methods on Mesh2D, a 2-dimensional mesh topology, as well as Mesh3D, a three-dimensional mesh topology; for these inputs, the intrinsic Rent parameters are respectively known to be 1/2 and 2/3. Note that in general, it does not seem possible to evaluate the intrinsic Rent parameter for arbitrary circuits. Thus, Struct, Mesh2D and Mesh3D are very useful, since they allow us to assess the near-optimality of various algorithm partitioning hierarchies. In general, it does not seem possible to evaluate the intrinsic Rent parameter for arbitrary circuits. Table 1 summarizes the characteristics of the benchmark circuits.

The experiments were performed as follows. Each partitioning algorithm was used to construct a partitioning hierarchy for the circuit via recursive partitioning of the circuit and its subpartitions until all subpartitions contained less than 9 modules. At each

[3] We selected the FM-based Rent parameter as the minimum of 10 independently run FM-based partitioning hierarchies.

Benchmark	cells	nets	pins	pads
Primary1 (P1)	752	904	2941	81
Primary2 (P2)	2907	3029	11226	107
Struct (St)	1888	1920	5471	64
Mesh2d (2D)	2000	4090	8000	180
Mesh3d (3D)	1000	3300	6000	600

Table 1: Benchmark Circuit Characteristics

partitioning step, we noted the size and number of external pins for each subpartition.

We next established *levels* within the partitioning hierarchy, with each level containing a set of disjoint subpartitions of roughly equal size. The average size and average number of pins of the subpartitions in these partition levels yield the data points from which the Rent parameter is extracted. We generated these partition levels in two different ways: (i) by traversing the partitioning hierarchy in a breadth-first manner, i.e. a partition level consists of all subpartitions at a given depth in the hierarchy; and (ii) by defining a partition level to be a set of k subpartitions containing all modules, subject to the constraint that the maximum subpartition size is minimized. Traversal method (ii) derives partition levels by traversing the partitioning hierarchy as described in Figure 1: partition level P_{k+1} with $k+1$ subpartitions is constructed from partition level P_k with k subpartitions by replacing the largest subpartition in P_k by its two children in the partitioning hierarchy.

Partition-Level-Generator(H_P)
Input: H_P a partitioning hierarchy
Output: P_k a sequence of k-way partitions, $k = 2, \ldots, n$
let $k = 1$
let P_k = the complete circuit
let $big = P_k$
while big is partitioned in H_P
  $k = k + 1$
  $P_k = P_{k-1} - big$
  $P_k = P_k \cup$ subpartitions of big in H_P
  Output P_k
  big = largest subpartition of P_k

Figure 1: Traversal (ii) partition level generation.

For a partitioning hierarchy based on bisection, the partition levels produced by traversal (i) will be a subset of the partition levels of traversal (ii). However, as the balance restrictions are loosened, the two traversals give different results. Using traversal (i), the lower levels may include only a subset of the circuit if previous levels contain subpartitions that are leaves. On the other hand, any traversal (ii) level will

always include the complete circuit, and moreover for 1/4 – 3/4 range limited partitioning the ratio between the largest and smallest non-leaf subpartitions in any given level will be less than or equal to three.

In order to correlate the experimental data to Rent's rule, we re-express the relationship $T = kC^p$ as $\log T = \log k + p \cdot \log C$, which is a straight line equation with intercept $\log k$ and slope equal to the Rent parameter p. From this formula, we see that the Rent parameter p can be calculated by performing linear regression on the data points plotted on a *log-log* scale. Our plotted data points represent the average[4] number of external terminals and modules per subpartition for each partition level.

Last, we followed the methodology of [12] and divided our data points into two regions: Region I where Rent's rule applies (and wherein we perform the regression), and Region II where the rule breaks down. For traversal (i), in no instance were more than the first two levels of the partitioning tree assigned to Region II; for traversal (ii), the number of levels assigned to Region II ranged from 0 to 7.

Calculations of the Rent parameters for the different partitioning variations are summarized in Tables 2 and 3. Since the results for all the Rand variants gave essentially identical Rent parameters we chose Rand-Bis as a representative from this category to compare with the other partitioning algorithms.[5]

Partitioning strategy	Rent parameter (p)				
	P1	P2	St	2D	3D
Rand-Bis	.880	.931	.923	.942	.936
FM-Bis	.736	.794	.848	.681	.689
FM-1/4	.606	.736	.713	.573	.691
Spec-Bis	.660	.706	.598	.524	.613
SpecRC-1/4	.396	.640	.516	.554	.655
SpecRC-Full	.196	.491	.510	.546	.666

Table 2: Rent parameter results using traversal (i).

The results indicate that SpecRC-1/4 and SpecRC-Full generate partitioning hierarchies with uniformly better Rent parameters for all test circuits. For Struct and the mesh inputs, where we know the value of the intrinsic Rent parameter, we see that the spectral ratio cut variants, in particular SpecRC-1/4 and SpecRC-Full, give partitioning hierarchies with Rent parameters very close to the theoretical value of 1/2 for Struct and Mesh2d, and 2/3 for Mesh3d. As expected, the Rent parameters for random partitioning are very close to 1 for all benchmark circuits.

Last, we note that our conclusions are strengthened when we take into consideration the quality of the fit between our data and the regressed line. Figure 2 shows a graph depicting the data points and their regressed lines for the Struct benchmark, using the traversal (i). Virtually every example had correlation coefficient higher than .98, indicating a consistently good fit.[6]

Partitioning strategy	Rent parameter (p)				
	P1	P2	St	2D	3D
Rand-Bis	.916	.951	.935	.970	.953
FM-Bis	.723	.933	.878	.663	.711
FM-1/4	.670	.772	.726	.563	.720
Spec-Bis	.662	.693	.635	.514	.620
SpecRC-1/4	.574	.658	.580	.540	.654
SpecRC-Full	.456	.617	.572	.524	.660

Table 3: Rent parameter results using traversal (ii). Numbers in parentheses show the points belonging to Region II.

Figure 2: Rent's rule fit for Struct using traversal (i)

5 A λ-Rent Relationship

The empirical results presented above suggest that the smallest Rent parameter is derived when we use the ratio cut metric for partitioning. In view of the proposed concept of an intrinsic Rent parameter, this suggests that the spectral ratio cut approach is in some sense an intrinsically good top-down partitioning strategy. This section presents theoretical arguments and empirical results which support this conclusion.

Given a circuit C, let U and W be the partitions re-

[4] While previous work has calculated the Rent parameter [12] using arithmetic averaging, we derive the experimental data below using geometric averaging at each partition level; this a more "natural" average on the log-log scale. The distinction between geometric and arithmetic averaging is irrelevant vis-a-vis bisections, and hence the analysis given in previous work (all of which derives Rent's relationship using bisection methods) holds with either averaging method. Thus, our choice of geometric averaging still allows direct comparison with previous studies of Rent's parameter.

[5] Also note that the Rent parameters for all bisection variants should be the same using either traversal (i) or (ii); however, slight differences result from the fact that the traversal (i) data points used in the regression are a subset of the data points used to calculate the Rent parameter for traversal (ii).

[6] The sole exception: Primary1 with traversal (i) for SpecRC-Full, where the fit was done on only five data points.

sulting from applying a spectral ratio cut partitioning to C. Theorem 1 [6] gives the following lower bound on the value of the ratio cut cost:

$$\frac{e(U,W)}{|U|\cdot|W|} \geq \frac{\lambda}{n} \tag{2}$$

Assuming the optimal ratio cut partition of C achieves this lower bound[7], we have:

$$\frac{e(U,W)}{|U|\cdot|W|} = \frac{\lambda}{n} \tag{3}$$

If Rent's rule holds for partitions U and W, then we must also have

$$e(U,W) = k \cdot [Avg(|U|,|W|)]^{p^*}$$

where $Avg(|U|,|W|)$ denotes the average of $|U|$ and $|W|$, k is Rent's constant and p^* is the intrinsic Rent parameter. Assuming that $Avg(|U|,|W|)$ is computed as the geometric average, we may rewrite Rent's relationship for U and W as

$$\begin{aligned} e(U,W) &= k\left[(|U|\cdot|W|)^{\frac{1}{2}}\right]^{p^*} \\ &= k\,(|U|\cdot|W|)^{\frac{p^*}{2}} \end{aligned} \tag{4}$$

We can also compute $e(U,W)$ from (3) as:

$$e(U,W) = \frac{\lambda}{n}(|U|\cdot|W|) \tag{5}$$

Setting $|U| = x^*$, (5) and (5) together yield the approximate relationship

$$\frac{\lambda}{n}x^*(n-x^*) = k\,[x^*(n-x^*)]^{\frac{p^*}{2}}$$

or

$$\frac{\lambda}{n} = k\,[x^*(n-x^*)]^{\frac{p^*}{2}-1} \tag{6}$$

which strongly suggests a close relationship between λ and the intrinsic Rent parameter p^*. Indeed, the relationship (6) may be viewed as a new characterization of the scaling properties of circuit netlists.

To validate the relationship in (6), we performed the following experiment. First, we observe that (6) implies that $\frac{\lambda}{n}$ can be plotted versus $x^*(n-x^*)$ on a log-log scale as a straight line with slope $\frac{p^*}{2}-1$. Based on this observation, our task of experimentally validating the relation in (6) is reduced to testing the fit of the partitioning data obtained from our experiments to a straight line on a log-log plot. Given a spectra-based partitioning method (e.g., Spec-Bis, SpecRC-1/4, or SpecRC-Full), we computed average $x^*(n-x^*)$ and $\frac{\lambda}{n}$ values for each partition level in the partitioning hierarchy. In order to obtain an average point for each level of the hierarchy, we geometrically averaged the x-values (i.e., the $x^*(n-x^*)$ values). Both geometric and arithmetic averaging of the y-values (i.e., $\frac{\lambda}{n}$) were used, with the latter giving much better fits.

Figure 3: Experimental validation of the λ-Rent relationship for Struct using traversal (i)

For every benchmark circuit, we plotted the data corresponding to Spec-Bis, SpecRC-1/4, and SpecRC-Full. In each case, we performed a linear regression and estimated the slope of the regression line. Only the data which was found to belong to Region I in Rent's relationship (as described in Section 4) was included in the fit. From this data, we used a procedure similar to the one used in Section 4 to locate the region, which we call Region A, where the relationship in Equation (6) is valid; remaining data points comprised Region B. In all the cases, Region B had no more than the first two points of each set (i.e. corresponding to the first two levels). Figure 3 shows typical results using traversal (i). Although the fits are not quite as good as those pertaining to the Rent parameter in Section 4 above, the data gives a clear indication that the relationship in Equation (6) holds.[8]

Table 4 compares the slope of the regression line fit to the data and the one predicted by Equation 6 using the estimated Rent parameter from Table 2. We notice that the range of slopes is well within what is predicted by the λ-Rent relationship: if $0 \leq p \leq 1$, then $-1 \leq (\frac{p}{2}-1) \leq -0.5$. All the slopes were in the

[7] footnote about how this seems true for graph partition within small constant factor...

[8] There are several sources of error that would potentially affect the goodness of the fit: (1) the relationship derived in Theorem 1 assumes a graph model whereas the circuits are actually hypergraphs with an average net fanout of around 3.5; (2) the relationship in Equation (6) assumes that the lower bound on the ratio cut function predicted by Theorem 1 can be achieved exactly, which may not always be the case; (3) the points on the graph corresponding to the first levels were otained by averaging a very small number of points and thus may not be as statistically significant as other data points; and finally, (4) a small percentage (about 10%) of the partitioning data was discarded because the eigenvalue computations resulted in floating point errors.

range $[-.99, -.64]$. Generally speaking, there is a reasonable agreement between the estimated slopes and the predictions based on Rent's relationship. The only exceptions arise with the Mesh2d benchmark, where for SpecRC-Bis and SpecRC-1/4 we find a relatively large difference (about 25%). Overall, the experimental data strongly confirms the relationship proposed in Equation (6).

Partitioning strategy	calculated p				
	P1	P2	St	2D	3D
Spec-Bis	.38	.48	.72	.02	.58
SpecRC-1/4	.22	.58	.56	.18	.52
SpecRC-Full	.20	.68	.46	.54	.50

Table 4: Experimental validation of the Rent-Eigenvalue relationship using traversal (i) — Summary of results. The numbers indicate the calculated Rent parameter p from the slope s with $p = 2(s+1)$.

6 Future Work and Conclusions

We are currently integrating spectral ratio cut partitioning into a top-down layout package, to verify that spectral partitioning will indeed give denser layouts. Other possible extensions of this work include estimating the Rent parameter from the first 3 or 4 levels of the partitioning hierarchy, or by Monte Carlo traversals of root – leaf paths in the partitioning hierarchy. Our conjecture is that either of these methods will give very accurate Rent parameter estimates, thereby reducing the time needed to estimate the wirelength requirements of a candidate layout. Another possibility is to compute the Rent parameter from the λ values of the first few partitioning levels. This latter methodology is dependent on the accuracy of the hypergraph model, and we are currently looking into possibly better ways of transforming the hypergraph to a graph.

In conclusion, we have introduced the notion of a circuit's "intrinsic Rent parameter" defined as the lowest Rent parameter achievable by any partitioning method. Our empirical results indicate that spectral ratio cut partitioning methods generate partitioning hierarchies whose Rent parameters are lower than those of any other algorithms tested, and which are moreover optimal in those examples where the intrinsic Rent parameter is known. In particular, comparisons of the partitioning hierarchies generated by spectral and Fiduccia-Mattheyses based partitioning methods show that with all benchmarks the spectral partitioning hierarchy is superior to the hierarchy generated by Fiduccia-Mattheyses based partitioning. This result suggests that top-down layout techniques based on spectral ratio cut partitioning methods will achieve denser layouts than the current tools based on Fiduccia-Mattheyses style partitioning.

We also suggest a relationship between the second smallest eigenvalue of the connectivity matrix and the intrinsic Rent parameter for any circuit, with this relationship given by $\lambda/n = k\,[x^*(n-x^*)]^{\frac{p^*}{2}-1}$. Our empirical analysis of the λ values for subpartitions in hierarchies generated using spectral ratio cut partitioning shows that this relationship indeed holds, giving further support to the notion that spectral partitioning generates partitioning hierarchies with Rent parameters equal to the circuits' intrinsic Rent parameters.

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