Toward a Methodology for Manufacturability-Driven Design Rule Exploration*

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ABSTRACT

Resolution enhancement techniques (RET) such as optical proximity correction (OPC) and phase-shift mask (PSM) technology are deployed in modern processes to increase the fidelity of printed features, especially critical dimensions (CD) in polysilicon. Even given these exotic technologies, there has been momentum towards less flexibility in layout, in order to ensure printability. However, there has not been a systematic study of the performance and manufacturability impact of such a move towards restrictive design rules. In this paper we present a design flow that evaluates the application of various restricted design rule (RDR) sets in deep submicron ASIC designs in terms of circuit performance and parametric yield. Using such a framework, process and design engineers can identify potential solutions to maximize manufacturability by selectively applying RDRs while maintaining chip performance. In this work we focus attention on the device layer which is the most difficult design layer to manufacture. We quantify the performance, manufacturability and mask cost impact of several common design rules. For instance, we find that small increases in the minimum allowable poly line end extension beyond active provide high levels of immunity to lithographic defocus conditions. Also, modification of the minimum field poly to diffusion spacing can provide good manufacturability, while a single pitch single orientation design rule can reduce gate 3σ uncertainty. Both of these improve in data volume as well, with little to no performance penalties. Reductions in data volume and worst-case edge placement error are on the order of 20-30% and 30-50% respectively compared to a standard baseline design rule set.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: IC; B.8.2 [**Hardware**]: Performance and Reliability; J.6 [**Computer Applications**]: CAD

General Terms

Design, Performance, Algorithms, Reliability

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Table 1: Projected L_{gate} CD control in sub-wavelength lithography regime

Year	2001	2004	2007	2009
Technology Node	130 nm	90 nm	65 nm	50 nm
MPU L_{gate} (nm)	90	53	35	28
CD Control (3σ) (nm)	5.3	3.75	***2.5***	***2.0***
MPU Pitch (nm)	300	214	160	130
Wavelength (λ) (nm)	248	193	193	157

Keywords

Process variation, Lithography, VLSI Manufacturability, OPC, RET, Yield

1. INTRODUCTION

Optical lithography has long been the key enabler for the continuation of Moore's Law. However, CMOS processes recently reached the sub-wavelength lithography regime (i.e., the wavelength of light is larger than the minimum feature size to be printed), making the critical dimension (CD) tolerances prescribed in the 2003 International Technology Roadmap for Semiconductors (ITRS) (see Table 1[1]) very difficult to achieve. This has brought about the need for correction techniques to enhance resolution and avoid unacceptably high circuit and critical path performance variation [1]. Resolution enhancement techniques (RETs) that address three degrees of freedom in lithography, *aperture*, *phase*, and/or *pattern uniformity*, are increasingly adopted in nanometer-scale design (i.e., 130 nm processes and beyond) with respect to not only the number of mask levels incorporating RETs but also the variety of techniques applied.

Due to the technological challenges of controllably printing very small features, the non-recurring engineering (NRE) and turn-around time (TAT) costs of correction (optical proximity correction (OPC), phase-shifting, dummy features) are very high in terms of design time and mask yield/verification. Many costs (yield, mask writing time, data volume, etc.) are directly proportional to the complexity of the shapes needed on the masks. Mask writing time has increased from just a few days to over a month due to RET complexity [2]. This brings up an important relationship between design type and lithography costs, namely, that the total cost to produce low-volume parts (such as most ASIC designs) is dominated by mask costs [3].

Designers and manufacturers are jointly faced with determining how best to apply RETs within current design flows to minimize mask cost while maintaining good circuit performance. Approaches have been taken to minimize RET cost, notably OPC costs that lead to large mask feature counts. For example, [4] reported up to 69% saving in RET cost without penalizing parametric yield, via use of selective OPC and OPC-aware standard cell libraries. Fur-

[1]Manufacturable solutions are not known for italicized numbers.

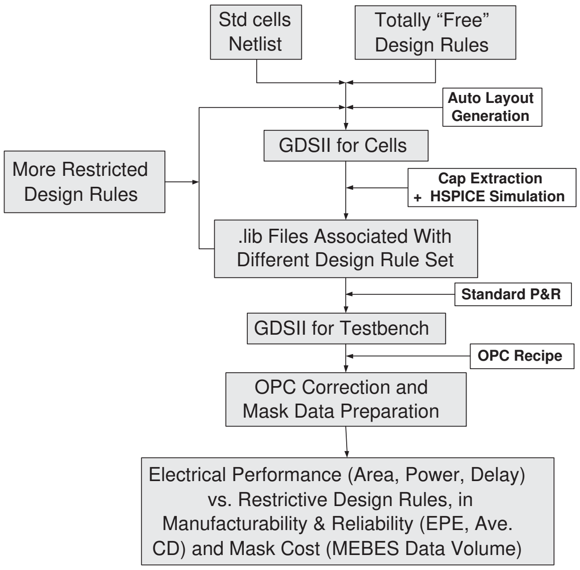

Figure 1: ASIC design flow targeting RDR evaluation.

thermore, although RETs have historically been a strictly post-layout procedure, they now need to become part of a cohesive design flow in which libraries and layouts are optimized directly based on conflicts discovered by the RET tool [5]. This "trickle-down" effect of RETs towards the design process is also manifested by more conservative design rules, particularly for the critical polysilicon layer. In particular, the ability to print very tight pitches as well as print a wide range of pitches in a given layer is very difficult for subwavelength lithographic systems. As a result, there is a trend towards limiting the range of allowed pitches in the polysilicon layer [6]. This type of restricted design rule (RDR) seeks to enforce a particular style of layout that is known to be highly manufacturable. As with any design rule, it is a tradeoff between manufacturability and performance, where performance can be measured as layout density, delay, power, etc. By nature, these RDRs seek to push the tradeoff more in favor of the manufacturing side, sacrificing performance in the process. Despite the move towards RDRs, there has been no comprehensive and systematic study of their expected impact on manufacturability and performance.

This paper presents an analysis of various RDR sets applied within an ASIC design methodology. We seek to minimize mask costs, maintain circuit performance, and enhance feature printability and reliability. Our primary contribution is in providing a framework for systematic study of the impact of restricted design rules for the polysilicon layer, for both performance and manufacturability. Through extensive lithographic simulation and integration with traditional ASIC design implementation, we show that RDRs can provide improved printability, yield, and reduced data volume with little performance impact as measured through delay, area, and power metrics. In the next section we describe the design flow used to incorporate and investigate various RDRs and introduce the candidate RDRs under study. Section 3 discusses our simulation results using various metrics to evaluate the efficacy of RDRs. Finally, Section 4 draws conclusions.

2. RDR EVALUATIVE METHODOLOGY

2.1 ASIC Design Flow Targeting RDR Evaluation

To evaluate the performance and manufacturability impact of restricted design rules, we set up the design flow shown in Figure 1. Initially we have a set of default design rules based on IBM 0.13 μm technology and a pruned standard cell netlist containing basic cell types such as BUF, INV, NAND, NOR, AND, OR, AOI, and OAI. We then create GDS representations for each cell with an automatic layout generation tool. After parasitic extraction, each cell is characterized for both timing and power performance to generate a .lib file. At this point we have the necessary infrastructure to proceed to synthesis/place and route (P&R).

The library generation process is repeated by altering the set of design rules through inclusion of a single candidate RDR, such as adding stricter requirements for poly gate spacing, minimum poly line end extension, etc. The goal of these added RDRs is to improve the final printability and reliability with as little performance impact as possible. We re-generate layouts and .lib files for a number of candidate RDR sets, then perform synthesis/P&R, and obtain timing, power, and area reports after back-annotation for several benchmark circuits. Note that the circuit topology is unchanged in all implementations of a given benchmark. That is, we do not re-synthesize the circuit with a new library but instead map the gate-level netlist to a new .lib and proceed with the back-end of the typical ASIC flow.

After circuits are placed and routed for each individual library, we perform OPC for each layout with a general but comprehensive model-based OPC recipe containing information such as the line end correction procedures, concave and convex corner correction instructions, etc.[2] The amount and impact of the applied RET is a function of the circuit layout which in turn depends on cell layout among other factors. Thus, we can evaluate how specific design rule changes impact both circuit performance (delay, area, power) and manufacturability/printability/mask cost as measured on MEBES data volume, histograms of resulting edge placement errors (EPE), etc. The next section contains more details about EPE and MEBES data volume. Specific EDA tools used within this overall flow are:

- Layout automatic generation - Prolific *Progenesis* [7];
- Physical capacitance extraction - Mentor Graphics *Calibre xRC* [8];
- Timing and power characterization tool - Synopsys *HSPICE* and *Powerarc* [9];
- Synthesis/P&R - Synopsys *Design Compiler* [9] and Cadence *Silicon Ensemble* [10];
- Back-annotated timing simulation - Synopsys *PrimeTime* [9];
- OPC layer generation, EPE extraction, and mask data preparation (MDP) - Mentor Graphics *Calibre RET* [8].

This section discusses candidate design rules that can be altered in an attempt to improve printability or manufacturability. Modern design rule manuals have hundreds of entries; we examine just a handful of possible RDRs on the polysilicon layer, which is the most critical for transistor performance, in order to draw concise conclusions. In particular, spacing between features is one of the most important rule types that affects circuit manufacturability: the light field of a given feature is greatly affected by the location of neighbor features, leading to CD variations that can result in loss of parametric yield. Most of the design rules we investigate therefore deal with either intra-layer or inter-layer spacings. As another example, minimal polysilicon overlap of diffusion is a critical design rule as it ensures that the edges of a MOSFET maintain consistency in dimensions with the interior portion of the channel.

Our starting point is a default flexible design rule set within which all spacing rules are at their minimum values and bent gates or 45-degree routes of poly are allowed (i.e.,

[2]All OPC-related results shown in this paper are extracted based on simulations on layout test patterns with industry optical and process environments.

Table 2: RDR default and modified values (note that the corresponding rule names appearing in all following figures are included in parentheses after values)

Rule name	Default(μm)	Modified(μm)	
Bentgate line width	"off" 0.12	"on", *baseline* 0.12 (bentgate)	"on" 0.14 (bent_w14)
Poly_poly space	0.20 (sp_20)	0.24 (sp_24)	0.28 (sp_28)
Poly_diffusion space	0.08	0.10 (pdsp_10)	0.12 (pdsp_12)
Poly end extension	0.28	0.34 (povg_34)	0.40 (povg_40)

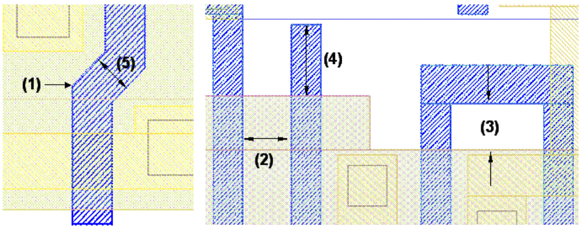

Figure 2: Layout illustrations of RDR candidates.

bentgate is "on"). From this point we construct restricted design rule sets by first turning bentgate "off" and then investigating the following rule categories: increased minimum poly to poly spacing, increased minimum field poly to diffusion spacing, larger minimum poly line end extension beyond diffusion, and also turning bentgate back on while increasing the minimal allowable linewidth in a bent gate structure. Figure 2 depicts layouts corresponding to the RDR candidates we investigate:

- Bentgate "on" as *baseline* (Figure 2 (1));
  - Bentgate line width (Figure 2 (5)).
- Bentgate "off"
  - Poly to poly spacing (Figure 2 (2));
  - Poly to diffusion spacing (Figure 2 (3)); and
  - Poly end extension (Figure 2 (4)).

2.2 RDR Candidates

Once the form of the specific RDRs are decided, we then seek to find the range of values that the RDRs should take on so that we can expect printability improvements. For example, it is clear that poly to poly spacing cannot be set below the value in the default design rule set since that spacing has already been determined to be the minimum allowable that ensures decent printability. To create more conservative design rules, we want to examine the impact of larger poly to poly spacings. However, if this spacing becomes too large it can actually jeopardize manufacturability since many modern lithography systems are not adept at printing intermediate pitch values [5].

To investigate the range of poly pitches that print well using our (fixed) OPC recipe, we use edge placement errors (EPE) as a quantifying metric. EPE is a common measure of how closely a printed feature actually reflects the corresponding designed feature. The EPE value is defined as the distance between the edge of the actual printed image

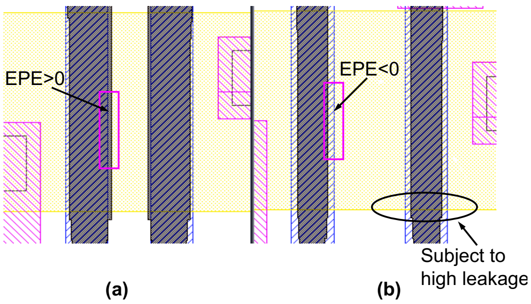

Figure 3: Edge placement error (EPE) definition.

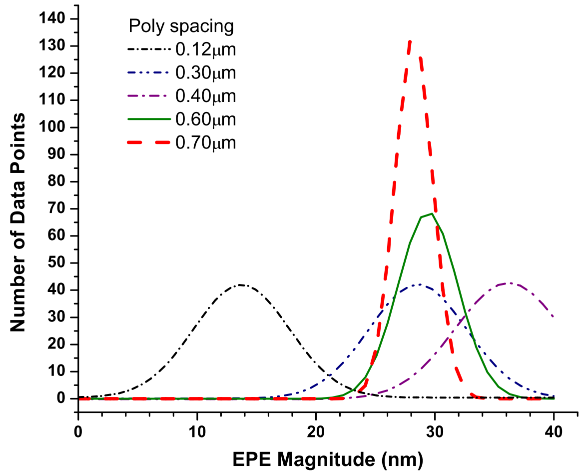

Figure 4: Impact of pitch on the EPE histogram of a NAND2X2 without OPC.

and the edge of the drawn feature and takes on a negative (resp. positive) value if the printed feature is contained within (resp. lines outside) the drawn feature boundary, as shown in Figure 3. Usually EPE has larger magnitude near the ends (along the width dimension) of a transistor gate; this implies that in small-width gates the impact of CD variability is relatively larger and that the edges of a device may exhibit substantial leakage currents since a smaller-than-nominal channel length leads to exponentially more subthreshold leakage through short-channel effects [11]. This also points to line end extension rules as a possible RDR. As indicated in Figure 4, with a more restrictive minimum poly to poly spacing rule the EPE distribution of a NAND2X2 (2-input NAND of size 2) without OPC shows a consistent left shift until it reaches approximately $0.70\mu m$ at which point it then moves back to tighter distributions. In general, with modern off-axis illumination approaches such as annular or quadrupole illumination there is a pitch range where the optical diffraction results in poor printed images (in this paper, this manifests as larger EPEs). This pitch region, determined by the details of the entire lithography process, is sometimes referred to as the *forbidden pitch* range, and should be avoided by IC designers. As can be seen, the EPE (or CD) variation becomes smaller for isolated lines but the average value increases. This behavior can be attributed to the fact that the radius of influence of optical diffraction effects extends to approximately $0.6\mu m$ and any pitch above that prints similarly poorly [12]. In our study, we define $0.42\ \mu m$ to $0.72\ \mu m$ (equivalent to $0.30\ \mu m$ to $0.60\ \mu m$ poly spacing where poly width is set to its minimum value of $0.12\ \mu m$) as our forbidden pitch range. In our study, we investigate RDRs that take on the values shown in Table 2.

2.3 Evaluation Metrics for Manufacturability/Cost

As described above, EPEs are used as a measure of OPC effectiveness with a goal of zero EPE for all polygons forming transistor gates. However, an "edge" placement error does not provide complete insight to the actual critical dimension or CD - two edges (or EPEs) are needed to determine CD, indicating the need to localize each EPE and match it with the EPE value on the immediately opposing side of the polygon. Considering that each single transistor may actually have multiple CDs due to irregular printed image (i.e., transistor gate lengths can be non-uniform along the width dimension), we find an average CD for each transistor by calculating the gate and active overlap area with the simulated printed image and dividing it by the measured gate width. When CD is reported in the remainder of this

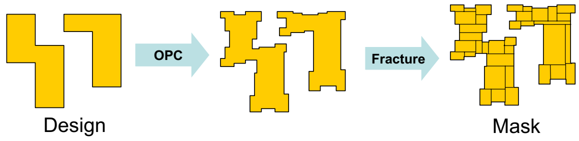

Figure 5: Mask data preparation (post OPC).

paper, it refers to the average gate-length calculated in this manner.

Moreover, we use the mask writer format (MEBES) data volume to evaluate the complexity of the resulting mask for the critical layer. We use this as an OPC or design-cost metric since GDSII files must be fractured into MEBES format (see Figure 5[3]) during mask data preparation and this step has become a serious bottleneck due to large figure counts from RETs. For out purposes, MEBES data volume reflects the complexity of an OPC layer which is impacted by the design rules used for that layer. In summary, EPEs and averaged CD variation are used as criteria for manufacturability while we use MEBES data volume to evaluate OPC cost.

3. TESTBED AND EXPERIMENTAL RESULTS

We use IBM 0.13 μm CMOS technology in the following simulations and ISCAS85 circuits as benchmarks to evaluate our .lib files. The descriptions of these testcases are as follows:

- c7552 - a 32-bit adder/comparator, the largest circuit in ISCAS85;
- c6288 - a 16×16 multiplier; and
- c5315 - a 9-bit ALU.

3.1 Impact of Defocus

Defocus in the lithography system is a key parameter that strongly affects the printability of fine resolution images since it determines the process window (defined as the range of exposure dose and defocus within which acceptable image tolerance is maintained). When the absolute amount of defocus exceeds a certain "best-focus" value, the printed features can go out of the CD variation tolerance, since only a limited depth of focus (DOF) is allowed in a lithography system. Four different defocus values, 0, 0.1 μm, 0.2 μm, and 0.3 μm are tested in our experiments. If not specifically mentioned, all designs are simulated at 0 defocus with a comprehensive model-based OPC recipe.

3.1.1 Impact of Defocus on Maximum EPE Levels

Figures 6 and 7 show the extracted maximum gate CD EPE tolerance (i.e., the maximum EPE observed for any gate in the specified design). As can be seen, with constant defocus, as poly spacing increases from 0.20 μm to 0.24 μm the maximum EPE tolerance either remains constant or decreases, demonstrating an impact on CD variation of this design rule. The maximum observed EPE nearly doubles as defocus rises to 0.3 μm, indicating that focus variation is a large contributor to CD variation as has been pointed out elsewhere [13]. Looking at the range of RDR sets, we first see that the default design rule set leads to very large EPEs, up to 40 nm for a 130 nm process. Furthermore, the simple removal of bent gates (shown as RDR set "sp_20") helps dramatically while further changes to the design rule set can also improve the worst-case EPE. The best RDR sets from these data sets are the "povg_34" set which increases the minimum poly overlap of active by 60 nm and the "sp_24" set which relaxes the poly-to-poly spacing by 20% relative to the baseline. We also note that the relaxation of some design rules (e.g., "pdsp_10") can actually worsen printability of some difficult features in a layout compared to the "sp_20" design rule set.

[3]Figure courtesy M. Reiger, Synopsys Inc.

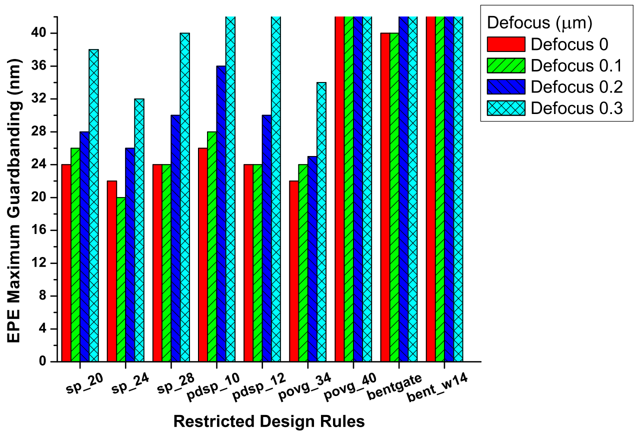

Figure 6: Impact of defocus on c6288.

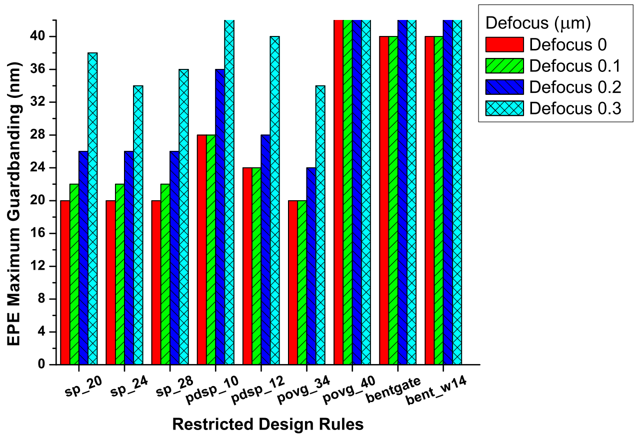

Figure 7: Impact of defocus on c7552.

3.1.2 Impact of Defocus on CD Distribution

To assess the impact of focus variation on CD, we use aerial image calculation which models optical effects[4]. The intensity level for aerial image simulation is fixed at the value which gives best aerial image for the "isofocal spacing"[5] at best-focus. Separately, the isofocal spacing is computed to be 200 nm by defocus simulations of a simple test structure. This intensity level was maintained constant with defocus. We then extracted the averaged CDs and their variation from aerial image contours, as shown in Table 3. The 200 nm poly-spacing rule prints the best through-focus as it results in cell layouts with inter-device spacings closest to the isofocal spacing. This suggests that intelligent choice of the min-poly spacing which is cognizant of the isofocal spacing as defined by the process can improve defocus characteristics of the design.

3.1.3 Impact of Defocus on Functional Yield

In [14], the allowed variability in physical gate length is fixed at 10%. This translates to an average maximum allowable EPE of 5% on each edge of the gate. Note that it is possible for a printed gate to have larger EPE on both sides and still maintain a nominal L_{gate} (i.e., positive and negative EPEs may appear simultaneously and cancel the effect of each other) but this increases the possibility of functional

[4]We ignore resist effects in this analysis as Calibre models are calibrated at best-focus and may not yield accurate print image results for defocus conditions.

[5]The spacing for constant width that has nearly zero variation through a range of defocus levels.

Table 3: Impact of defocus on extracted CD mean and variation (unit: nm)

	Defocus							
	0		0.1(μm)		0.2(μm)		0.3(μm)	
RDR	Mean	σ	Mean	σ	Mean	σ	Mean	σ
sp_20	147.2	7.79	140.2	7.98	138.3	8.08	136.2	7.99
sp_24	147.0	7.79	141.0	7.91	138.1	7.94	136.1	9.54
sp_28	146.7	7.97	139.8	7.84	137.7	7.54	134.8	8.67
pdsp_10	147.1	8.23	140.3	8.16	138.2	8.36	135.8	9.03
pdsp_12	147.1	8.48	141.2	8.23	137.9	8.44	135.5	8.55
povg_34	140.2	8.27	138.9	8.13	138.8	8.90	136.1	9.10
povg_40	140.5	9.58.	142.5	9.25	139.2	9.03	136.4	33.7
bentgate	146.9	8.03	139.1	7.60	135.7	7.41	132.6	7.97
bent_w14	147.0	7.80	139.3	7.36	135.4	7.13	132.9	7.08

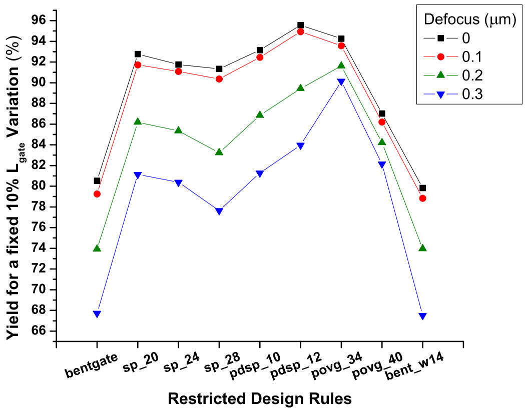

Figure 8: Functional yield for a fixed 10% L$_{gate}$ variation for c7552.

failure in a relatively dense circuit. To examine the fraction of printed gates in our benchmark circuits that meet this ITRS requirement, we define functional yield to be the percentage of total gates that print with less than 5% EPE for all fragments of the gate.

As seen in Figure 8, for nearly every RDR set the functional yield is rather sensitive to focus variation. This is expected since printability gets markedly worse when features are out of focus. However, we find that the RDRs associated with increased poly line-end extensions (povg_∗) show dramatically less sensitivity of functional yield to defocus. This implies that design rule sets that include relaxed (larger), poly line-end extension rules may have larger process windows which reduce manufacturing overhead/cost. We observe from the figure that the use of bent gates with off-axis illumination (as we are using) produces a large number of gates with substantial (>5%) EPEs. Finally, we also see that the "pdsp_12" design rule set provides a very high percentage of gates within the stated ITRS specification indicating it has promise as an RDR.

3.2 Scattering Bars

Isolated lines usually suffer more optical distortion effects than dense lines since lithography and RET recipes are not tuned or optimized for isolated lines. Although OPC corrects for the iso-dense bias at zero defocus, with non-zero defocus isolated lines tend to print narrower (or wider depending on the lithography system being used). Scattering bars (SBs), which are extremely narrow lines that do not actually print on the wafer, can modify the wavefront and reduce these distortions. However, liberal use of SBs adds considerable data volume in the MEBES format and places additional requirements on the resolution of the mask writing equipment. For the experiment of this section we modified our OPC recipe by adding scattering bars. These SBs are added whenever a poly line is fairly isolated; their impact is to make all poly lines in the design look similarly

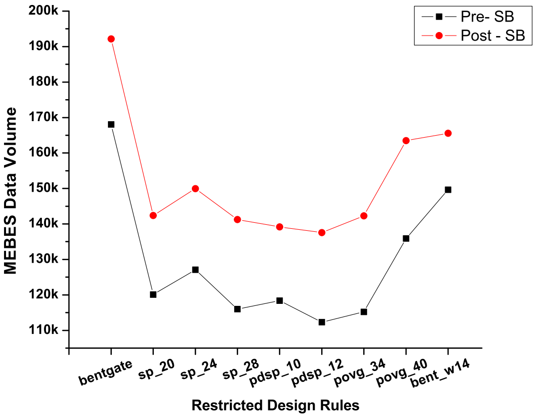

Figure 9: Impact of scattering bars on data volume for various RDRs for the c7552 circuit.

Table 4: Comparison of the single pitch library (SP) and the reduced default library (RDL)

RDR	3σ CD Uncertainty			Normalized Performance			
	Defocus (μm)						
	0.1	0.2	0.3	Delay	Area	Power	MEBES
RDL	1.0	1.0	1.0	1.0	1.0	1.0	1.0
SP	0.91	0.79	0.75	1.05	1.10	1.01	0.75

dense. Figure 9 shows the increase in data volume when SBs are inserted for our experimental setup. We observe a relatively consistent 15-20% increase in data volume when including SBs in the various RDR-based libraries. Insertion of scattering bars depends on the desired tradeoff between DOF margin and RET cost.

3.3 Approach of the Single Pitch RDR

Modern processes are usually tuned to favor one particular pitch (e.g., in off-axis illumination the angle of illumination to the mask is optimized so that one pitch can be printed perfectly due to the diffraction of light). Although within a limited range the illumination distortion caused by pitch differences may be compensated with other techniques such as SBs, designers still must keep the forbidden pitch range in mind for better yield. A "single pitch, single orientation" rule, where orientation implies horizontal or vertical gate routes, is a highly desirable solution from a lithography perspective but it requires significant constraints in library design and P&R. For simplicity, the AOI and OAI cell types are excluded in this section. A larger pitch number is expected than the default value so that a contact can be inserted between two poly lines. We obtain a pseudo single pitch library in which 97.6% of the gate pitches are fixed at a single value, while the remaining 2.4% are among three other other values. This is due to limitations in the cell layout synthesis tools. We compare the results with the reduced "sp_20" library, where AOI and OAI cell types are excluded, and all RDRs are set at default except that bentgate is "off". With a scattering-bar OPC recipe only tuned at defocus 0.1μm for the single pitch library, this RDR shows good potential to reduce the 3σ L$_{gate}$ uncertainty (may reach 24.60% as shown in Table 4). Moreover, the MEBES data volume can be 25% less with some penalty on performance (less than 6% in delay and power and about 10% in area).

3.4 Experiment on Circuit Performance

While the above discussion has been targeted at the manufacturability improvements provided by various RDRs, we must simultaneously consider the performance penalties incurred. In this section we report on the timing, area, and

Table 5: Summary of normalized performance and manufacturability results

Testcase	RDR	Delay	Area	Power	MEBES	Yield
c7552	bentgate	1	1	1	1	1
	sp_20	1.09	0.96	0.88	0.72	1.15
	sp_24	1.00	1.01	0.92	0.76	1.14
	sp_28	1.02	0.99	0.92	0.69	1.13
	pdsp_10	1.02	1.00	0.91	0.70	1.16
	pdsp_12	1.04	1.00	0.88	0.67	1.19
	povg_34	1.02	0.98	0.88	0.69	1.17
	povg_40	0.98	1.06	0.91	0.81	1.08
	bent_w14	1.05	0.95	0.94	0.89	0.99
c6288	bentgate	1	1	1	1	1
	sp_20	0.99	1.12	1.02	0.87	1.13
	sp_24	1.02	1.07	0.96	0.84	1.11
	sp_28	1.01	1.10	0.99	0.85	1.11
	pdsp_10	0.97	1.10	0.98	0.85	1.12
	pdsp_12	0.97	1.13	1.00	0.81	1.15
	povg_34	1.03	1.06	0.98	0.80	1.14
	povg_40	0.99	1.10	0.94	0.87	1.08
	bent_w14	0.96	1.05	1.03	0.99	1.00
c5315	bentgate	1	1	1	1	1
	sp_20	0.99	1.00	0.85	0.75	1.12
	sp_24	0.94	1.05	0.94	0.79	1.11
	sp_28	1.00	1.09	1.00	0.76	1.12
	pdsp_10	0.90	1.05	0.92	0.807	1.07
	pdsp_12	0.93	1.04	0.91	0.70	1.17
	povg_34	0.90	1.15	1.03	0.85	1.16
	povg_40	0.93	1.20	1.06	0.94	1.07
	bent_w14	0.94	1.04	1.04	1.00	1.00

power implications of the aforementioned RDRs for the three studied benchmarks.

Table 5 summarizes the circuit performance, mask data volume, and parametric yield given a 10% CD variation tolerance budget for all RDRs considered in this work. Looking at all three benchmarks we first point out that the range of delay values is quite small over all RDRs (5-10% worst-case spread) while the area and power impact is somewhat larger (up to 20% spread in both). The minimum poly_diffusion spacing rule as 0.12 μm ("pdsp_12") appears to be the most favorable rule for low MEBES data volume and high yield with acceptable performance. In particular it is useful to compare the "sp_20" and "pdsp_12" design rules which differ only in the poly_diffusion spacing rule. The latter shows improvements in both data volume and yield with negligible performance penalties (including better delay in all three circuits). The two line end extension rules (shown as "povg_∗") exhibit very similar characteristics and show excellent robustness to process defocus as mentioned earlier. The use of bent gates with minimum size may typically save area but at the expense of greatly increased data volume and substantial yield loss. As a result, it is now commonplace to see bent gates prohibited in modern design rule sets to improve manufacturability. All of the above indicates that there are good performance arguments to introduce RDRs in modern processes to reduce cost of ownership, without hurting yield and circuit performance.

4. CONCLUSIONS AND FUTURE WORK

Lithography bottlenecks in advanced CMOS processes call for the growing use of resolution enhancement technologies, which in turn benefit from less flexible, more restrictive design rule sets. In this paper we investigate the performance and manufacturability impact of a number of possible restricted design rules (RDRs). We build a framework to evaluate RDRs based on edge-placement errors or CD tolerances, mask data volume, as well as placed and routed circuit speed, area, and power characteristics. We point to various rules such as the use of increased field poly to diffusion spacings or increased poly line end extensions that may be good candidates to create more robust and cost-effective circuits without sacrificing performance. We demonstrate data volume reductions on the order of 20-30% relative to a baseline design rule set (reductions are ∼10% when referenced to a design rule set excluding bent gates) and reductions of nearly 50% in worst-case EPE when using even basic RDRs. These advantages come with very small performance penalties, namely 0-5% in area and a few percent in delay at most. We investigate the promising RDR for the "single pitch, single orientation" library which provides less gate CD uncertainty, 25% reduction in mask data volume, at the cost of less than 5% increase in delay and power and 10% in area. We put forth a word of caution here in that the optimal restricted design-rule set will depend heavily on the various process parameters such as illumination type, nature of resist, etc. However, our results suggest that compelling RDR sets can be formulated to support subwavelength lithography by providing substantial cost reductions with negligible performance tradeoff.

Table 6: Impact of corner correction on normalized yield at 10% EPE tolerance and mask cost for c7552 (the numbers are normalized to the corresponding library with baseline OPC for c7552)

RDR	Slightly Conservative		Very Conservative	
	Yield	MEBES	Yield	MEBES
sp_20	1.00	0.98	0.81	0.91
sp_24	1.00	0.97	0.80	0.90
sp_28	1.00	0.99	0.78	0.94
pdsp_10	1.00	0.98	0.81	0.86
pdsp_12	1.00	0.98	0.82	0.95
povg_34	1.00	0.98	0.91	0.93
povg_40	1.00	0.98	0.91	0.97
bentgate	1.00	0.99	0.84	0.97
bent_w14	0.99	1.00	0.84	0.92

Such a methodology can also be followed for metal layers to provide a good set of restricted design rules that have been qualified by extensive performance and manufacturability studies. For the polysilicon layer a large percentage of the feature count, and hence the mask data volume, arises from corner correction features (e.g., serifs, hammerheads). Extensive corner correction can be avoided [12] without impacting performance or yield. Although preliminary results in Table 6 indicate a relatively large impact on yield by corner corrections, we are evaluating whether the undesirable impact of relaxed corner corrections can be avoided through additional and simple design rules.

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