

# Research Directions for Coevolution of Rules and Routers

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## ABSTRACT

Design rules in advanced IC manufacturing processes are increasingly problematic for modern router architectures and algorithms. This paper first reviews types and causes of “difficult” design rules, as well as implications for current routing approaches. Next, some basic router components are assessed with respect to future viability. Last, the paper discusses prospects for future “coevolution” of design rules and detailed routing methods.

**Categories and Subject Descriptors:** B.7.2 [Integrated Circuits]: Design Aids – Layout, Place and Route

**General Terms:** Algorithms, Design

## 1. INTRODUCTION

Complexity of design rules for advanced CMOS processes ultimately hit home in two ways. First, with respect to *algorithms and tools*, the impact is felt in detailed routing, physical verification, reticle enhancement (RET), and mask data preparation (MDP). Second, with respect to *costs*, the impact is felt in loss of design tool quality and design productivity, as well as increased project uncertainty and manufacturing NRE. This paper explores the respective trajectories of rules and router technology and, notwithstanding many industry-structural and cultural barriers, describes necessary aspects of “coevolution”. Section 2 reviews examples of design rules that increasingly affect algorithmic and implementation complexity, runtime, completion rate, and result quality for modern routers. This is followed by some reasons for these rules’ existence, and implications for future routers. Section 3 comments on the viability of various techniques within future routers. Finally, Section 4 concludes with thoughts on rule-router coevolution.

## 2. RULES

### 2.1 Problematic Rules

The following list is by no means exhaustive. Entirely new sets of criteria arise when the mask production (write, inspect) flow is taken into consideration, or as the X-architecture ([56, 26]; see also [11, 52]) is deployed. E.g., X routing entails different landing pad shapes (isothetic rectangle vs. octagon vs. circle), different spacings (at least 10% pitch difference) between diagonal and axis-parallel wires, etc.

“Antennas” are formed by metal traces that accumulate static charge during manufacturing. Without a safe discharge path (through the reverse-biased diode at the output stage of a logic gate) any connected

gate may be damaged due to electrostatic discharge. “Antenna rules” establish maximum allowable ratios of metal area to gate area in the absence of discharge path. The complexity of such rules is increasing: *cumulative* (all layers) rules are supplemented by *per-layer* rules and recent *capacitance-based* rules (whereby parallel neighbors contribute to the antenna area calculation). The pure router-based solution is *bridging* (layer-hopping) to limit the amount of metal connected to a gate; this creates more wiring, vias and congestion. The combined router- and library-based solution is to drop reverse-biased diodes (source-drain contacts) close to the gate, i.e., (ECO substitution of) dioded cell variants, with negative area and power implications. Tightening of antenna ratios has lowered completion rates of detailed routers and led to more antenna waivers.<sup>1</sup>

*Via stacking and minimum area rules* arise because stacking of vias through multiple layers can cause minimum area violations with respect to stacking-dependent alignment tolerances. The resulting via cells (i.e., for intermediate layers in stacked vias) have more metal area than the minimum via overlap. In addition, use of multiple-cut via cells to increase BEOL yield is complicated by dependencies on the layers and wire segment widths to be connected.<sup>2</sup> In conjunction with wide-wire spacing rules, this increases difficulty of pin access. Via and line-end extension rules have been common since the 250nm node, and reflect “zeroth-order proximity correction” to compensate for line-end shortening in optical lithography.

*Width- and length-dependent spacing* (“halation”) rules make minimum spacing a function of both wire width and length of parallel adjacencies. This means that edge costs during heuristic search are dependent on path history (e.g., spacing depends on the distance traveled by the previous part of the connection). Ripple effects are common: changing one wire’s dimensions can lead to a wave of spacing and other dimensional changes, notch-filling, etc. Especially pernicious are *influence rules* (stub rules, halo rules), where a wide wire will influence the spacing rule within its surroundings.<sup>3</sup> A wide wire typically has thin “tributaries”, and influence rules will dictate larger spacing around every wire within some distance of the thin tributaries (near the wide wire). This results in strange jogs and spreading when wires enter an influenced area, as well as complicated ECO effects (e.g., insertion of a tributary).

*Density control rules* arise due to chemical-mechanical planariza-

<sup>1</sup>Antenna ratios differ with oxide thickness and, as gate oxides become extremely thin, slow their decrease (below a certain oxide thickness, leakiness helps prevent antenna damage). Reasonable values today might be thick-oxide antenna ratio of 400 for I/Os, and thin-oxide antenna ratio of 2000 for gates. On the other hand, the ITRS [27] calls for new high-k gate dielectric materials by 2005-2006. Should liberal use of dioded cells be required, there will be high costs with respect to chip area and power metrics as well as non-trivial balancing of two sources of yield loss: increased die area vs. antenna damage.

<sup>2</sup>Multiple via cut patterns have different spacing rules depending on the pattern, e.g., a 2x2 pattern can have different rules than a 2x3 pattern. In general, cut-to-cut spacing once again influences via-to-via spacing.

<sup>3</sup>For example, any wire that is X nm away from a wide wire must also be at least Y nm away from any other geometry.

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ISPD’03, April 6–9, 2003, Monterey, California, USA.

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tion (CMP) and other manufacturing steps (cf. terms such as microloading, halation) which have varying effects on device and interconnect features depending on local layout density characteristics. Foundry rules require that a layout be uniform with respect to prescribed density criteria; this is achieved through insertion of *fill* geometries (*slotting*, the complement of filling, may also be required in wide wires). Traditionally, fill is added by physical verification tools and eventually merged with functional layout geometries during mask data preparation. Unfortunately, both foundry rules and design tools are in a mutual “local minimum” with respect to density control: high-quality rules are not imposed because tools cannot handle them, and tools do not evolve because there is no pressure from new rules.<sup>4</sup> Because area fill impacts coupling capacitance and hence all performance criteria, grounded fill has been used where parasitic uncertainty must be minimized; this resembles power/ground routing and has been achieved by in-house routers since at least 1997 [37]. Density control is now more constraining on all layers, e.g., we now see via density and array density rules that create multilayer constraints and induce solutions akin to the “filling and cheating” used on active and poly (complementary fill patterns to avoid creating spurious devices).

## 2.2 Causes of Layout Rule Complexity

Design rule complexity stems mainly from the need to compensate (1) subwavelength optical lithography interference effects, and (2) systematic microloading effects in resist development and etch. Minimum feature sizes since the 350nm node have been smaller than the wavelength of light used in the stepper, leading to two lithography-driven forms of reticle enhancement: *optical proximity correction* (OPC) and *phase-shifting masks* (PSM).

OPC perturbs mask aperture shapes to systematically compensate for nonlinear feature distortions arising from optical diffraction and resist process effects [46, 10]. Common types of OPC include (1) serifs, hammerheads and tomahawks to reduce corner rounding and line-end shortening; (2) notches to control linewidth in the face of iso-dense effects; and (3) subresolution assist features (SRAFs, or scattering bars [10]) for narrow gate geometries. OPC is responsible for much of the above-cited design rule complexity (e.g., to leave space for serifs and SRAFs, extend line ends, etc.); it also explodes data volumes and mask write-inspect times, reducing mask yield and increasing NRE.

PSM enables the clear regions of a mask to transmit light with prescribed phase shift. Light diffracted into the nominally dark region between two clear apertures of phase 0 and 180 degrees will interfere destructively; the improved image contrast leads to better resolution and depth of focus [43, 47]. With the more widely used *bright-field* alternating phase-shifting approach, a feature with width smaller than some constant  $B$  cannot be printed unless it is defined by two phase shifters having opposite phase. The *phase assignment problem* seeks to assign phases to all shifters needed to define the critical features in a given layout, such that each feature is surrounded by opposite-phase shifters and any overlapping shifters have the same phase. The phase assignment is feasible if and only if a particular graph derived from the shifter layout is bipartite – a highly non-local criterion for manufacturability.<sup>5</sup>

<sup>4</sup>A glaring example is the case of CMP. Note that the heritage of PV tools is one of (1) local checking, (2) focus on Boolean operations performed on polygon data, and (3) lack of empowerment to change the layout. Thus, today’s foundry metal density rules impose only upper and lower bounds on areal coverage in square windows of prescribed size in the layout. However, because post-CMP ILD thickness is roughly monotone in feature density, rules should actually enforce bounds on *variation* in feature content between (circular) windows (of varying sizes) – not to mention distinctions based on shape dimensions to account for tradeoffs between the failure modalities of metal dishing and oxide erosion. Such “correct” criteria are not easily checked or optimized by PV tools, though optimal LP-based methods have been known since [34]. Fill methods, moreover, check only a “fixed-dissection” subset of all windows [12, 33].

<sup>5</sup>PSM is not “transparent” to custom and semi-custom layout since there are no “local rules” that can guarantee phase-assignability of layouts without huge area penalties. PSM methodologies have been proposed since at least 1998 to distribute responsibility for phase-

*Deposition of copper.* Since copper metallization is formed by an inlaid (damascene) process, it is significantly more susceptible to open faults than short faults (estimates are by 3x [23]; cf. [31]). This is the reason for via-doubling rules and other practices that mitigate high-resistance or open faults.

*Microloading and global density effects.* As noted above, OPC systematically compensates for nonlinearities in both exposure and resist process steps. Microloading-induced variation of resist development and etch dynamics occurs at length scales of microns, while CMP variability is a consequence of density variation on length scales of millimeters.

## 2.3 Takeaways

From the above, brief takeaways are as follows. (1) Gridded approaches (even “reduce to greatest common denominator” and “gridding at the coarse routing level”) appear doomed.<sup>6</sup> (2) History independent edge costing fails, and stymies traditional Dijkstra, A\* or other best-first search frameworks. (3) Non-local effects are starting to predominate (influence rules, global density checks, alternating PSM bicolorability, etc.). (4) Exceptions are the rule. For example, there are more non-default net classes with respect to timing, reliability, signal integrity, etc. – such that annotation and constraint semantics are nearly as complex as for board routing. (5) Fewer issues are treatable by postprocessing (e.g., track switching for signal integrity or bridging for antennas). The number of first-class objectives is steadily growing.<sup>7</sup>

## 3. ROUTERS

This section assesses several router component technologies, assuming that design rule trends of the previous section continue.<sup>8</sup>

### 3.1 Optimization Approaches

Consider a strawman “standard” framework of (1) fixed-die, grid graph based global area routing followed by gridded detailed routing, (2) construction of multi-pin Steiner trees through sequences of source-target A\* search-based connections, (3) LVS clean (DRC unclean) routing with ripup and reroute to eliminate blockage and DRC violations. Scalability of this metaheuristic framework is hampered by (1) weak ability to construct “whole” interconnect topologies, e.g., to maximize source required arrival time or control critical area, and (2) sensitivity to arbitrary ordering decisions with respect to connections, ripup-reroute, etc. Constraint-dominated routing must increasingly refrain from arbitrary local decisions. Thus, connection-at-a-time will be increasingly replaced by net-at-a-time; set-of-nets-at-a-time, region-at-a-time (= switchbox routing), etc. (cf. [25]). When edge costs depend on previous path history and the foundations of A\* search disappear, more enumerative (iterative-deepening A\* [40], depth-first-search, etc.) or combinatorial approaches may be neces-

assignability, e.g., (1) “good layout practices” (no T shapes or doglegs on critical levels, no uneven-length fingers of transistors, etc. [45]); (2) graph bipartization and compaction algorithms for automatic phase conflict resolution [55, 20, 36, 3]; and (3) mechanisms for achieving composable standard-cell phase layouts [35]. Today, shifter sizes have prevented phase-shifted layout pitches from shrinking as fast as the ITRS prescribes, *but this has not yet impacted batch routing that takes place on M2 and above*. Transparent insertion of phase-shifting may be helped by the two-mask method of [51].

<sup>6</sup>[5] provides the following justification of this claim. The issue is that one must find a “GCD” that at least includes: (i) all widths of all types of wires, (ii) with and without the various (up and down) via sizes, (iii) the various OPC features that are contemplated, (iv) for each customer process. If this GCD is too small, the gridless approach is better from a capacity and memory perspective. (And, with gridless routers we would have better libraries, since designers would not be forced to put pins on grid.)

<sup>7</sup>Of course, the router is also responsible for more than strict manufacturability: reliability (electromigration, joule heating), signal integrity and timing, low-resource power and clock distribution, global signaling bandwidth, etc. are all concerns. It is safe to say that the day of “constraint-dominated routing” [4] has arrived.

<sup>8</sup>Of course, as Section 4 proposes, design rules should not necessarily continue these trends!

sary, tempered in complexity by consideration of limited sets of patterns for connections, topologies, pin escapes, etc. The pattern-based methods of [44, 8] are a relevant example.

Two recent advances in multicommodity flow (MCF) methods are particularly appealing for “simultaneous” global routing. First, breakthrough improvements for finding approximate fractional multicommodity flows [21, 19] have improved runtime scalability compared to [7, 24].<sup>9</sup> Second, recent research has extended MCF to very powerful and general global routing formulations. A series of works by Dragan et al. [16] gives provable approximations to the problem of congestion and wirelength driven buffered global routing with a prescribed *buffer block* plan, taking into account signal parity, delay upper/lower bounds, and other practical considerations.<sup>10</sup> [2] further extends the method to perform *timing-driven* global buffered routing according to a prescribed *buffer site* map: a provably good MCF algorithm simultaneously performs global routing, buffer/wire sizing and layer/pin assignment with the objective of minimizing routing area subject to given constraints on source/buffer wireloads, wire and buffer congestion, and individual sink delays.

### 3.2 Representations

For many years, *gridless* (shape-based) representation of resources and wires has been the “wave of the future” for full-chip, cell-based detailed routing. Gridded routers have survived such presumed show-stoppers as wide wires and crosstalk constraints, while gridless routers’ flexibility in costing and shaping has never outweighed their lack of speed and capacity. But in the regime of severe manufacturability rules, gridless routers – armed with scalability tricks from the gridded world – may finally prove superior.<sup>11</sup>

Topological routing will likely see a renaissance. Compared to geometric routers, which determine the exact geometric paths of the wires, topological routers use a more abstract representation of interconnect, and determine only the topology of the wires but not their exact paths. The topological representation defers detailed geometric decisions, and is thus much better suited for as-late-as-possible elimination of various design rule violations.<sup>12</sup>

### 3.3 Legacy Perspectives

Today’s routers retain several outdated perspectives on the routing problem, e.g., (1) clock and power are “special nets”, (2) interconnects are routed as tree topologies, and (3) “wires” are graph edges rather than multi-edges. These legacy perspectives can be overly restrictive, and likely harmful. Several example shifts in perspective are as follows. (1) Distinctions between “signal” and “special” must disappear as *all* metal geometries – clock, power, scan, signal, shield, and fill – share available resources to achieve chip design goals. (2) Following the mesh-based distribution of clock and power for improved reliability and process variation tolerance, large non-critical signal nets may improve critical-area or electromigration profiles through non-tree routing [31, 49]. (3) Fill is likely to become more “active” than “dumb”: grounded fill can serve as shielding to manage signal in-

<sup>9</sup>Albrecht [1] reports excellent runtime for a congestion and wirelength driven global router based on [21, 19] that is able to route very large chips (over half-million nets).

<sup>10</sup>The method extends to a general class of multiterminal multicommodity flows in graphs with capacities on vertices and subsets of vertices in [18]. The latter extension enables performing buffered routing simultaneously with floorplan compaction and buffer sizing from a discrete buffer library.

<sup>11</sup>Melding of hierarchical graph-based layout resource abstractions from global/coarse routing [50, 54] with shape-based detailed routing [60, 15], as described in [4], has become common practice in commercial tools. Additional methods transferable from gridded full-chip routing include “midway” track ordering [28], distributed solution followed by stitching of small switchboxes, etc.

<sup>12</sup>The most popular topological encoding is the Rubber Band Sketch (RBS) model, proposed by Rivest and fully formalized by Maley [41, 48]. It is the basis of, e.g., the SURF system [53]. RBS has proven its flexibility for manipulation of layout objects during routing [48, 14, 57] and compaction [48, 9], as well as channel routing, via minimization [13], and post-layout optimization [59].

tegrity and delay uncertainty, and fill can also control iso-dense or other microloading effects (perhaps even parity for phase-shifting). (4) Wire splitting and similar geometric transformations that create “multi-edges” already save density today by achieving equivalent current delivery capability while avoiding wide wire spacing rules; such transformations can also create *active shielding* [38] in clock or other high-performance signaling, and can potentially help manage inductance effects when compared against monolithic wide wiring.

### 3.4 Takeaways

Brief takeaways are as follows. (1) Once again: gridded routing must eventually be supplanted by gridless. (2) More global optimizations (e.g., MCF) will be used, entailing more deferred decisions (e.g., topological framework) and better solvers, will be used; these will be stitched together, and simplified by templates and patterns, as necessary for runtime and scalability. (3) Metal will be “multi-purposed”, and more flexibly shaped to not only deal with manufacturing requirements, but also to improve distributions of catastrophic and parametric (performance) yield. A fill rectangle can be both a shield and an assist feature. A non-tree edge can enhance reliability as well as performance. Splitting (a limiting case of slotting) can improve both density and delay. Etc. (4) A side observation is that a large backlog of routing technology has not yet made it into commercial routers. The challenge of difficult layout rules may be a catalyst for the industry to eliminate some of this backlog.

## 4. COEVOLUTIONS AND CONCLUSIONS

Four years ago, I wrote [32]: “Thus, abstraction and understanding of manufacturing issues should be shifted up: (i) OPC- and PSM-related design rules will move up into global and detailed routing; (ii) PSM phase assignability checks and iterations with compaction will move into detailed routing; (iii) final PSM phase assignment will move up before traditional performance and physical verification; (iv) full-chip OPC insertion, full-chip aerial intensity mapping, “silicon-level” DRC/LVS/PA, and eventually function-centric DRC/LVS/PA will be added into the design flow; etc. At the same time, improved forward annotation of functional intent will ease the burden on verification tools for both layout geometry and mask geometry.” Unfortunately, today’s goals for “coevolution of rules and routers” appear similar to those of 1999. This begs the question: What have we been doing all this time? I will conclude with several scenarios for “coevolutions”.

Idealism says that EDA can still deliver an appropriate and timely unification of layout, RET, MDP and foundry flows, enabling maximum extraction of value from process innovations. This ideal EDA capability would provide a \$/wafer driven layout-to-manufacturing flow that minimizes total cost of achieving prescribed function and production volume. A key mindset change is that there are no more “design rules”, only statistical models of the manufacturing process that allow EDA tools to reconcile predicted distributions of printed dimensions against cost-performance goals [6, 22].

The realist in me views the context for rule-router coevolution as:

- There is only one “rule” (or, “law”) in the entire semiconductor industry: *Cost of integration must decrease such that new, high-value products are enabled which amortize whatever infrastructure is needed to achieve the cost reduction, and moreover allow additional wealth creation.*
- 157nm steppers are nowhere in sight for the 65nm node, and hence high-NA 193nm lithography will (supposedly) be used for 65nm starting in two years. In this light, “all things to all users” EDA tools and “as flexible as possible” layout ground rules - with neither process nor design technologists making any hard calls - appear to have coevolved themselves into a corner ([51] aside, very little will print using 193nm except uniform gratings).

I believe that we have basically two “reset” choices.<sup>13</sup> (1) One future is a more “head in sand” trajectory. Lithographers will avoid acknowl-

<sup>13</sup>Other choices - (3) stall the 65nm and 45nm nodes for cost reasons until 157nm lithography is delivered, and (4) change definitions (e.g., “pitch” becomes redefined as “contacted metal pitch” in order to help stay on the roadmap - are not realistic.

edging the impact of delayed 157nm lithography, and rely on emergence of either 157nm tools or cost-effective hard phase-shifting mask production and double-exposure lithography (e.g., using the method of [51]). With no letup in the aggressiveness of RETs or layout flexibility, EDA will then continue to fix on “rules” (and, for other reasons, paths of least resistance in technology development). The end result could be a “hard reset” when 65nm costs – mask NRE, wafer processing, design cost, and design quality – are all found to be prohibitive. (2) A second future might be termed a “meet in the middle” trajectory (cf. “shared red bricks” [29, 30]) whereby lithographers *unilaterally restrict critical-level layout freedoms* – most likely to subsets of regular gratings (cf. [39]) – in order to achieve cost-effective, reliable printing of critical features. Several technologies can achieve this “two-beam imaging”, e.g., [42, 58]. Though EDA will need to respond with tool modifications for pure right-way, restricted-pitch layout design, significant design-rule pressure will have been removed. Density losses associated with pure right-way, grating-based layout will likely leave sufficient cost advantages to justify the 65nm transition, and can be compensated by new EDA technology such as low-metal-layer count tools for extremely cost-sensitive designs. I view this second future as a win-win, “soft reset”. With either future, of course, there are sufficient challenges for routing technology.

## 5. ACKNOWLEDGMENTS

Many thanks are due to Andrew Caldwell for helpful discussions, to Ion Mandoiu and Qinke Wang for help in gathering background material, and to Raymond Nijssen for the invitation to prepare this paper as well as additional background material.

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