A NEW DESIGN COST MODEL FOR THE 2001 ITRS

Andrew B. Kahng
UCSD CSE and ECE Departments,
La Jolla, CA 92093-0114, USA

Gary Smith
Gartner Dataquest, Inc.
USA

1. INTRODUCTION

For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law ("the number of components per chip doubles every 18 months"). The most significant trend for society is the decreasing cost-per-function, which has led to significant improvements of productivity and quality of life through proliferation of computers, electronic communication, and consumer electronics.

Table A. Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last two decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. *The International Technology Roadmap for Semiconductors (ITRS)* has been an especially successful worldwide cooperation. It presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations, and governments. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs.

The 2001 edition of *ITRS* is the result of a worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. has ensured that the 2001 ITRS continues to be the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology. This paper presents details of an important new element of the 2001 *ITRS*, namely, the Design Cost Model that has been introduced in the Design Chapter.

2. DESIGN SCOPE

Design technology (DT) enables the *conception*, *implementation*, and *validation* of microelectronics-based systems. Elements of DT include *tools*, *libraries*, *manufacturing process characterizations*, and *methodologies*. DT is the link that transforms ideas and objectives of the electronic systems designer into manufacturable and testable representations. The role of DT is to enable profits and growth of the semiconductor industry via cost-effective production of designs that fully exploit manufacturing capability.

A core message in the 2001 *ITRS* Design Chapter is this: *Cost of design is the greatest threat to continuation of the semiconductor roadmap.* Cost determines whether differentiating value is best achieved in software or in hardware, on a programmable commodity platform or on a new IC. Manufacturing non-recurring (NRE) costs are just reaching one million dollars (mask set + probe card); design NRE costs routinely reach tens of millions of dollars, with design shortfalls being responsible for silicon re-spins that multiply manufacturing NRE. Rapid technology change shortens product life cycles and makes time-to-market a critical issue for semiconductor customers. Manufacturing cycle times are measured in weeks, with low uncertainty. Design and verification cycle times are measured in months or years, with high uncertainty.

It is understood that without foundry amortization, the semiconductor investment cycle is at risk. Indeed, "fill the fab" has been the rallying cry for DT. It is also understood from previous ITRS editions that there is a *design productivity gap*: the number of available transistors grows faster than the ability to design them meaningfully. Yet, investment in process technology has by far dominated

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investment in design technology. The good news is that enabling progress in DT continues to be made. Figure 1, which appears in the 2001 *ITRS*, shows that the estimated design cost of a prototypical "low-power SOC PDA" (cf. the definition presented in the 2001*ITRS* System Drivers Chapter [1]) is approximately $15M in 2001, versus $342M had DT innovations between 1993 and 2001 not occurred. (On the other hand, the bad news is that many long-standing design technology challenges (embedded software design, verification, new and reuse logic design productivity, etc.) have recently become crises.) The remainder of this paper describes the development of the new Design Cost Model.

3. THE DESIGN COST MODEL

A breakthrough in this year's Design Roadmap was the ability to develop a cost model. The environment today is similar to the environment surrounding thefab equipment market at the founding of SEMATECH in the 1980s. Today, Designs and Design Methodology are considered the crown jewels of a semiconductor or electronic equipment vendor. Process technology still holds an important spot in product differentiation, but it has been repeatedly proven that the major breakthroughs come through design. For purposes of roadmapping, this means that getting design input into the Design Technology Working Group has been difficult. Still, we believe that the systems and semiconductor houses are coming to see that setting accurate expectations – for both the EDA and the designer communities – is now possibly more important than the guidance the Roadmap has givenFab Equipment and the Semiconductor vendors for over a decade.

The Cost Model was developed by first identifying the direct costs involved with an ASIC design. These included the salary and overhead costs of an engineer, EDA tool cost per seat, and interoperability costs. Interoperability costs were impossible to determine directly. As we were able to determine engineering and tool costs, and had good data on design overruns, we were able to derive the interoperability costs. However, until future efforts take a closer look at interoperability costs (instead of just complaining about these costs in an "ungrounded" manner), we will be unable to directly quantify what appear to be almost a third of our total design costs.

While improved studies on interoperability issues will enhance future versions of the model, our confidence in the overall model is quite high. As with any model, the assumptions and the data that fill out those assumptions determine the accuracy. The first data points were as follows.

- Engineering salary for an experienced ASIC designer.
- Cost overhead, including workstations, for that engineer.
- Cost of design tools for one engineering seat.

We based our engineering salary and overhead cost on U.S. data. This model can be used in determining the estimated costs of any design, but engineering costs would require modification for specific geographic locations and for the degree of difficulty of the design. Note that the original

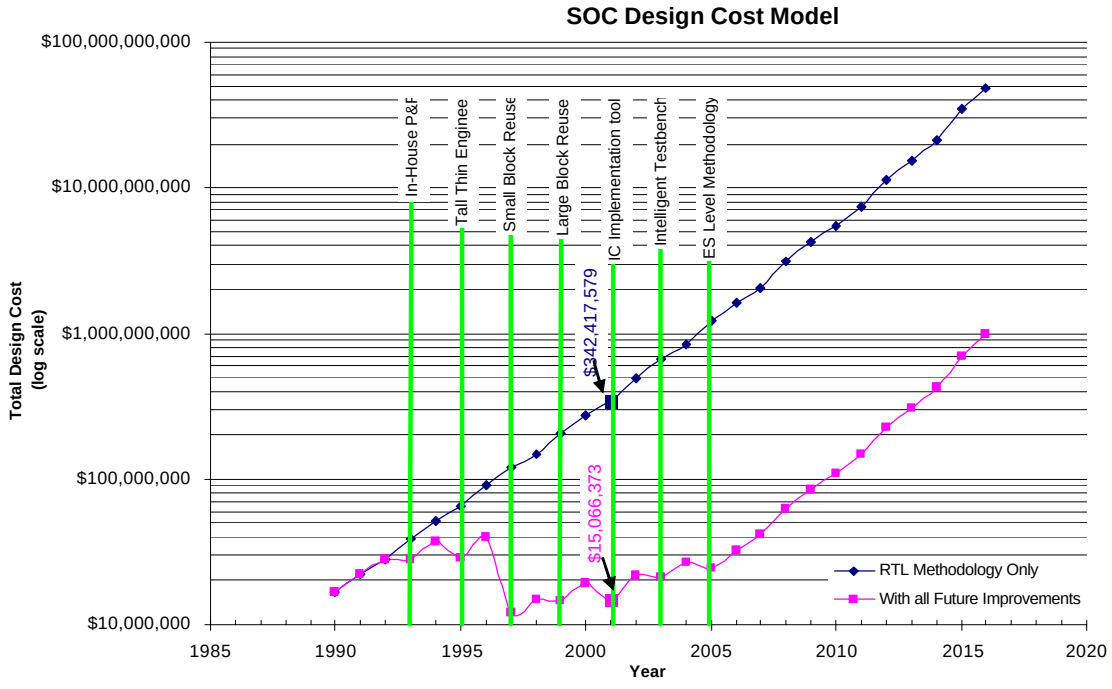

Figure 1. Impact of Design Technology on system implementation cost

intent of the new model was to determine the cost of the *largest possible ASIC* within a given process generation. This means that engineering costs were at the high end of the spectrum; possibly, a different estimate would be appropriate in the next roadmap.

Tool cost was an input from a Gartner Dataquest study that is performed every two years. The per seat tool costs are not on the high end of tool cost, as was the engineering cost data, but an average of tool costs per seat in the Dataquest-defined Power User category. Of course, the model can be perturbed depending on any individual design project's or design organization's data.

Next, we considered design productivity for:

- Number of engineers needed to design a million gates of logic at each of the .8 micron, .5 micron, 350nm, 250nm and 180nm process nodes.

Designer input was used to estimate future design productivity:

- Number of engineers needed to design a million gates of logic at each of the 130nm, 90nm and 70nm process nodes.

The .8 and .5 micron data came for past experience as a methodologist. The reluctance from the User Community to share data was a problem. The .35 micron data came from a Dataquest study, and actually ranged from 110,000 gates to 250,000 gates. The committee picked a "centerline" point, 180,000 gates. The 250nm and 180nm productivity data came from a small sample of North American and European users; we were unable to integrate Japanese semiconductor industry input into the model. Finally, future process node projections came from users. Considerable discussion was generated, especially concerning the impact of the Intelligent Test Bench. A significant minority believed our estimates of increased productivity to be significantly lower than indicated by current RTL Functional Verification costs.

We then determined the design challenge, that is the largest possible design for a particular semiconductor node.

- Size of the largest possible design in gates (four transistors per gate) by silicon node.
- The percent utilization of the silicon by memory.
- The largest possible logic design by silicon node.

The largest possible design is a Dataquest number derived from previous ITRS data, and checked through designers' input. The difficult part was the memory content. Dataquest's studies show that memory took up 15% of the silicon in 1990, which grew to 29% in the year 2000. There is a significant semiconductor contingent that believes that most of the design area will become memory or that the designs will become all memory and microprocessors. The theory seems to be that software will solve all our design problems. This does not take into account the power-hungry characteristics of software, nor does it consider the possibility that true hardware/software co-design could easily lower the software content of future designs. There is also the lack of automation in today's software development environment. That being said, we have remained with Dataquest's projections, which show that 35% of the silicon area will be taken up by memory in the year 2005. Logic design area is a consequence of this assumption.

4. THE ANSWERS TO PRODUCTIVITY

Figure 1 shows that we have had four significant improvements in productivity since the introduction of the RTL Methodology. These are:

- In-House Place & Route;
- The Tall Thin Engineer;
- Small Block Reuse (2,500 to 24,999 gates); and
- Large Block Reuse (25,000 to 100,000 gates).

In-House Place & Route was a fairly straight forward methodology change. The increase of iterations needed to close timing for .5 micron designs made the use of the ASIC vendor's Place & Route services suboptimal. If it took the ASIC house a week for each iteration, one could easily eat up the entire design time just in the final layout phase of the design. Bringing Place & Route in-house cut the turn-around time down to hours or at most days.

The Tall Thin Engineer was an interesting discovery. Some design teams were dividing their design teams horizontally, that is, there would be a simulation expert, then a synthesis expert, etc. It was discovered that if you have an engineer that followed or actually performed all of the design skills, then productivity increased significantly. Basically, the horizontal approach optimized the tool function but lost track of the actual design goals.

Small Block Reuse and then Large Block Reuse were methodology changes that had the highest impact on design productivity. There is Very Large Block Reuse that will come about somewhere before 2010, but first we need to get the ESL (Electronic System Level) Methodology and tools in place.

The industry is presently putting in place the new IC Implementation Tool Set. Early users have seen significant improvement in productivity. This and two other tool/methodology changes will continue to lower our design costs:

- IC Implementation Tool Set;
- Intelligent Test Bench; and

- ES Level Methodology.

The IC Implementation Tool Set is the automation of the RTL Design Flow. Today it is defined as Synthesis to GDS II tape out. It will probably come to include the Silicon Virtual Prototype and the rest of the RTL design tools.

The Intelligent Test Bench is the automation of the RTL Functional Verification flow. We have had to include the physical verification into the IC Implementation Tool Set because of the necessity of timely concurrent analysis during the design process.

The ES Level, or Electronic System Level tends to be called just the System Level by many in the world of electronics. The Electronic System Level includes Hardware and Software design. The true System Level also include MEMs, Mechanical and possibly some day BioChemical design. This would represent a shift in methodology equal in impact to the introduction of the RTL methodology in the late 1980s. Once we have the RTL flow automated, Design will move up to the ES Level and RTL will be come an implementation flow as the Gate Level Design Methodology did with the adoption of the RTL Methodology.

We may summarize the quantifications used in the productivity analysis, as follows. First, we measured designer productivity at 4K gates (= 16K transistors) per year in 1990 – the year in which the so-called "RTL methodology" originated – and then calibrated the design productivity improvements for seven major DT innovations that occurred or are anticipated since then. The specific improvements are: in-house place-and-route (1993; +38.9% productivity improvement to 5.55K gates per designer-year); "tall-thin engineer" (1995, +63.6% improvement to 9.09K gates), small-block (2,500 – 74,999 gates) reuse (1997, +340% improvement to 40K gates), large-block reuse (75,000 – 1M gates) (1999, +38.9% improvement to 56K gates), IC implementation suite (2001, +63.6% improvement to 91K gates); "intelligent testbench" (2003, +37.5% improvement to 125K gates); and "electronic system-level (ES-level) methodology" (2005, +60% improvement to 200K gates).

Even though the cost and productivity analyses were originally used to assess the cost of designing the largest possible ASIC in a given technology, the 2001 *ITRS* (Figure 1) quantified the impact of the DT innovations on design cost for the low-power System-on-Chip (SOC-LP) PDA driver defined in the System Drivers chapter. The model further sets the historical rate of increase in engineer cost at 5% per year (salary and overheads starting at $181,568 in 1990), and the rate of increase in EDA tool cost at 3.9% per year (starting at $99,301 per engineer in 1990). The number of designers per million logic gates is 250 in the year 1990 and 11 in 2001. The low-power SOC PDA model has 3M logic gates in 2001, implying an SOC PDA design cost (designers + tools) of $15.1M. Without the five major DT innovations that occurred between 1993 and 2001, the design cost for the same SOC in 2001 would be approximately $342.4M. Among the conclusions drawn in the Design Chapter of the 2001 *ITRS*: without a continued DT innovation pipeline, design cost would quickly become prohibitive or designs will be forced to have less valuable content.

5. The Design Roadmap

The Power Users have been frustrated at the rate of advance by the EDA tool providers. A Dataquest study, done on behalf of the 2001 *ITRS* Design Technology Working Group, found that there were just under 6,000 R&D engineers employed in the EDA Industry. Still, most of these answers have been known for quite a while. LSI Logic was doing design reuse years before it caught the attention of the design community in general. The Intelligent Test Bench was first defined (to the authors' knowledge) in the spring of 1996, but we have yet to see a full implementation of the tool. The first ES Level designs were done in 1994, but we have yet to solve the technical challenges needed for general adoption. Hopefully the 2001 Roadmap will provide the direction needed to contain the rising design cost problem.

6. Acknowledgements

Some of the preceding material – particularly in the introductory sections – is quoted at length from the 2001 *ITRS*. The authors thank the *ITRS* community for making its roadmap available for such use. Discussions with Design Technology Working Group members are gratefully acknowledged.

References

[1] International Technology Roadmap for Semiconductors 2001 (`http://public.itrs.net`)