Interconnect Implications of Growth-Based Structural Models for VLSI Circuits [*†]

Chung-Kuan Cheng[1], Andrew B. Kahng[1,2] and Bao Liu[1]
[1] UCSD Computer Science and Engineering Dept., La Jolla, CA 92093-0114
[2] UCSD Electrical and Computer Engineering Dept., La Jolla, CA 92093-0406
kuan@cs.ucsd.edu, abk@ucsd.edu, bliu@cs.ucsd.edu

Abstract

Power-law scaling phenomena that govern VLSI circuits have for several decades formed the foundation of VLSI interconnect estimation. This research investigates possible alternative power-law phenomena in VLSI circuits. In particular, we develop new *random growth* models and assess their implications for VLSI interconnect structure. We assess our models' predictions for *fanout*, *crossing edge*, and *terminal* scaling using test data from 21 industry standard-cell designs with up to 283K cells. Our work demonstrates the possibility of non-Rent based, yet equally plausible and well-fitting, structural models for VLSI circuits and their interconnections.

1 Introduction

Scaling phenomena that govern VLSI circuits have for several decades formed the foundation of interconnect estimation. In particular, "Rent's rule" observes a power-law relationship between terminal number and gate number of a "well-placed" circuit [9], or intrinsic to the circuit topology [7]. Donath [6] and Davis et al. [5] have respectively proposed highly referenced Rent's rule based interconnect estimation models. Stroobandt and Kurdahi [11] observe an empirical power-law with exponent -3 and derived fanout distribution expressions that are close to power-law for two- and three-terminal nets. Zarkesh-Ha et al. [12] derive from Rent's rule a power-law for *fanout distribution* with exponent $p-3$, and report good agreement with experimental data.

In this work, we address the possibility of alternative power-law phenomena in VLSI circuits, governing not only terminal number and fanout distribution, but also the number of *crossing edges*. We also investigate the formal derivation of interconnect-related power laws from *growth models* for circuit structure. We make the following contributions:

- We note a potential glitch in the derivation of [12], and the existence of families of circuit topologies with identical fanout distribution but widely varying (intrinsic) Rent exponents. Such open aspects of the relationship between Rent exponent and fanout distribution motivate our investigations.
- We note the existence of a literature on random growth models for graphs, e.g., [1], [8]. These models are motivated by observed scaling phenomena in a wide range of contexts (World Wide Web, paper citation, social connections, power distributions grids, and even human brain structure), and share structural characteristics, notably a power-law fanout distribution (with different exponent values). The previous random growth models can infer power-law fanout distributions from simple random growth rules, but only a fixed exponent -3 is derived in [1], and no explicit relationship is derived in [8]. We give several new random growth model variants in the VLSI context, along with their implications for interconnect structure. Specifically, we provide a new *preferential attachment* variant model, and a new kind of *temporal attachment* model.
- We validate our models using test data from 21 industry standard-cell designs with between 4K and 283K cells. We find that (i) our new preferential attachment model provides the best fanout distribution prediction; (ii) the model of Barabasi et al. [1] provides the best scaling model for crossing edges; and (iii) a temporal attachment variant provides the best fits for terminal scaling.

Our work demonstrates the possibility of non-Rent based, yet equally plausible and *well-fitting*, structural models for VLSI circuits and their interconnections. Given that our new power-law models have been "empirically validated" with similar procedures as in previous empirical studies of Rent's rule, our work also suggests that power-law fanout distribution or other interconnect structural characteristics may not necessarily follow from, nor imply, that the circuit is "Rentian". Hence, emphasis on Rent's rule based structure may be inappropriate.

Our paper is organized as follows. We give necessary definitions and interpretation of growth models as random graphs and hypergraphs in Section 2. Previous Rent-based and random growth models are reviewed in Section 3. Section 4 proposes a new preferential attachment variant, and Section 5 gives a temporal attachment model along with several variants. Section 6 presents experimental tests of the various models using industry circuits, and we conclude in Section 7.

2 Definitions

We make the following definitions.

- The *degree* d_i of a *vertex* i is the number of edges incident to vertex i.

[*]Supported by a grant from Cadence Design Systems, Inc. and by the MARCO Gigascale Silicon Research Center. Address communications to: Prof. Andrew B. Kahng, UCSD CSE Department, Mailcode 0114, La Jolla, CA 92093-0114.

[†]Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.
SLIP'01, March 31-April 1, 2001, Sonoma, California, USA.
Copyright 2001 ACM 1-58113-315-4/01/0003 ...$5.00.

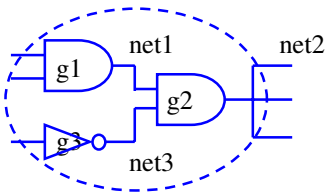

Figure 1: Example VLSI circuit partition with three gates.

- The *degree* d_{net} of a *hyperedge net* is the number of vertices incident with *net*.
- The *fanout* $f(net)$ of a hyperedge *net* is the degree of *net* minus one, i.e., $d_{net} - 1$.
- $N(f)$ is the number of hyperedges with fanout f.
- A *boundary vertex* of a *partition* is a vertex incident to at least one edge that crosses the boundary of the partition.
- E is the number of *crossing edges* of a partition. Crossing edges are edges between two vertices in different partitions, or in the VLSI context, a pair of components in different partitions that are on the same net.
- G is the number of vertices of a partition.
- T is the number of boundary vertices of a partition. (Note that $T \leq E$.)

Figure 1 shows an example VLSI circuit partition. The partition has three gates $g1$, $g2$ and $g3$, implying $G = 3$. There are three primary inputs (two inputs of $g1$ and one input of $g3$), one primary output $net2$, and two internal nets $net1$ and $net2$. Since each of the three gates $g1$, $g2$ and $g3$ is incident to a primary input or a primary output, we have $T = 3$. Gate $g2$ connects to $net1$, $net2$ and $net3$, implying $d_{g2} = 3$. Gate $g2$ drives three sinks, implying $d_{net2} = 4$ and $f(net2) = 3$. Each of the internal nets $net1$ and $net3$ has fanout 1, which implies $N(1) = 2, N(f : f \neq 1) = 0$ for this particular partition. Finally, if we assume that all three primary inputs have fanout 1, and know that $net2$ connecting to three gates, we have $E = 6$.

In general, we may also use *graphs* to model VLSI circuits, where each component or gate is represented as a vertex, each multi-pin net is decomposed into two-pin nets, and each two-pin net is represented as an edge. Essentially, this represents each (directed) hyperedge as a star of (directed) graph edges. Of particular interest for this work is the use of (random) *growth models* for graphs, where vertices and edges are added into a growing graph, and are thus implicitly sequenced in time. Below, we will develop random graph growth models, but interpret the resulting "time-sequenced" graphs as hypergraphs according to the following convention.

- Each vertex v has exactly one output hyperedge. Hence, we use $f(v)$ to denote the fanout of vertex v or the fanout of the output hyperedge of vertex v.
- All edges incident to a vertex v from "downstream" neighbors (i.e., vertices that were generated *later* in the growth process) form the output hyperedge of vertex v. The number of these "downstream" edges is the fanout $f(v)$.
- Any edge incident to v from an "upstream" neighbors v' (i.e., a vertex that was generated *earlier* in the growth process) is a fanin of v. The degree of vertex v minus the number of these "upstream" edges equals $f(v)$.

In hypergraphs corresponding to time-sequenced graphs, we will be concerned only with partitions corresponding to some prefix of the vertex sequence $v_1, v_2, \ldots, v_N$, i.e., partitions of form $\{v_1, v_2, \ldots, v_G\}$ with $G \leq N$. The terminal number of a circuit partition then corresponds to the number of hyperedges crossing the boundary of the partition, i.e., it corresponds to T (the number of boundary vertices of the partition).

Figure 2 illustrates a time-sequenced graph and its interpretation as a hypergraph. In the Figure, vertex 2 has degree 7 because there are 4 backward edges and 3 forward edges. Hyperedge 2 (output hyperedge of vertex 2) has degree 4, hence fanout $f(2) = 3$. Vertex 2 is a boundary vertex for a partitioning along the dotted line in the figure because it connects to other vertices to the right side of the partition. At least 4 crossing edges pass over the dotted line, implying $E \geq 4$. The number of vertices of the left side partition is $G = n + n_0$ (where the random growth process started with n_0 initial, or *primary*, vertices). Since vertices 1 and 2 are boundary vertices, the number of boundary vertices of the partition is $T \geq 2$.

3 Previous Models

3.1 Rent-Based Models

Zarkesh-Ha Model. Zarkesh-Ha et al. [12] propose that $Net(i)$, the number of i-terminal (i.e., i-pin) nets, is given by

$$Net(i) \approx k(1-p)i^{p-3} \quad (1)$$

Their result is obtained as follows. Rent's rule gives the number of external terminals for a circuit of N gates as

$$T_{external} = kN^p$$

and the total number of terminals for all N gates as

$$T_{total} = Nk1^p = kN$$

where k (average pins per cell) and the Rent exponent p are two empirical constants. The number of internal terminals is therefore

$$T_{internal} = kN - kN^p$$

and the average number of terminals incident with each gate is

$$\sum_{i=2}^{N} T_{net}(i) = \frac{T_{internal}}{N} = k(1 - N^{p-1})$$

where $T_{Net}(i)$ is the number of terminals in nets with fanout i. Similarly in a circuit of $N-1$ gates,

$$\sum_{i=2}^{N-1} T_{net}(i) = \frac{T_{internal}}{N-1} = k(1 - (N-1)^{p-1}).$$

Subtracting these two equations leads to the number of terminals in "N-terminal nets" (here, N is the size of any given circuit partition):

$$T_{net}(N) = k((N-1)^{p-1} - N^{p-1})$$

from which

$$\begin{aligned} Net(i) &= \frac{T_{Net}(i)}{i} \\ &= \frac{k}{i}((i-1)^{p-1} - i^{p-1}) \\ &\approx k(1-p)i^{p-3} \end{aligned}$$

Stroobandt-Kurdahi Model. Another fanout distribution model is proposed by Stroobandt and Kurdahi [11]. The authors analyze the hierarchy structure of a netlist and represent

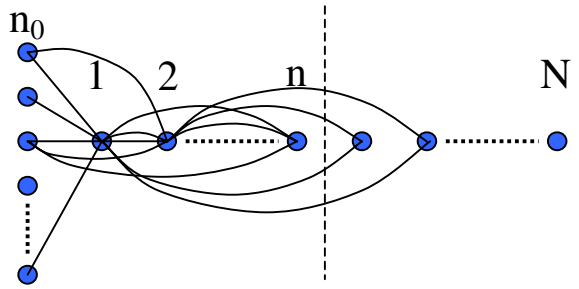

Figure 2: A time-sequenced graph with a partition after vertex n. The leftmost n_0 vertices are *primary* vertices that existed at timestep 0 of the growth process; the other vertices $1,2,...n,...N$ are each added at corresponding timesteps during the growth process. The dotted line defines a partition that consists of all vertices added up through timestep n.

the fanout distribution by a generating polynomial of net degrees. The resulting recursive equations can be transformed into the logistic equation. Although there is no closed form solution for the logistic equation in general, closed form expressions for 2- and 3-terminal nets are presented. These expressions are close to a power-law, especially for large circuits; this agrees with an empirical power-law with exponent -3 observed by the authors.[1]

Observations. We make the following observations. First (as independently noted in [10], p. 104), we note that the Zarkesh-Ha model depends on $T_{net}(i)$ being the same in both the N-gate circuit and the $(N-1)$-gate circuit, for all $i < N$. However, such an assumption may not be valid. [10] also notes that only the *internal* nets and the terminals in the *internal* nets for a boundary of N gates are counted,[2] while the *external* nets and their terminals are omitted in the Zarkesh-Ha model. Second, we observe the existence of a family of circuit graph topologies with Rent exponent $p = 0$ (chain, i.e., 1-D mesh), $p = 0.5$ (2-D mesh), $p = 0.666$ (3-D mesh), etc. – all with identical fanout distribution (a spike at fanout $f = 2$), yet with Rent p varying from 0 to 1. Certainly, the first two cases have many "real" examples in arithmetic circuits. Third, the "embedded" Rent parameter depends on the layout method, while the "intrinsic" Rent parameter as well as the fanout distribution are intrinsic to the circuit structure.[3] However, the derivation of the relationship between Rent parameter and fanout distribution in [12] does not appear to be restricted to only intrinsic Rent parameter.[4] These observations suggest that the relationship between fanout distribution and Rent parameter may still be an open issue.

3.2 Random Growth Models

3.2.1 Basic Model of Barabasi et al.

Barabasi et al. [1] give a random graph growth model with two rules:

- Random Growth: as new vertices are generated, they connect randomly to previous vertices; and
- Preferential Attachment: new edges are more likely to be adjacent to large fanouts (thus, larger fanouts are more likely to grow even larger).

Barabasi et al. originally proposed this model in the context of the World-Wide Web. We observe that these two rules are also plausible for VLSI circuits: when designing a circuit, one creates new components and connects them to existing components, with higher probability to connect to larger fanouts (power supply, clock, reset, global buses or control signals, etc.) than smaller fanouts. Recall from the discussion of Figure 2 that we can interpret random growth as a time sequence that defines a hypergraph topology. In the Barabasi model, a new vertex is added at each timestep. Each new vertex v has m new edges that connect to previous vertices, and the probability of any previous vertex j being connected to v is proportional to its degree $d_j(t = v)$ at that timestep (before the m new edges are added). We thus have

$$\frac{\partial d_i(t)}{\partial t} = m\frac{d_i(t)}{\sum_{j=0}^{t-1} d_j(t)}. \tag{2}$$

For completeness, at time $t = 0$ there are $n_0 \geq m$ *primary* vertices (e.g., corresponding to the primary inputs in a VLSI design) to which all randomly-added vertices may connect. After t timesteps, the model leads to a random graph with $n_0 + t$ vertices and mt edges. From

$$\sum_{j=0}^{t} d_j(t) = 2mt$$

we have[5]

$$d_i(t) = \begin{cases} m(\frac{t}{i})^{0.5} & i \neq 0, \\ \frac{m}{n_0}t^{0.5} & i = 0. \end{cases} \tag{3}$$

The probability for vertex i's degree d_i to be less than d is

$$P(d_i(t) < d) = P(t_i > \frac{m^2 t}{d^2}) = 1 - \frac{m^2 t}{d^2(t+n_0)}$$

and the probability density is

$$P(d) = \frac{\partial P(d_i(t) < d)}{\partial d} = \frac{2m^2 t}{n_0 + t}\frac{1}{d^3}.$$

Observing that there are $t + n_0$ hyperedges (there are $t + n_0$ vertices, each with exactly one output hyperedge), and that the difference between vertex degree and vertex fanout is a constant m as the number of input edges,

$$f(i) = d_i - m$$

and the fanout distribution is given by

$$N(f) = (N + n_0)P(f) = \frac{2m^2 N}{(f+m)^3} \tag{4}$$

i.e., a power-law with exponent -3.

The parameters E and T depend on partitioning. As described in Section 2, we partition the random time-sequenced

[1] The model takes two parameters as inputs: (i) the Rent exponent p characterizing the netlist topology, and (ii) an internal/external terminal number ratio f characterizing the partitioning (larger f means more internal terminals at each hierarchy level).

[2] In [12], slightly different notation is used: there the boundary has m gates.

[3] The intrinsic vs. embedded distinction, along with example circuit families (trees, meshes, etc.) was given by Hagen et al. [7]; subsequent work of Christie [4] provides a similar distinction ("topological" vs. "geometric").

[4] Moreover, experimental data presented in Section 6 fail to confirm the $p - 3$ power law: different circuits with the same power-law exponent for fanout distribution can have significantly different Rent parameter values, and vice-versa. We recognize that data presented in [12] support the $p - 3$ relationship, and are still looking into possible reasons (provenance of test cases, Rent parameter fitting methodology, etc.) for this discrepancy.

[5] There is actually a glitch in the Barabasi et al. [1] derivation: $\sum_{j=0}^{t-1} d_j(t)$ (before the t^{th} timestep) is mixed with $\sum_{j=0}^{t} d_j(t)$ (after the t^{th} timestep). Since the impact is small, for consistency of the exposition we will follow Barabasi's (approximate) derivation.

graph by setting all vertices added before timestep n in one partition (left) and all other vertices in the other partition (right) (recall Figure 2). The whole circuit has N gates and the left partition has $G = n_0 + n$ gates. For ease of exposition, in all the following analysis we will assume that n_0 is small, thus permitting the approximation $G = n + n_0 \approx n$. (Generally, removing the approximation entails replacing G's by $n + n_0$, and replacing n's by $G - n_0$.)

The number of crossing edges of a partition at vertex n is

$$\begin{aligned} E(G) &= E(0) + \sum_{i=1}^{n} d_i(N) - 2mn \\ &= mN^{0.5} + 2mN^{0.5}(G^{0.5} - 1) - 2mG \end{aligned} \quad (5)$$

where $E(0)$ is the number of edges connecting to the n_0 primary vertices, and the discrete summation is approximated by a continuous integration.

A boundary vertex i of partition at vertex n has, by definition, at least one edge connecting to some vertex $j > n$. This means that

$$d_i(N) - d_i(n) \geq 1,$$

and from Equation 3

$$\begin{aligned} d_i(t) = m(\frac{t}{i})^{0.5} \text{ when } i \neq 0 \\ m(\frac{N}{i})^{0.5} - m(\frac{n}{i})^{0.5} > 1 \\ m(\frac{N^{0.5} - n^{0.5}}{i^{0.5}}) > 1 \end{aligned}$$

from which we can upper-bound i:

$$\begin{aligned} i^{0.5} < m(N^{0.5} - n^{0.5}) \\ i < m^2(N^{0.5} - n^{0.5})^2. \end{aligned}$$

Hence, the number of boundary vertices is given by

$$T(G) = Min\{m^2(N - 2(NG)^{0.5} + G), G\}. \quad (6)$$

Barabasi et al. further analyze two variants to show that *both* elements of their model – preferential attachment, and random growth – are necessary to yield the fanout distribution power law. We now briefly sketch this analysis.

3.2.2 Variant A: Uniform Attachment

The uniform-attachment variant has two rules:

- Growth: new vertices are randomly generated; and
- Uniform Attachment: all previous vertices have equal probability to be connected to a new vertex:

$$\begin{aligned} \frac{\partial d_i(t)}{\partial t} &= \frac{m}{n_0 + t - 1} \\ d_i(t) &= m\log(\frac{n_0 + t - 1}{n_0 + i - 1}) + m \\ P(d) &\approx \frac{e}{m} e^{-\frac{d}{m}} \\ N(f) &= (t + n_0)P(d) \\ &\approx \frac{e}{m}(t + n_0)e^{-\frac{f}{m} - 1}. \end{aligned} \quad (7)$$

This leads to

$$\begin{aligned} E(G) &= E(0) + \sum_{i=1}^{n} d_i - 2mn \\ &= (G + n_0)m\log\frac{n_0 + N - 1}{n_0 + G - 1} + mn_0\log\frac{n_0}{n_0 - 1} \\ &\quad + m\log(n_0 + n - 1) + m(n_0 - 1). \end{aligned} \quad (8)$$

Analysis of boundary vertices yields that $T(G) = G$ when

$$G < \frac{n_0 + N - 1}{e^{\frac{1}{m}}} - n_0 + 1,$$

otherwise

$$\begin{aligned} T(G) &= G(d_i(N) - d_i(n)) \\ &= Gm(\log(n_0 + N - 1) - \log(n_0 + G - 1)). \end{aligned} \quad (9)$$

3.2.3 Variant B: No Growth

Under the no-growth variant model, the size of the random graph is fixed, and we randomly connect between vertices:

$$\begin{aligned} \frac{\partial d_i}{\partial t} &= \frac{N}{N - 1}\frac{d_i}{2t} + \frac{1}{N} \\ d_i(t) &\approx \frac{2}{N}t. \end{aligned} \quad (10)$$

4 A New Preferential Attachment Model (*Pref* Model)

Barabasi's model gives a power law for fanout distribution under a random growth model. However, it fails to give a correct exponent: only the power law with exponent -3 is available. We now show that a power-law fanout distribution with varying exponent values can be achieved by switching to a different *preferential attachment* (*Pref*) rule:

$$\frac{\partial d_i(t)}{\partial t} = m\frac{d_i - qm}{\sum_{j=0}^{t-1}(d_j - qm)} = \frac{d_i - qm}{(2 - q)t} \quad (11)$$

where $q \leq 1$. Using analysis similar to that of the previous section,

$$d_i(t) = \begin{cases} qm + m(1 - q)(\frac{t}{i})^{\frac{1}{2-q}} & i \neq 0, \\ qm + m(\frac{1}{n_0} - q)t^{\frac{1}{2-q}} & i = 0. \end{cases} \quad (12)$$

and

$$\begin{aligned} P(d) &= \frac{\partial P(d_i(t) < d)}{\partial d} \\ &= \frac{t}{t + n_0} m^{2-q}(1 - q)^{2-q}(q - 2)(d - qm)^{q-3} \\ N(f) &= (N + n_0) \cdot P(d) \\ &= m^{2-q}(1 - q)^{2-q} N(q - 2)(f - qm + m)^{q-3}. \end{aligned} \quad (13)$$

The exponent of $q - 3$ appears to be a coincidence with [12]. We now consider implications of the new preferential attachment model for scaling of E and T.

- The number of crossing edges induced by separating all vertices added before timestep n is given by

$$\begin{aligned} E(G) &= E(0) + \sum_{i=1}^{n} d_i(N) - 2mn \\ &\approx mN^{\frac{1}{2-q}} + mqn_0(1 - N^{\frac{1}{2-q}}) + (q - 2)mG \\ &\quad + m(1 - q)N^{\frac{1}{2-q}} G^{\frac{1}{q-2}} \end{aligned} \quad (14)$$

with $G \gg 1$. This implies a hybrid of power-law and linear relationship between the number of crossing edges and the size of a given vertex subset – equivalently, between terminal number and gate number of a circuit partition.

- Any boundary vertex i of the partition at vertex n has, by definition, at least one edge connecting to some vertex $j > n$. This implies

$$d_i(N) - d_i(n) \geq 1$$
$$i < (m(1-q)(N^{\frac{1}{2-q}} - n^{\frac{1}{2-q}}))^{2-q}$$

or, equivalently,

$$T(G) = Min\{(m(1-q)(N^{\frac{1}{2-q}} - G^{\frac{1}{2-q}}))^{2-q}, G\}. \quad (15)$$

5 New Random Growth Models Via Temporal Attachment Rules

We have also investigated several alternative random growth models for VLSI circuit hypergraphs, including models that attempt to capture replication and copying, and hierarchical reuse. Here, we describe several variants of a new *temporal attachment* model, and their interconnect scaling implications. Recall from Section 2 our convention for inducing hypergraph structure from random graph growth, via the time sequence in which vertices are added. With this convention, "temporal locality" in the growth model affects the hypergraph structure. In our temporal attachment model, each vertex has probability

$$\Pi(d_i) = \frac{i^s}{\sum_{j=1}^{t} j^s}. \quad (16)$$

of receiving any one of the m edges added at timestep t. Different values of s induce different behaviors. Three specific examples: $s = 0$ gives random equiprobable attachment to all previous vertices; $s = 1$ gives attachment that prefers temporal locality; and $s = \infty$ gives an extreme temporally preferential attachment whereby a vertex connects only to its temporally immediate neighbors.

5.1 Temporal Attachment Model 1: $s = 1$

For $s = 1$,

$$\frac{\partial d_i(t)}{\partial t} = m\frac{i}{\sum_{j=0}^{t-1} j} = m\frac{i}{t(1+t)/2} = \frac{2mi}{t(1+t)}, \quad (17)$$

$$d_i(t) = \begin{cases} 2mi(\log\frac{t}{t+1} - \log\frac{i}{i+1}) + m & i \neq 0, \\ \frac{m}{n_0} & i = 0. \end{cases} \quad (18)$$

A partition at vertex n in a graph containing a total of N vertices will have the following number of crossing edges:

$$\begin{aligned} E(G) &= E(0) + \sum_{i=1}^{n} d_i(N)di - 2mn \\ &\approx mG(G+1)\log\frac{N}{N+1} + mG + m. \end{aligned} \quad (19)$$

For boundary vertex i, we have

$$d_i(N) - d_i(n) \geq 1$$
$$i > \frac{1}{2m(\log\frac{N}{N+1} - \log\frac{n}{n+1})}$$

from which

$$T(G) = Min\{\frac{1}{2m(\log\frac{N}{N+1} - \log\frac{G}{G+1})}, G\}. \quad (20)$$

5.2 Temporal Attachment Model 2: $s = 0$

For $s = 0$,

$$\begin{aligned} \frac{\partial d_i}{\partial t} &= \frac{m}{t} \\ d_i(t) &= \begin{cases} m\log(\frac{t}{i}) + m & i \neq 0, \\ m\log t + \frac{m}{n_0} & i = 0. \end{cases} \end{aligned} \quad (21)$$

We also have

$$\begin{aligned} P(d_i(t) < d) &= P(i > \frac{t}{e^{\frac{d}{m}} - 1}) = 1 - \frac{t}{t+n_0}e^{1-\frac{d}{m}} \\ P(d) &= \frac{\partial P(d_i(t) < d)}{\partial d} = \frac{mt}{t+n_0}e^{1-\frac{d}{m}} \\ N(f) &= mNe^{-\frac{f}{m}}. \end{aligned} \quad (22)$$

A partition at vertex n in a graph containing a total of N vertices will have the following number of crossing edges:

$$\begin{aligned} E(G) &= E(0) + \sum_{i=1}^{n} d_i(N)di - 2mn \\ &= mG(\log N - \log G) + n_0 m\log N. \end{aligned} \quad (23)$$

Analysis of boundary vertices i connecting to vertices $j > n$ yields that

$$T(G) = G \text{ when } n < \frac{N}{e^{\frac{1}{m}}} \quad (24)$$

else

$$\begin{aligned} T(G) &= G(d_i(N) - d_i(n)) \\ &= mG(\log N - \log G). \end{aligned} \quad (25)$$

5.3 Temporal Attachment Model 3: $s = \infty$

For $s = \infty$, the graph is a chain (actually, a multigraph with edge multiplicity m between adjacent (consecutive) vertices). This means that $E = m$, $T = 1$, and all output hyperedges have fanout m.

6 Experimental Observations

Table 1 summarizes the models developed in Sections 3-5. In this section, we report experimental observations concerning the three structural parameters T (= terminal number), E (= crossing edges) and $N(f)$ (= net fanout) of given partitions (having gate count G) of the circuit. Relevant aspects of our experimental studies are as follows.

- We use 21 industry standard-cell test cases with between 4K and 283K cells. 18 netlists originate in Cadence Design Systems, Inc. LEF/DEF format, and are processed with public-domain tools obtainable on the Web from the MARCO GSRC Bookshelf in the UCLA PDTools release (see, e.g., links from [3]); 3 netlists originate in Bookshelf format.
- Net fanout $N(f)$ is obtained by scanning the netlist file.
- Terminal number T and crossing edge number E are obtained using UCLA's Capo placer [3], which is based on top-down recursive bipartitioning. Capo's output is taken after filtering out the top three levels of the partitioning hierarchy, which have large deviations (Region II in the

Model	Assumption	Resultant Relationship
Zarkesh-Ha	$T = cG^p$	$N(f) \approx cf^{p-3}$
Barabasi	$\frac{\partial d_i}{\partial t} = m\frac{d_i}{\sum_j d_j}$	$N(f) = c(f+m)^{-3}$
		$E = c_1 - c_2 G^{\frac{1}{2}} - c_3 G$
		$T = Min\{c_1(c_2 - G^{0.5})^2, G\}$
Preferential	$\frac{\partial d_i}{\partial t} = m\frac{d_i - q}{\sum_j (d_j - q)}$	$N(f) = c_1(f+c_2)^{q-3}$
($Pref$)		$E = c_1 G + c_2 G^{\frac{1}{q-2}}$
		$T = Min\{c_1(c_2 - G^{\frac{1}{2-q}})^{2-q}, G\}$
Temporal 1	$\frac{\partial d_i}{\partial t} = m\frac{i}{\sum_j j}$	$E = c_1 G^2 + c_2 G + c_3$
($s = 1$)		$T = Min\{\frac{1}{c_1(c_2 - \log\frac{G}{G+1})}, G\}$
Temporal 2	$\frac{\partial d_i}{\partial t} = \frac{m}{t}$	$N(f) = ce^{-f}$
($s = 0$)		$E = c_1 G + c_2 G \log G + c_3$
		$T = Min\{c_1 G - c_2 G \log G, G\}$
Temporal 3	$\frac{\partial d_i}{\partial t} = m\frac{i^p}{\sum_j j^p}$	$N(m) = t, N(f \neq m) = 0$
($s \to \infty$)		$E = m$
		$T = 1$

Table 1: Model summary.

terminology of [9]). For a given test case, we geometrically average over all blocks that have the same number of cells to obtain an averaged terminal number and an averaged crossing edge number. In this, we basically follow the protocol established in [2].

- For each parameter, linear regression (in the appropriate log-log representation) is applied to the experimental data. We may further remove points in Rent's rule Region II if they contain large deviations [9, 7], until the standard deviation in the linear regression procedure is less than a small value (we use the value 0.1 in our experiments).
- We extract power-law exponents from the linear regression on the log-log plot.[6]
- We apply non-linear regression (a Levenberg-Marquardt variant) to find the *minimum standard deviation* fit of each model to experimental data.

Figure 3 gives a qualitative view of how different the various models' predictions are for fanout distribution. Each dot in the Figure represents a data point for a given fanout value and a single test case, case13. The dots are normalized, e.g., if 0.01 fraction (i.e., 1%) of the nets in a test case have $f = 6$, then there will be a single dot for $f = 6$ and $N(f) = 10^{-2}$. The best-fits of fanout distribution predictions from the Zarkesh-Ha, Barabasi, Preferential and Temporal 2 models are plotted. Coefficients of the best-fits can be found in the Tables given elsewhere in this section.

- Table 2 contrasts fitted $N(f)$ power law exponents (fourth column) with the Zarkesh-Ha model's fanout distribution prediction (exponent $p-3$, fifth column). All of the fitted $N(f)$ exponents have essentially zero standard deviation. The fitted exponents do not generally resemble the Zarkesh-Ha model's $p-3$ exponents, for which the best-fit standard deviations are fairly large (sixth column). We observe that while the Zarkesh-Ha model does not fit the data closely, the power-law *form* of the model (which is shared by the *Pref* model, without the $p-3$ constraint) can fit the data very well.

[6] As discussed below, data from our studies can be used to support the notion that all three parameters T, E and $N(f)$ have power-law scaling. Previous works [9, 12] have suggested that T and $N(f)$ follow power-law scaling, and our data also also show that E follows a power law.

- Table 3 contrasts fitted E exponents with each other model's E predictions. Again, all of the fitted E exponents have essentially zero standard deviation. The data suggest that the Barabasi model gives the best fitted prediction for crossing edges.
- Finally, Table 4 contrasts fitted Rent parameter exponents p with each other model's T predictions. Again, all of the fitted p exponents have essentially zero standard deviation. The data suggest that the Temporal 2 model gives the best fitted prediction for terminals.

From these data we see that each model has its own strength and weaknesses. (1) Zarkesh-Ha's model cannot provide E prediction and it takes p (Rent exponent) as an required parameter. Thus, the *Pref* model provides the most reasonable fanout distribution prediction. (2) The Barabasi model gives the best E prediction. (3) The Temporal 2 model gives the best T prediction. At this point, we feel that our investigation is only scratching the surface of non-Rent based (and, specifically, growth model based) scaling models for VLSI interconnects.

Test Case	Total #cells	Total #Nets	fitted N(f) exponent	ZH N(f) exponent	ZH N(f) std. dev.
case1	4670	4670	-2.109	-2.299	1.9e3
case2	6923	7637	-1.688	-2.392	2.6e4
case3	7703	5657	-1.305	-2.266	3.0e7
case4	7445	7721	-2.253	-2.360	6.7e4
case5	8609	9074	-1.304	-2.357	4.1e4
case6	9011	11962	-1.802	-2.490	2.3e6
case7	9797	8734	-1.278	-2.532	8.8e2
case8	12133	11828	-1.314	-2.418	2.9e4
case9	12261	13245	-2.258	-2.399	3.1e4
case10	12857	10880	-1.217	-2.388	4.9e4
case11	20577	25634	-1.982	-2.451	2.5e5
case12	25995	28603	-2.154	-2.488	3.1e5
case13	27412	31022	-1.395	-2.468	6.0e4
case14	33917	39152	-1.270	-2.346	2.3e5
case15	35549	44121	-1.982	-2.579	3.5e5
case16	85572	87390	-2.053	-2.448	2.8e6
case17	117617	124688	-2.122	-2.644	8.0e7
case18	182137	181188	-4.099	-2.405	3.2e8
case19	183102	180684	-3.983	-2.351	2.8e8
case20	210323	200565	-3.303	-2.405	2.4e8
case21	282979	284735	-1.201	-2.495	6.4e8

Table 2: Fanout distribution scaling exponent (with essentially zero standard deviation), and best-fit (with respect to standard deviation) of Zarkesh-Ha model prediction.

7 Conclusions

For many decades, parameters and scaling descriptions of VLSI interconnects have been connected with "Rent's rule". In this work, we show that random growth models are also a potentially viable source of scaling phenomena for VLSI. Such models may be appealing, given their demonstrated applicability in a wide variety of contexts.

We have given several new random growth model variants in the VLSI context, along with their implications for interconnect structure. We observe that each model has its own strengths and weaknesses in predicting the various parameters that we studied (fanout, terminal and crossing number), and that no model predicts all parameters simultaneously. We leave open the possibility of other, equally plausible and well-fitting structural models for VLSI circuits and their interconnections. We further note

Test Case	fitted E exponent	Barabasi's E std. dev.	*Pref.* E std. dev.	Temp.1 E std. dev.	Temp.2 E std. dev.
case1	0.669	2.2e4	2.4e4	2.7e4	2.2e4
case2	0.454	2.3e4	3.9e4	2.8e4	2.3e4
case3	0.875	3.0e4	6.0e4	3.3e4	2.2e4
case4	0.504	2.2e4	2.3e4	3.0e4	2.3e4
case5	0.613	1.8e5	3.0e5	3.0e5	2.0e5
case6	0.419	3.3e4	2.0e5	9.3e4	4.0e4
case7	0.184	3.5e5	6.6e5	5.4e5	3.7e5
case8	0.341	4.8e5	4.8e6	4.4e6	1.1e6
case9	0.288	2.2e5	2.2e5	5.0e5	2.4e5
case10	0.339	3.0e5	2.9e6	2.7e6	6.3e5
case11	0.503	9.8e4	2.3e5	1.3e5	1.0e5
case12	0.413	8.2e4	2.1e5	1.1e5	9.4e4
case13	0.541	2.0e6	4.5e6	3.6e6	2.0e6
case14	0.418	3.2e6	1.8e7	1.9e7	5.9e6
case15	0.342	3.2e5	1.0e6	7.4e5	4.2e6
case16	0.480	5.4e5	1.4e6	8.3e5	6.4e5
case17	0.734	1.5e6	5.4e6	3.1e6	1.4e6
case18	0.519	1.3e6	4.9e6	1.5e6	1.4e6
case19	0.552	1.1e6	5.3e6	1.6e6	1.4e6
case20	0.518	2.2e6	7.3e6	2.4e6	2.3e6
case21	0.293	1.5e8	1.5e9	1.3e7	4.0e7

Table 3: Comparision of each model's best-fit (with respect to standard deviation) E prediction.

Test Case	Rent p	Barabasi's T std. dev.	Temp.1 T std. dev.	Temp.2 T std. dev.
case1	0.701	6.0e2	8.2e3	5.4e2
case2	0.608	1.2e3	1.2e4	1.2e3
case3	0.734	7.8e2	5.8e3	2.8e2
case4	0.640	1.2e3	9.1e3	7.9e2
case5	0.643	2.7e3	2.3e4	2.6e3
case6	0.510	1.4e3	9.8e3	1.1e3
case7	0.468	1.9e3	6.0e3	1.7e3
case8	0.582	5.3e2	6.3e3	4.3e2
case9	0.601	1.9e3	2.4e4	1.4e3
case10	0.612	5.4e2	5.9e3	3.9e2
case11	0.549	2.5e3	1.1e4	2.3e3
case12	0.512	2.3e3	1.6e4	2.4e3
case13	0.532	1.8e3	1.0e4	1.5e3
case14	0.654	1.3e6	8.0e4	1.2e4
case15	0.421	7.4e3	3.4e4	8.2e3
case16	0.552	5.2e3	5.1e4	5.9e3
case17	0.356	6.5e3	1.8e4	3.8e3
case18	0.595	4.5e4	2.5e5	3.3e4
case19	0.649	6.0e4	4.8e5	4.8e4
case20	0.574	8.0e4	2.7e5	6.7e4
case21	0.506	3.0e4	9.8e4	2.0e4

Table 4: Comparision of each model's best-fit (with respect to standard deviation) T prediction.

that a power-law fanout distribution or other interconnect structural scaling might not imply, nor be implied by, any "Rentian" nature of VLSI circuits.

Our ongoing research addresses such open questions as:

- Construction of 2-dimensional random growth models, where random growth depends not only on time but also on other characteristics of the growing circuit.
- Random growth models that capture growth by replication and/or copying: VLSI designs tend to grow by copying parts of previous designs. There is a tenuous analogy to web designers copying links of previous webpages, which has been shown to lead to a power law fanout distribution in webpage connections [8].
- How Rent p of a block affects the Rent p of a larger system that reuses that block (i.e., since the block's Region II terminal-vs.-gate relationship becomes part of Region I in the larger system).

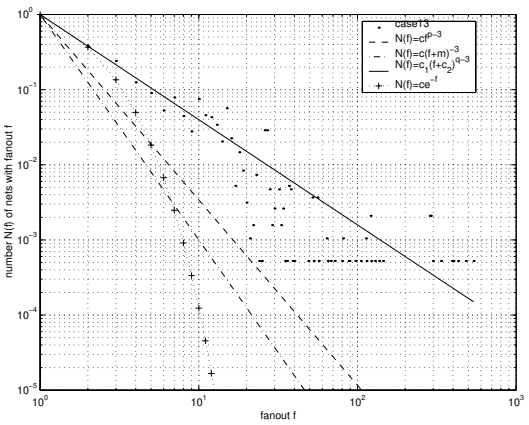

Figure 3: Fanout distribution, and qualitative match to different scaling models. Each dot represents the normalized number $N(f)$ of nets with fanout f. Four predictions are best-fit (with respect to standard deviation) to these data, according to the Zarkesh-Ha, Barabasi, Preferential and Temporal 2 models.

8 Acknowledgments

We thank Igor Markov and Stefanus Mantik for modifications to, and help with use of, the UCLA Capo placer.

References

[1] A. Barabasi, R. Albert and H. Jeong, "Mean-field theory for scale-free random networks", *Physica*, vol. A 272, 1999, pp. 173-187, `http://www.nd.edu/~networks/Papers/physica.pdf`.

[2] A. E. Caldwell, A. B. Kahng and I. L. Markov, "Relaxed Partitioning Balance Constraints in Top-Down Placement", *Proc. IEEE ASIC Conference*, 1998, pp. 229-232.

[3] `http://nexus6.cs.ucla.edu/GSRC/bookshelf/Slots/Placement/Capo/` See also: A. E. Caldwell, A. B. Kahng and I. L. Markov, "Can Recursive Bisection Produce Routable Placements?", *Proc. ACM/IEEE Design Automation Conf.*, 2000, pp. 477-482.

[4] P. Christie, "Tutorial: Managing Interconnect Resources", *Proc. Intl. Workshop on System-Level Interconnect Prediction*, 2000, pp. 1-51.

[5] J. A. Davis, V. K. De and J. D. Meindl, "A Stochastic Wire- Length Distribution for Gigascale Integration(GSI)-part 1: Derivation and Validation", *IEEE Trans. on Electron Dev.*, 45, 1998, pp. 580-589.

[6] W. E. Donath, "Placement and Average Interconnection Lengths of Computer Logic", *IEEE Trans. on Circuits and Systems* CAS-26(4) (1979), pp. 272-277.

[7] L. Hagen, A. B. Kahng, F. Kurdahi and C. Ramachandran, "On the Intrinsic Rent Parameter and New Spectra-Based Methods for Wireability Estimation", *IEEE Trans. on CAD* 13(1) (1994), pp. 27-37.

[8] J. M. Kleinberg, R. Kumar, P. Raghavan, S. Rajagopalan and A. Tomkins, "The Web as a graph: measurements, models, and methods", *Proc. International Conference on Combinatorics and Computing*, 1999, pp. 26-28.

[9] B. S. Landman and R. L. Russo, "On a Pin versus Block Relationship for Partitions of Logic Graphs", *IEEE Trans. on Computers* C-20 (1971), pp. 1469-1479.

[10] D. Stroobandt, *A Priori Wire Length Estimates for Digital Design*, Kluwer Academic Publishers, 2000, pp. 140.

[11] D. Stroobandt and F. J. Kurdahi, "On the Characterization of Multi-point Nets in Electronic Designs", *Proceedings of the 8th Great Lakes Symposium on VLSI*, 1998, pp. 344-350.

[12] P. Zarkesh-Ha, J. A. Davis, W. Loh and J. D. Meindl, "Prediction of Interconnect Fan-Out Distribution Using Rent's Rule", *Proc. ACM Intl. Workshop on System-Level Interconnect Prediction*, 2000, pp. 107-112.