On Switch Factor Based Analysis of Coupled *RC* Interconnects

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Abstract

We revisit a basic element of modern signal integrity analysis, the modeling of worst-case coupling capacitance effects within a *switch factor* (SF) based methodology. We show that the exact SF is a function of the ratio of slew times of both aggressor and victim interconnect voltages. Our main result is that $2C_c$ (or, SF = 2), where C_c is the static coupling capacitance, is not a correct upper bound when calculating interconnect delay in presence of crosstalk: we show that for signals modeled as finite ramps the worst case is SF = 3. This has implications for almost all signal integrity methodologies, e.g., window-based approaches that iteratively determine worst-case coupling effects. We have tested our result in a worst-case delay analysis methodology by transforming the coupled RC network to an RC network where each coupling capacitance C is replaced by a capacitance $3C$ to ground. SPICE simulation confirms the accuracy of worst-case delay estimates produced using SF = 3. Delay with SF = 3 can still be underestimating because of exponential waveforms.

1 Introduction

Crosstalk affects the behavior of VLSI circuits in two ways: (i) incorrect functionality through introduction of noise at sensitive nodes, and (ii) increasing (or decreasing) interconnect delays. A major cause of delay, and hence timing, uncertainty is the increasing effect of crosstalk between parallel *RC* interconnect lines in DSM circuits. Here, we focus on the crosstalk that is due to capacitive coupling between lines; this increases with average interconnect length, routing density, and device switching speeds.[1]

Timing and Crosstalk Analysis Methodologies. Transient analysis of crosstalk using circuit simulation tools [4, 3] is computationally expensive and inapplicable to full-chip analysis. *Static* timing analysis by its nature uses static methods and models to verify timing. However, static techniques cannot model wire delays accurately in the presence of crosstalk. Since such tools seek worst-case analyses, the standard signal integrity analysis and performance optimization methodology multiplies coupling capacitance by a *switch factor* (SF) to yield an "equivalent" grounded capacitance that is used in delay and noise calculations.[2] Analysis of victim line delay in the presence of crosstalk from a neighboring aggressor line[3] assumes that switch factors range between 0 and 2, i.e., the worst-case capacitive loading due to crosstalk is $2C_c$ (twice the nominal coupling capacitance).

Today, switch factor based delay computation is chiefly used within *iterative* timing analysis methods [2, 5]. Iteration is needed to address the "chicken and egg" problem of computing crosstalk-dependent delays [12]. The approach starts with the worst possible switch factor between coupled nets. Then, using timing tool results – and depending on signal arrival and transition times – the switch factor values are updated in the range between 0 and 2, and this procedure usually converges within several iterations.

We note that in such timing verification methodologies, the worst-case coupling is assumed to occur when the victim and aggressor signals switch at the same time and with same transition times (or, typically, assuming no transition time – i.e., a step input). Such assumptions are used throughout the industry and academia to provide an "upper bound" on capacitive coupling. [11] demonstrates that SF = 2 yields pessimistic results; since this result, designing circuits and interconnects with an SF = 2 assumption has been the de facto industry standard. In [10] the time average of effective capacitance is shown to be $2C_c$. The authors of [13] suggest that using $2C_c$ as an upper bound in computing wire delays leads to overestimation and unnecessarily increases the area and power of the design. They also indicate that SF = 2 can be optimistic for some cases and conclude that this is due to decomposition of signal paths into stages, where each stage begins at the output of a gate and extends through to the output of next gate on the path.

Contributions of this work. In this paper, we revisit the foundation of modern switch factor based analysis methodology, namely, the assumption that the constant 2 (as in SF = 2) is "special". Recall that coupling is a function of signal arrival times and slew times of coupled lines. In reality, the signals arrive at different times and switch with different slew times on neighboring (or coupled) lines. We show that the true effective capacitance, i.e., *exact switching factor*, is a function of ratio of slew times of both aggressor and victim lines. We prove that $3C$ is the worst case for linear ramp voltages if the rise (fall) of the aggressor is at least twice as fast as the fall (rise) of the victim. Other required conditions to have SF =3 are that the aggressor voltage starts its transition before the victim line voltage reaches its reference voltage level, and this time differ-

[1] In current processes, coupling capacitance for a given wire can be as high as the sum of area and fringe capacitances, and coupling capacitances will be even more dominant in future processes [1].

[2] This is based on heuristic charge-sharing analysis. The resulting decoupled *RC* network allows independent analysis of interconnects, hopefully without affecting the accuracy of the worst-case analysis.

[3] A line which generates a switching event is called the "aggressor", and the line which is affected by this switching is called the "victim".

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ence should equal the aggressor slew time. For non-linear (e.g., exponential) voltage waveforms the worst case coupling capacitance could be greater than 3C. The analysis of worst case switch factor for computing maximum delay on the victim line (setup time analysis) symmetrically applies to yield a best-case switch factor of -1 (for hold time analysis).

To assess the impact of our analysis on worst-case coupling delay analysis, we have implemented a simple technique that modifies an extracted RC network by replacing each coupling capacitance C by a grounded capacitance 3C. SPICE simulations on typical coupled nets, compared with our analysis results, show that using SF = 3 yields wire delays within 5% of the actual delay for the exact coupled RC network. However, as the slew time at the victim line input increases, delay with SF = 3 underestimates actual wire delay because of the exponential wvaeform at each node of the RC network. Below, we show three real configurations wherein the aggressor and victim line slew times can differ, and generate transitions leading to this worse behavior.

2 Exact Switch Factor Analysis

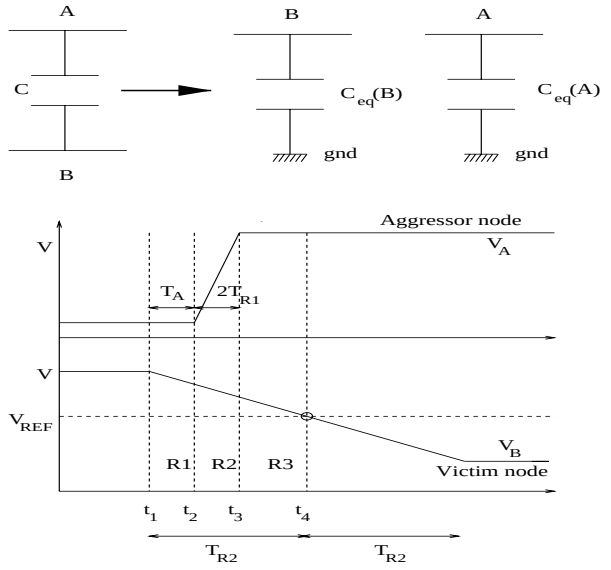

Figure 1: Voltage at nodes A and B modeled as linear ramps. V_A is a fast rising ramp with slew time $2T_{R1}$ (i.e., 0 to 100% transition times) and V_B is a slow falling ramp with slew time $2T_{R2}$. V_{REF} is the 50% *reference voltage* threshold for switching between different logic states.

Consider a single coupling capacitor with static capacitance value of C connected between nodes A (aggressor) and B (victim) in Figure 1. We seek the equivalent capacitances from nodes A and B to ground (see the Figure) so that total current through the equivalent capacitance is same as the original coupling capacitance between nodes A and B. We use ramp functions of arbitrary amplitude V for the voltages at the two nodes. (Additional details are given in [9].)

2.1 Worst-case Switch Factor

Assume that voltage V_A is a rising ramp with slew time $2T_{R1}$ (where T_{R1} is the 0 to 50% transition time) and voltage V_B is a falling ramp with slew time $2T_{R2}$. V_{REF} (typically 50% of supply voltage) is the *reference voltage* threshold for switching between different logic states. We also assume that $T_{R2} >> 2T_{R1}$, so that the entire transition of V_A could take place before V_B reaches the V_{REF} level. (The worst case victim line delay occurs when the aggressor net/node A switches fast, and the victim net/node B switches slowly in the opposite direction.)

Let the voltage at node B start its transition at time t_1 and reach V_{REF} at time t_4, as indicated in Figure 1. Similarly, the voltage at node A starts transitioning at time t_2 and reaches its final value at time t_3. Let $T_A = t_2 - t_1$. We observe three distinct regions R1, R2 and R3 of overlap for the transitioning voltages V_A and V_B. To compute the equivalent capacitance (or *exact switch factor*) during the transition period as seen by node B, we analyze behavior of the static capacitor in the three regions between t_1 and t_4.

In **region R1** the voltage at node A is constant (at logic 0) while node B is switching. The effective capacitance seen by voltage V_B is same as the static capacitance, i.e., $C_{eq}^{R1}(B) = C$. In **region R2** both node voltages are switching in opposite directions, hence the effective capacitance is computed by considering the individual currents drawn by voltages at each node. Note that if V_A is held at constant voltage then the only current through the equivalent capacitor is due to the voltage transition at node B, and is given by $i_{C_{eq}}(B) = C_{eq}(B)\frac{dV_B}{dt} = C_{eq}(B)\frac{V}{2T_{R2}}$ (V is supply voltage level). But when both V_A and V_B are switching in opposite directions the total current through the static capacitor is due to voltage transitions at both nodes: $i_C(BA) = C\frac{dV_A}{dt} + C\frac{dV_B}{dt} = C\left[\frac{V}{2T_{R1}} + \frac{V}{2T_{R2}}\right]$. The equivalent capacitance to ground seen by node B is found by equating the currents $i_{C_{eq}}(B) = i_C(BA)$, i.e.,

$$C_{eq}^{R2}(B) = C\left[1 + \frac{T_{R2}}{T_{R1}}\right] = C(1+K) \tag{1}$$

where $K = \frac{T_{R2}}{T_{R1}}$ is the ratio of victim and aggressor slew times.[4] Similarly, if V_B is held at constant voltage then the only current through the equivalent capacitor is due to the voltage transition at node A, and is given by $i_{C_{eq}}(A) = C_{eq}(A)\frac{dV_A}{dt} = C_{eq}(A)\frac{V}{2T_{R1}}$. The equivalent capacitance to ground seen by node A (from equating currents $i_{C_{eq}}(A) = i_C(BA)$) is

$$C_{eq}^{R2}(A) = C\left[1 + \frac{T_{R1}}{T_{R2}}\right] = C\frac{(1+K)}{K} \tag{2}$$

Given the assumption that the aggressor net switches faster than the victim, the upper bound on the aggressor node equivalent capacitance is 2C, which occurs for identical slews ($K = 1$). Finally, in **region R3** the voltage at node A is constant while node B is switching. The current through the static capacitor is a function of voltage difference $\Delta V = V_A - V_B$ between the nodes; since this difference is less than in region R1, the effective capacitance seen by voltage V_B is less than or equal to static capacitance, i.e., $C_{eq}^{R3} \leq C_{eq}^{R1} = C$.

Since we wish to model the switch factor over the complete switching window, we must compute a *time-average* worst case switch factor over the three regions. Unlike the equivalent capacitance in Region 2, the total equivalent capacitance seen by the voltage at node B (i.e., time average of all three effective capacitances) turns out to be bounded. We see:

$$C_{eq}^{tavg}(B) \quad = \quad \frac{T_A * C_{eq}^{R1} + 2T_{R1} * C_{eq}^{R2} + (T_{R2} - T_A - 2T_{R1}) * C_{eq}^{R3}}{T_{R2}}$$

[4] Note that the equivalent capacitance at victim node B linearly increases with slew ratio K, and is hence *unbounded*. For example, if the slew times are $T_{R1} = 50ps$ and $T_{R2} = 1000ps$ then the equivalent capacitance at victim node B is equal to $C_{eq}^{R2}(B) = 21C$, which can significantly affect the delay of the victim net. This maximum value, which occurs in one region of the switching window, cannot be used as the overall worst case switch factor (delay results will be too pessimistic) because the other two regions have equivalent capacitance less than or equal to C.

$$= \frac{T_A * C + 2T_{R1} * C[1 + \frac{T_{R2}}{T_{R1}}] + (T_{R2} - T_A - 2T_{R1}) * C_{eq}^{R3}}{T_{R2}}$$

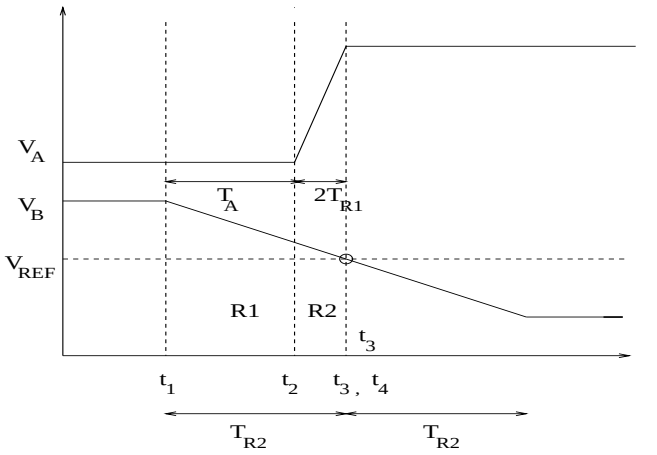

Figure 2: Worst-case configuration such that fast transition at node A overlaps with the slow transition at node B at the time close to reference V_{REF} voltage. In this configuration the time points t_3 and t_4 coincide and the region R3 does not exist.

Total effective capacitance is maximized when the contribution of region R3 C_{eq}^{R3} is reduced and that of region R1 C_{eq}^{R1} is increased. For this to happen, the starting time when node A transitions should be $T_A = T_{R2} - 2T_{R1}$ as shown in Figure 2. In this configuration, only regions R1 and R2 are present and region R3 disappears.

$$C_{eq}^{tavg}(B) = \frac{(T_{R2} - 2T_{R1}) * C + 2T_{R1} * C[1 + \frac{T_{R2}}{T_{R1}}]}{T_{R2}} = 3C \quad (3)$$

Hence, we have a worst-case capacitive coupling factor of three times the static capacitance. Equation (3) is valid with the following assumptions: for linear ramps at nodes A and B, $T_{R2} \geq 2T_{R1}$, and $T_A \leq (T_{R2} - 2T_{R1})$ or $t_2 \leq (t_4 - 2T_{R1})$. Cases with different amounts of overlap are discussed below. The maximum value of the equivalent capacitance seen by the voltage at node A occurs when both voltages start switching at the same time, and is given by $C_{eq}(A) = C\frac{(1+K)}{K}$.

Partial overlap of node voltages. We have seen that maximum coupling occurs if the ramp of voltage A completely overlaps the ramp of voltage B before voltage B reaches V_{REF}. In Figure 1 the fast voltage transition at node A completely overlaps with the slower voltage transition at node B. For this "overlap region" to occur,[5] node A must start its transition at $t_2 \leq (t_4 - 2T_{R1})$. The overlap time period itself can be expressed as $K_A T_{R1}$, where K_A is between 0 and 2. For $K_A < 2$ the voltage V_A *partially* overlaps with voltage V_B, i.e., region R1 is present and region R2 is only partially occurs. In this case, total effective capacitance is

$$C_{eq}^{tavg}(B) = \frac{(T_{R2} - K_A T_{R1}) * C + K_A T_{R1} * C[1 + \frac{T_{R2}}{T_{R1}}]}{T_{R2}} = C(1 + K_A)$$

This equation is valid for linear ramps at nodes A and B, and $t_2 \leq t_4$ or $T_A \leq T_{R2}$. If the voltage at A starts the transition after the voltage at node B reaches V_{REF}, then the total effective capacitance seen is the same as the static capacitance C, i.e., when $t_2 \geq t_4$ or $T_A \geq T_{R2}$.

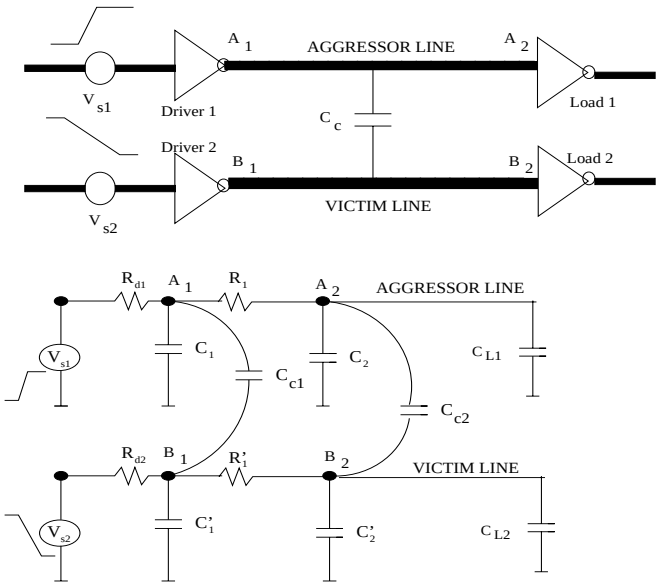

Figure 3: Two parallel coupled interconnects, with inverters as drivers and loads. This configuration is used for our analysis of optimal switch factor for victim and aggressor lines.

Identical slew times. When both node voltages have identical slew times $T_{R2} = T_{R1}$, the total effective capacitance is due solely to the overlap capacitance: only region R2 exists, i.e., $C_{eq}^{tavg}(B) = C_{eq}^{tavg}(A) = C[1 + \frac{T_{R2}}{T_{R1}}] = 2C$.

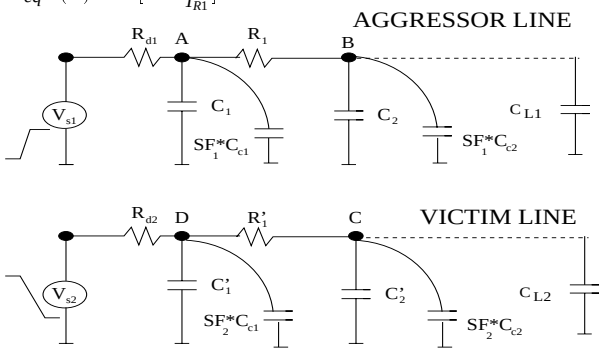

Figure 4: Modeling the coupling capacitance between the neighboring lines as a lumped capacitance to ground and scaling the value by an effective switch factor value.

2.2 Best-Case Switch Factor

Let V_A and V_B switch in the **same direction**, i.e., V_A is a falling ramp with slew time $2T_{R1}$ and V_B has slew time $2T_{R2}$. Again, assume $T_{R2} >> 2T_{R1}$ so that the entire transition of V_A can take place before V_B reaches V_{REF}. Total current is $i_C(AB) = C\frac{dV_A}{dt} - C\frac{dV_B}{dt} =$

[5] We call this the "overlap region" because the switching of both node voltages overlaps in this region. We also refer to the effective capacitance seen in this region as the *overlap capacitance*.

$C\left[\frac{V}{2T_{R1}} - \frac{V}{2T_{R2}}\right]$, and similar analysis to above gives $i_{C_{eq}}(B) = C_{eq}(B)\frac{dV_B}{dt} = C_{eq}(B)\frac{V}{2T_{R2}}$. The equivalent capacitance to ground seen by node B is

$$C_{eq}^{R2}(B) = C\left[1 - \frac{T_{R2}}{T_{R1}}\right] = C(1-K) \quad (4)$$

which can be negative – the victim line delay can be significantly smaller than the wire delay obtaining by neglecting (zeroing with SF = 0) the coupling capacitance. Again similarly to above, we may obtain the equivalent grounded capacitance seen by node A:

$$C_{eq}^{R2}(A) = C\left[1 - \frac{T_{R1}}{T_{R2}}\right] = C\frac{(K-1)}{K} \quad (5)$$

Because the equivalent capacitance at the aggressor node is always equal to or less than the coupling capacitance C, the smallest time-average equivalent capacitance at node B occurs when node A switches at the same time as node B. In this configuration, region R1 disappears. We obtain a *negative* (!) lower bound on best-case equivalent capacitance at node B:

$$\begin{aligned} C_{eq}^{tavg}(B) &= \frac{T_A * C_{eq}^{R1} + 2T_{R1} * C_{eq}^{R2} + (T_{R2} - T_A - 2T_{R1}) * C_{eq}^{R3}}{T_{R2}} \\ &= \frac{2T_{R1} * C[1 - \frac{T_{R2}}{T_{R1}}] + (T_{R2} - 2T_{R1}) * C}{T_{R2}} = -C \end{aligned} \quad (6)$$

3 Model for Coupled Interconnects

To assess the impact of our analysis on worst-case coupling delay methodology, we apply a simple technique that modifies an extracted RC network by replacing each coupling capacitance C by a grounded capacitance $3C$. (We will also present real examples where the aggressor and victim line slew times could differ, and generate transitions leading to even worse behavior.) We consider two parallel coupled interconnects with drivers and loads attached. In this configuration both drivers are on the same side and we assume different slew times at the inputs of the wires. An equivalent circuit using many segments of Π models for the interconnects and distributed coupling capacitances is used for accurate calculation of the interconnect delays. We then reduce this coupled RC interconnect to a distributed lumped RC line with coupling capacitance scaled by *switch factor* as shown in Figure 4. For the victim line, the switch factor is represented using $SF_2 = 3C$ from Equation (3), and for the aggressor line we use $SF_1 = C\frac{(1+K)}{K}$ from Equation (2). Note that these two switch factors are different for any configuration of slew times at the input of the lines. The optimal value for both these switch factors is calculated separately such that 50% threshold delay of coupled RC circuit matches the lumped RC circuit with switch factors.

Circuit Number	width (in μm)	spacing (in μm)	length (in μm)	R_{int} (in Ω)	C_{gnd} (in fF)	C_{coup} (in fF)
1	0.32	0.36	1200	229	63	84
2	0.32	0.36	2000	381	105	140
3	0.84	0.76	5000	363	570	170
4*	0.56	0.56	4000	188	245	334

Table 1: Interconnect parameters used in various SPICE simulations (C_L = 91.5 fF due to inverter gate capacitance for all cases). *Circuit 4 is based on different process technology and the gate load used is C_L = 96 fF.

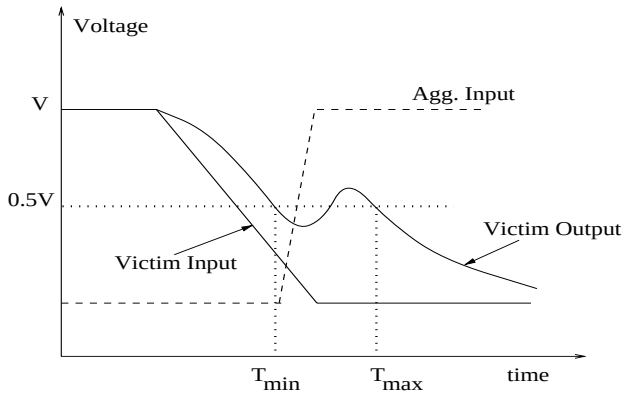

Figure 5: Typical waveform of coupled victim and aggressor wires. The victim line waveform is non-monotone due to aggressor switching. The delay of the victim line increases from T_{min} to T_{max} because the aggressor switching slows down the falling victim signal.

4 Simulation Results

To study the correlation between coupled RC network and the derived RC network with capacitances multiplied by switch factors, we considered four different real configurations: (i),(ii) two identical lines coupling for full length with drivers on the same side, and on opposite sides; (iii) three identical lines with all drivers on the same side; and (iv) three identical lines with aggressor line drivers on the same side but victim line drivers on the opposite side. We use global M5 interconnects from a recent microprocessor design in 0.25 μm CMOS technology. We assume identical interconnects are driven by identical inverters of size (56,23) μm, and also assume that the loads at the end of the lines are identically sized inverters. We study various configurations of interconnect length, width, and spacing with parameters as given in Table 1. The context for this experimentation is to discover how closely our proposed optimal SF = 3 model compares to the full coupled *RC* model, using SPICE simulations.

Figure 5 shows the typical victim line waveform, which is non-monotonic when the aggressor line is switching in the opposite direction. The delay of the victim line increases from T_{min} to T_{max} because the aggressor switching slows down the falling victim signal. Even though the load gate at the end of the victim line starts to trigger at T_{min} the output of the load gate will be delayed due to the non-monotonic behavior of the victim signal, which affects the gate delay.

Our simulations of the above configuration show that using SF = 3.0 yields accurate delays when compared to the coupled model (see Table 2). The worst case switch factor for the victim line could occur at any of the capacitance nodes in the equivalent circuit when the aggressor has a small slew time and the victim has a large slew time window. As the signal propagates down the victim line the shape of the signal is more like an exponential than a ramp, and hence the 50% threshold delay on the victim line for coupled *RC* configuration becomes slightly greater than the delay value computed using SF = 3. This implies that for signals other than ramps the switch factor could be higher than 3.

4.1 Coupled Lines with Opposite-Side Driver Configuration

Figure 7 shows two parallel coupled interconnects with drivers on opposite sides, with slow victim slew time and faster aggressor slew time. This configuration is common in high-performance ICs.

Circuit Number	Driver Loc.	Victim /Agg. Slew	50% threshold delay (ps)			
			Coupled RC	SF=1	SF=2	SF=3
1	Same	400/100	60	38	47	57
2	Same	400/100	134	80	104	128
3	Same	400/100	205	154	178	201
4	Same	400/100	209	100	154	195
4	Same	1000/100	303	104	165	225
4	Opp.	400/100	228	100	154	195
4	Opp.	1000/100	330	104	165	225

Table 2: Comparison of 50% threshold delays of victim line for various SF values, versus coupled RC configuration. We use two coupled lines with drivers on the same side, or on opposite sides.

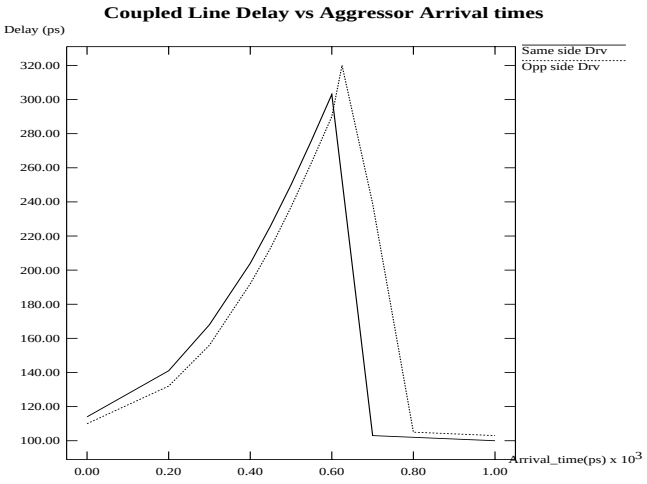

Figure 6: Change of victim line delay with the variation of arrival times of the aggressor input signal, using Circuit 4 parameters. Arrival time of the aggressor signal is computed with reference to the start of the victim signal transition. Victim slew time is 1000ps and aggressor slew time is 100ps.

When switching on the victim line reaches the load at the end of the line, the voltage at that point has a large exponential waveform due to line parasitics. Now, if the aggressor line switches just before the victim line reaches the reference voltage (say 50% threshold), then the above-described worst case switching occurs. Note that the effective coupling capacitance can be much greater than three times nominal, again due to the exponential waveforms at the nodes of the coupling capacitance. Results of simulations with this configuration are summarized in Table 2. The delay of the victim line with SF=3.0 still underestimates the coupled line delay for Circuit 4 with slew times 1000ps/100ps and 400ps/100ps. Both the same side and the opposite side driver configurations yield identical delay results for the circuit model with switch factors, since identical RC circuits are simulated. In other words, the switch factor that we derive is a function of only the slew times at the inputs of the lines and cannot distinguish between same and opposite drive configurations.

Figure 6 shows the change of victim line delay with the variation of arrival times of the aggressor input signal (using Circuit 4 parameters from Table 1). Arrival time of the aggressor signal is computed with reference to the starting point of the victim signal. We observe that instances with larger victim line slew times have larger victim line delays.

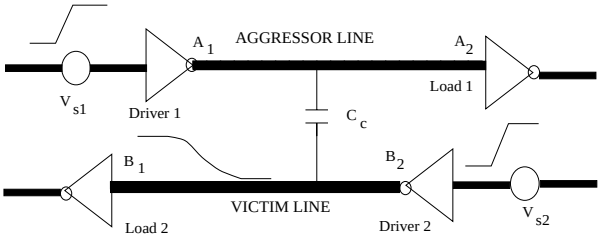

Figure 7: Two parallel coupled interconnects, with drivers on opposite sides. This configuration is used to investigate the case of victim signal switching slowly and aggressor line switching fast, which causes worst case coupling between the lines.

4.2 Two Aggressor and Victim Configuration

We extend our experiments to multiple aggressors, considering two identical aggressors coupling to a victim net for the full length of the line. We use drivers both on the same side and on the opposite side for this simulation configuration. Table 3 shows the victim line delay for various aggressor and victim line slews. Although the victim line delay with SF=3.0 is close to the worst possible delay with coupled line configuration, it is still underestimating the coupled line delay. One conclusion we can again draw from these simulations is that for worst case interconnect delay modeling, we need to use SF greater than 3. Figure 8 shows that victim line delay under coupled configuration is much higher than the delay obtained with the SF = 3.0 per aggressor line model.

Table 3 also shows an interesting comparison of victim line delays for the case when aggressor slew is 100ps and 5ps. The coupled line delay for the case of 5ps aggressor slew is less than for the case of 100ps aggressor slew as shown in Figure 8. We have plotted the worst-case victim line delay peak-noise on victim line for various aggressor slew times in Figure 9. As expected peak noise decreases for higher aggressor slew time (i.e., for smaller aggressor driver sizes) but victim line delay could increase for higher aggressor slew times. This shows a conflict for simultaneous optimization of peak noise and victim line delay by changing aggressor driver size. From the discussion in Section 3.1, the reason for this behavior is that even though effective coupling capacitance is proportional to ratio of aggressor and victim slews, the overlap time window when both aggressor and victim lines switching is small for the 5ps case. This implies that making aggressor driver big (i.e., small slew time) will reduce the worst-case victim line delay. However, from the functionality perspective the bigger aggressor driver injects more noise into the victim line. These are contradictory factors in achieving optimal aggressor and victim driver sizes in the design process.

Last, simulation of the coupled configuration of aggressor and victim lines generates non-linear waveforms instead of linear ramps at the input of the receiver gates. In particular, around the reference (50%) voltage level the victim line waveform has small convex/concave changes, making it very nonlinear and difficult to handle in any gate model characterization. Because of this non-linear waveform behavior at the gate inputs, the gate delay can no longer be computed using linear ramps or simple exponential waveforms.

5 Conclusions

In this paper, we have revisited a basic foundation of today's signal integrity tools methodology. We show analytically that the effec-

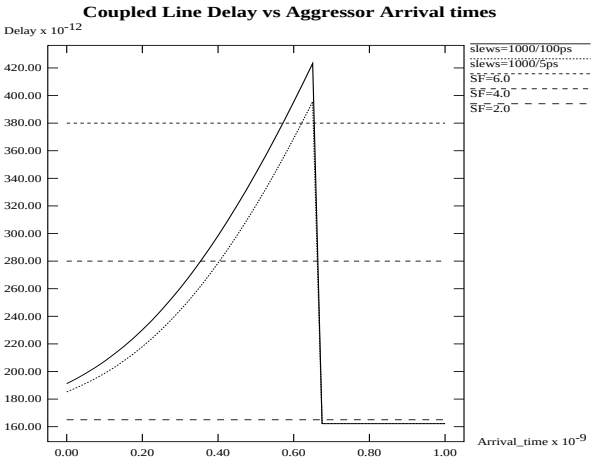

Figure 8: Change of victim line delay with the variation of arrival times of the aggressor input signal for the case of two aggressors with Circuit 4 parameters. This plot shows that victim line delay is less for aggressor slew = 5ps than for aggressor slew =100ps. The plot also shows the delay for various SF values.

Circuits	Driver Loc.	Victim /Agg. Slew	50% threshold delay (ps)			
			Coupled RC	SF=1	SF=2	SF=3
4	Same side	400/100	347	154	241	334
4	Same side	1000/5	400	165	280	380
4	Same side	1000/100	420	165	280	380
4	Opp. side	400/100	360	154	241	334
4	Opp. side	1000/5	410	165	280	380
4	Opp. side	1000/100	435	165	280	380

Table 3: Comparison of 50% threshold delays of two aggressor and victim coupled configuration with victim line delays computed using various SF values. The table indicates SF values for both coupled lines together and hence range from 2.0 to 6.0.

tive capacitance or *switching factor* (*SF*) is a function of ratio of slew times of both aggressor and victim lines. We present a formal proof that SF = 3 represents the worst case and SF = -1 represents the best case for linear ramp voltages. SPICE simulations on typical coupled RC nets, compared with our analysis results, indicate that using SF = 3 as switch factor in the decoupled RC network yields wire delays close to the actual delay for the exact coupled RC network configuration. In high frequency designs, current methodologies that use SF = 2 underestimate interconnect delays; this may result in timing problems with critical nets, and failure to meet cycle time goals in real silicon. (A recent tutorial presentation discusses the use of SF = 4 to capture worst-case coupling effects in the presence of exponential waveforms.) In practice, signals at the nodes of the coupling capacitance are most closely modeled as exponential waveforms, and the effective coupling capacitance of $3C$ may not be a upper bound in such conditions. Our ongoing work is aimed at extending the methodology discussed in this paper to compute worst-case switch factors for coupled nets with exponential signals at the aggressor and victim nodes.

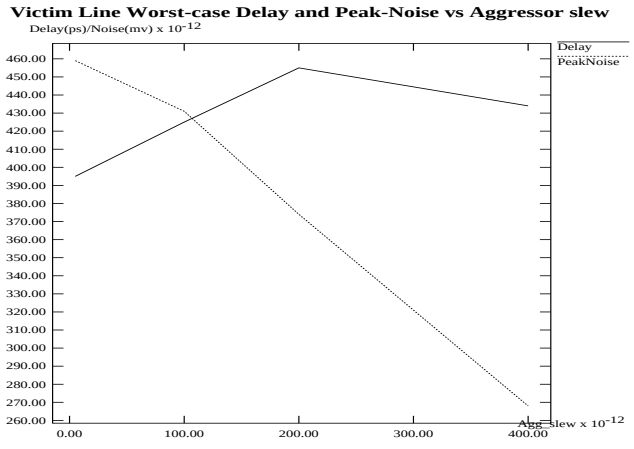

Figure 9: Worst-case victim line delay and peak-noise on victim line are plotted for various aggressor slew times. Peak noise decreases for higher aggressor slew time (or for smaller aggressor driver sizes) but victim line delay could increase for higher aggressor slew times.

References

[1] Semiconductor Industry Association, *National Technology Roadmap for Semiconductors*, 1997.

[2] H. Chin and S. Muddu, "LCK: Latch-based Static Timing Analysis Tool", Silicon Graphics, Inc., 1999.

[3] D. H. Cho, Y. S. Eo, M. H. Seung, N. H. Kim, J. K. Wee, O. K. Kwon and H. S. Park, "Interconnect Capacitance, Crosstalk, and Signal Delay for 0.35 μm CMOS Technology", *Proc. IEEE International Electron Devices Meeting*, 1996, pp. 23.2.1-23.2.4.

[4] N. Chang, V. Kanevsky, B. Queen, O. S. Nakagawa and S.-Y. Oh, "3-sigma Worst-Case Calculation of Delay and Crosstalk for Critical Net", *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, 1997, pp. 104-109.

[5] B. Franzini, C. Forzan, D. Pandini, P. Scandolara and A. Dal Fabbro, "Crosstalk Aware Static Timing Analysis: a Two Step Approach", *Proc. IEEE ISQED*, March 2000, pp. 499-503.

[6] G. A. Katopis and H. H. Smith, "Coupled Noise Predictors for Lossy Interconnects", *IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B* 17(4) (1994), pp. 520-524.

[7] H. Kawaguchi and T. Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed *RC* Lines", *Proc. Asian and South Pacific Design Automation Conference*, 1998, pp. 35-43.

[8] S. Muddu and S. McCormick, "Managing Noise in VDSM Designs", tutorial notes, *Proc. IEEE ISQED*, March 2000.

[9] S. Muddu and E. Sarto "Switch Factor Based Delay Methodology for Coupled *RC* Interconnects", *technical report*, MIPS TREX Microprocessor Group, 1999.

[10] L. Pileggi, "Coping with RC(L) Interconnect Design Headaches", *IEEE ICCAD Tutorial*, Nov. 1995.

[11] T. Sakurai, "Closed-form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's", *IEEE Trans. on Electron Devices* 40 (1993), pp. 118-124.

[12] S. S. Sapatnekar, "On the Chicken-and-Egg Problem of Determining the Effect of Crosstalk on Delay in Integrated Circuits," *Proc. IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP-99)*, 1999, pp. 245-248.

[13] G. Yee, R. Chandra, V. Ganesan and C. Sechen, "Wire Delay in the Presence of Crosstalk", *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, Dec. 1997, pp. 170-175.