The Road Ahead

Error tolerance

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THE *INTERNATIONAL* *Technology Roadmap for Semiconductors* (*ITRS*) states that *error tolerance* is a future "cross-cutting challenge" for design and test. Technology scaling is leading to more (postmanufacturing) permanent failures of devices and interconnects, and more transient errors in the signaling and storage of logic values. Methodology for the former is increasingly costly in terms of guard banding, and methodology for the latter is still under development.

Reliability

Reliability concerns permanent failures during operation. Well-known reliability problems include electromigration, hot-carrier injection, and joule heating:

- *Electromigration* is a consequence of current flow (think of it as an electron wind), which can cause voids in interconnects because of the displacement of the interconnect material.
- *Hot-carrier injection* stems from large electric fields below the gate oxide, which allow electrons to gain energy and embed themselves in the dielectric. This effect worsens when the scaling of feature size is not accompanied by equally aggressive scaling of supply voltage. According to the *ITRS,* oxide thickness will decrease below 2 nanometers (even with the deployment of high-*k* dielectrics) by 2005. In this regime, soft breakdown of gate oxide becomes a concern: There is no catastrophic hard breakdown (formation of a conduction path across the oxide that renders the gate unusable), but there are gradual increases in gate leakage current and shifts in threshold voltage. This is bad news for analog and low-power designs.
- *Joule heating* occurs because higher clock frequencies cause faster charge transfers, which in turn increase collisions and energy dissipation. Interconnect reliability is therefore a function of frequency. Low-*k* dielectrics, which typically offer poor thermal conductivity, worsen joule heating effects.

Today, IC implementation addresses these reliability concerns using simple abstractions. For example, current density limits prevent electromigration, and bounds on gate load capacitance versus output slew time prevent hot-carrier breakdown. Although such approaches are compatible with traditional flows, improved abstractions and analyses are necessary to reduce the amount of guard banding.

Transient errors

With respect to transient errors, the industry's focus is on *soft errors*—random events such as an alpha-particle strike on a storage latch—which cause data in a storage element to flip. In today's leading-edge processes, only two femtocoulombs of capacitive charge hold a bit of data. An excellent discussion of this topic, by Eric Dupont et al., appeared in the May-June 2002 issue of *IEEE Design and Test.*

High-energy particle flux depends on many factors, including altitude and latitude, packaging (unstable isotopes of lead solders), and even the isotopic purity of boron used in implant steps (boron-10 has a high thermal neutron cross section and, when struck by such neutrons, releases energetic alpha particles). With decreasing feature sizes and supply voltages, the value of Q_{crit} (the largest charge that can be injected without changing a memory cell's state) decreases rapidly to

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levels such that even the noise pulse from an alpha particle can be trapped as a logic fault. Designers try to counter this problem through technology (silicon on insulator, or multigate field-effect transistor architectures with lower alpha-particle cross sections), circuit design (error correction or relaxed densities in embedded SRAMs), and even layout techniques (sizing and orientation).

As both permanent and transient failures increase, automatic insertion of robustness into the design will be a key challenge for future design and test technologists. New defect definitions and screening mechanisms are necessary to address, for example, soft breakdowns. And as systems become increasingly complex, they could require hardware redundancy and on-chip reconfigurability (reprogrammable interconnects and reconfigurable control logic) for fault tolerance, development of adaptive and self-correcting or self-repairing circuits, and even software-based fault tolerance.

The *ITRS* provides an intriguing, speculative vision for the future when it notes that "relaxing the requirement of 100% correctness" for devices and interconnects might dramatically reduce the future costs of manufacturing, verification, and test. Today, it seems difficult enough to tolerate permanent and transient errors when the chip begins its lifetime as 100% correct. ■

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