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# “When will the cost of dependability end innovation in computer design?”

## VTS-2015 panel session

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# Huh???

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- IMHO,
- The cost of dependability ...
- ... to the extent that it will constrain or drive anything at all ...
- ... will SPUR innovation, not end it !

*But anyway...*

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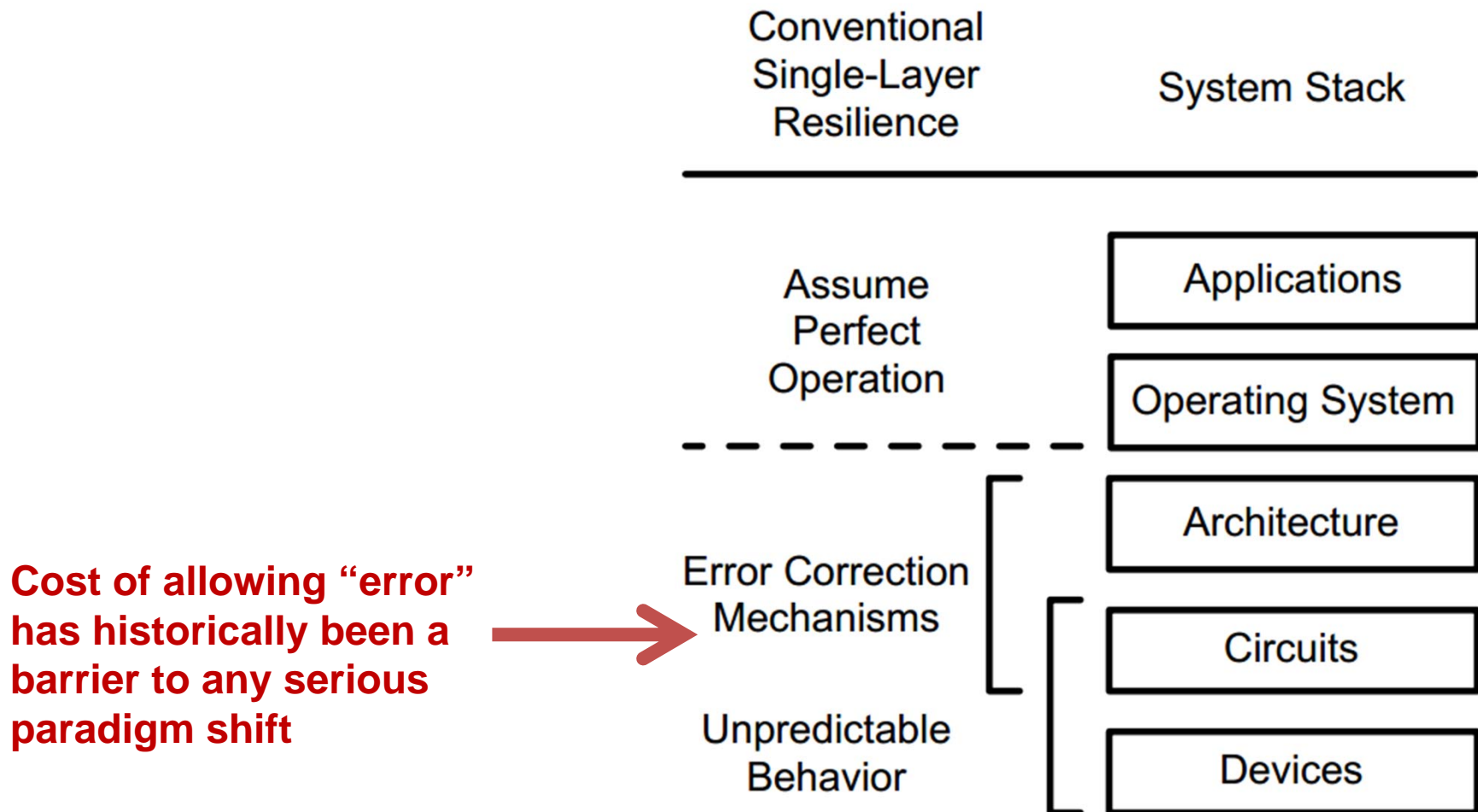
# What “dependability” are we talking about?

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- **With respect to (manufacturing, runtime) variability?**
  - Silicon-signoff or model-hardware miscorrelation → **margin** it, **adapt** to it
  - (same for temperature, voltage, battery condition, ...)
- **With respect to noise and integrity?**
  - Dynamic IR drop → **margin** it
  - (same for thermal gradient, external regulator, ..., PLL jitter, ...)
- **With respect to aging?**
  - BTI aging (10-year library in signoff) → **margin** it
- **With respect to failure?**
  - TDDDB → process **ground rules**
  - HCI, SIV → **design methodology**
  - Signal EM signoff: activity factor = 1.0 assumed on all nets (2.0 for clocks), and still virtually zero violators → **no-op**
  - Power EM signoff (tougher in FinFET nodes) → **margin** it

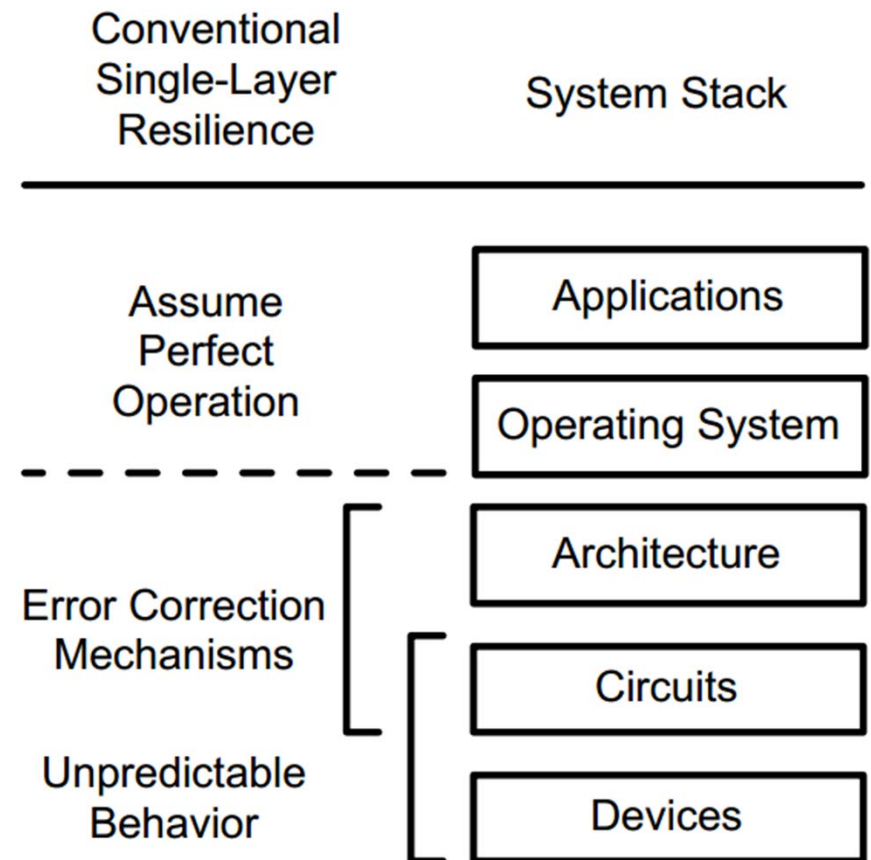
# Resilience = “Long-Term Challenge” in ITRS

- Resilience = system product’s ability to mitigate variability, reliability phenomena



# Resilience = “Long-Term Challenge” in ITRS

- **Resilience = system product’s ability to mitigate variability, reliability phenomena**
- Error detection and repair mechanisms
- “Cross-layer resilience” = recent buzz-phrase
- **Costs, benefits often hazy, difficult to quantify**
- **N.B.: Alternative guardbanding mechanisms for different system abstractions: stochastic, approximate, ...**



# What “cost” are we talking about?

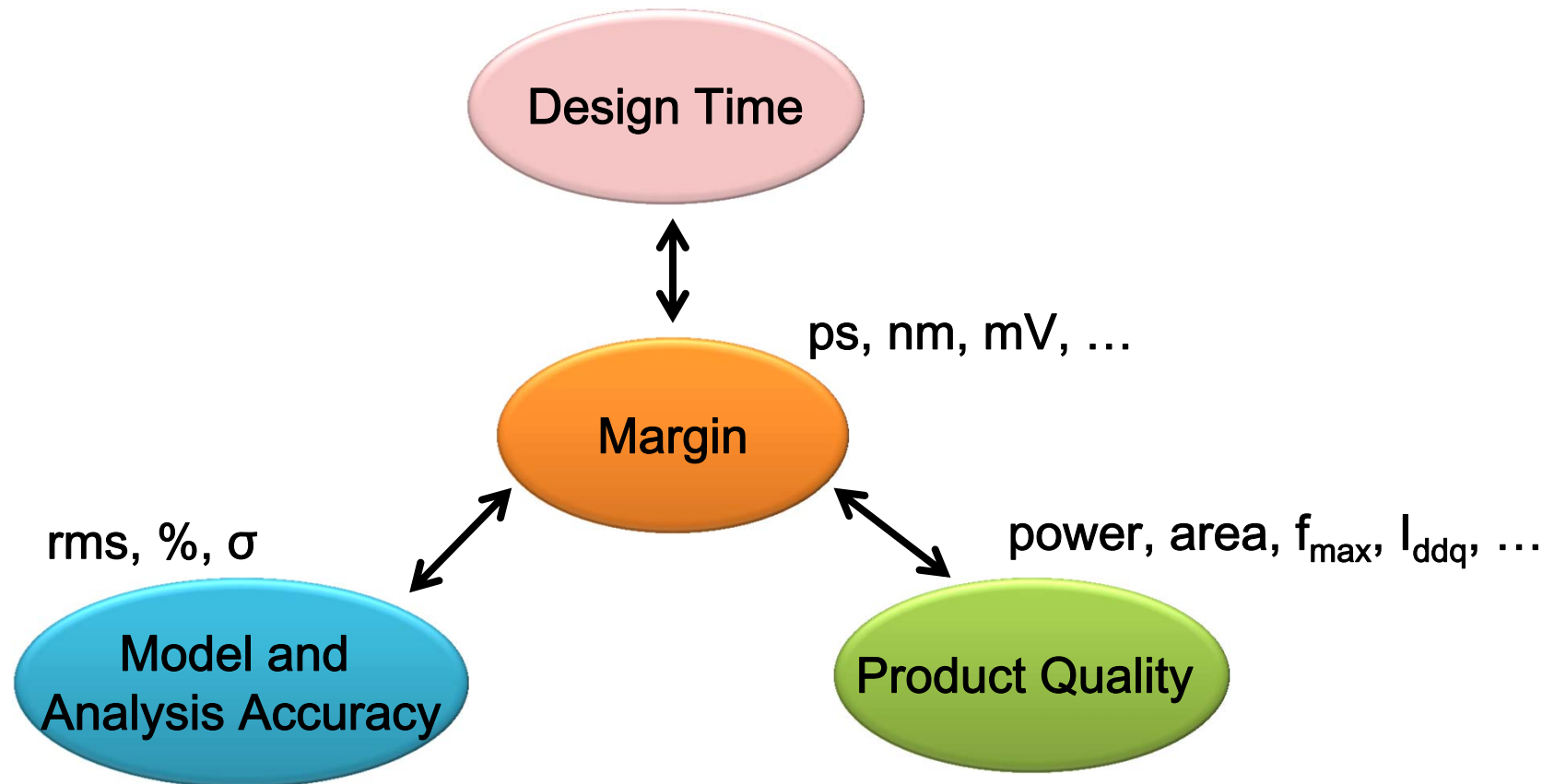
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- **Measuring “Cost of Dependability” is difficult**
  - Reliability margins are intertwined with other margins
  - Tough to isolate specific costs of variability / reliability / resilience, especially in any design-agnostic way

# Reduced Cost = Reduced Margin = My Focus

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- Pessimism removal with more accurate margins
- Explicit tradeoffs across various types of margin  $1 \text{ mV} = 5 \text{ MHz} \dots$
- Co-optimization across engineering scopes, chip implementation phases “cross-layer”, adaptivity / resilience, ...





# What “cost” are we talking about?

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- **Measuring “Cost of Dependability” is difficult**
  - Reliability margins are intertwined with other margins
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- **Assessing Cost of ... (= work at UCSD)**
  - **... Variability**
    - Reducing (phantom) margins: **tightened BEOL corners**, FF timing models
  - **... Reliability**
    - **AVS-BTI-EM: cost of wrong signoff conditions**
    - Non-default routing rules: cost of naïve enforcement of reliability margins
    - “Cost of EM guardband” + assessment of EM margin considering lifetime throughput, performance
  - **... Resilience**
    - “**MinRazor**”: **tradeoff of resilience mechanism cost vs. margin cost**
    - “**PVS**”: process-aware adaptive voltage scaling (design-independent, tunable monitors)

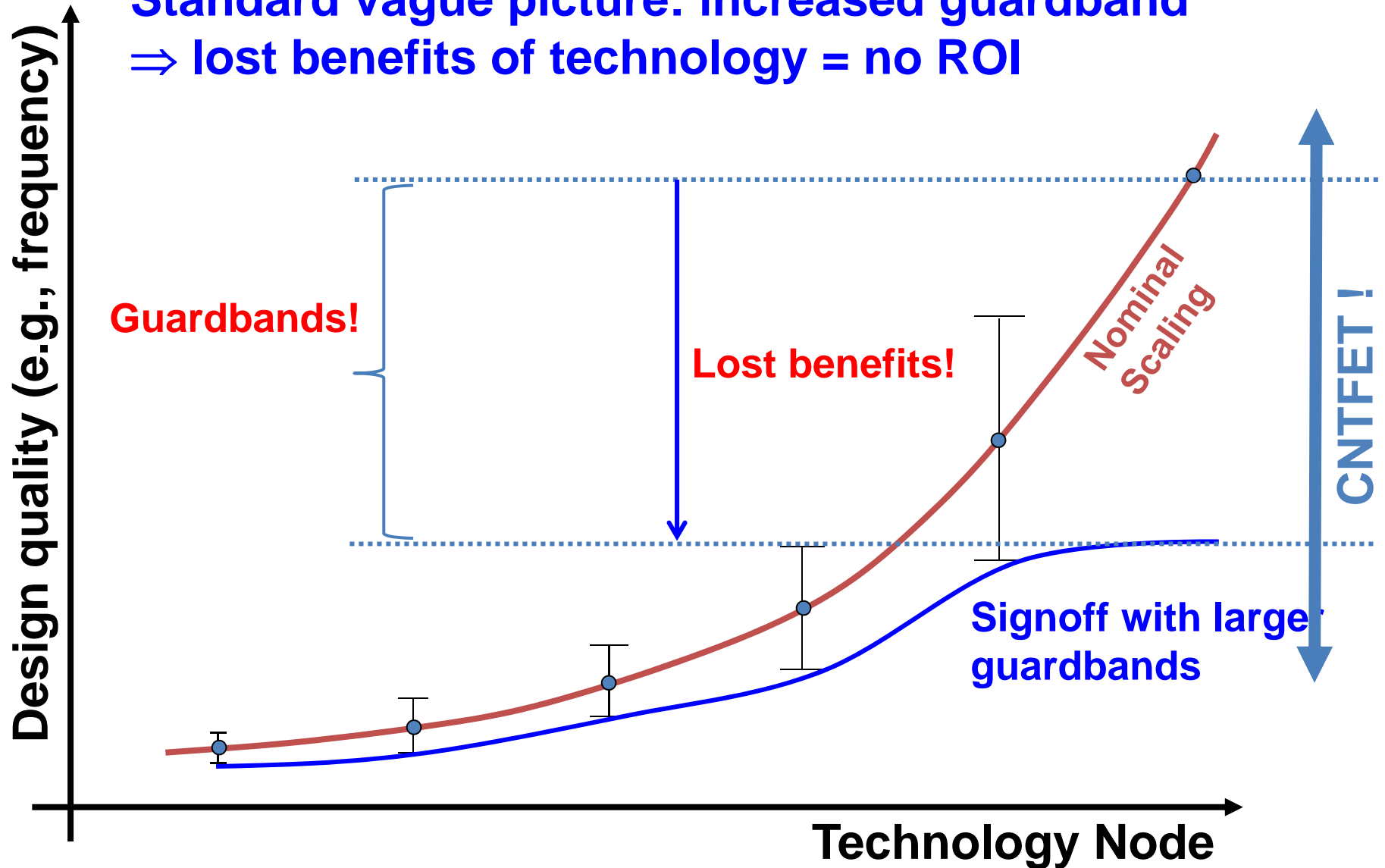
# Please consider:

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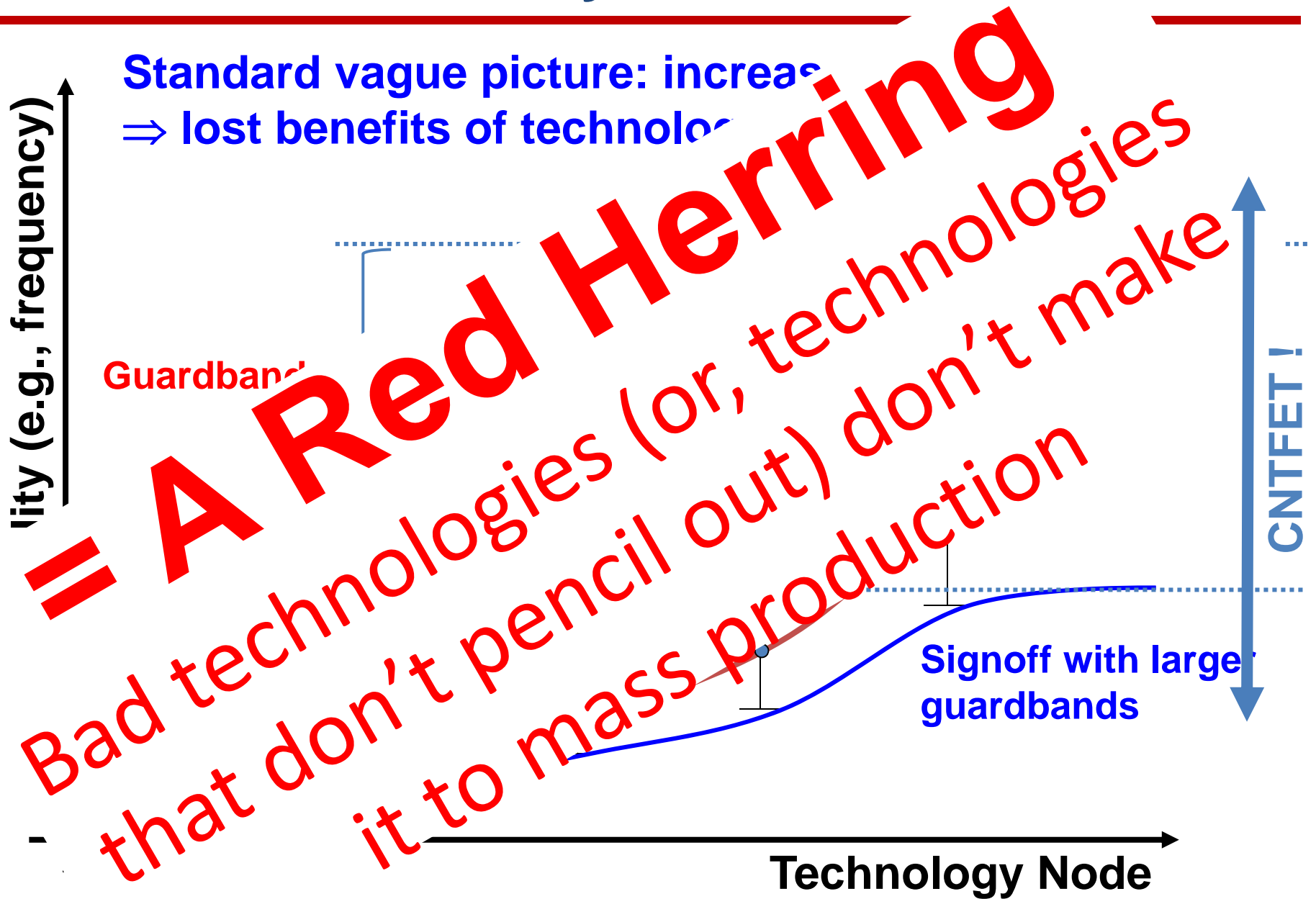
- **We can and do pay for dependability as needed**
- **Consumer, sensor, server, automotive, ...**
  - **In what technologies will these be produced?**
  - **Are fundamentally new dependability requirements in sight for high-volume products?**
  - **If so, what are the cost sensitivities of these products?**
- **Bigger fish to fry (?)**
  - **Performance spec, time to market, ASP, ...**

# On “Cost of Variability and Reliability”

Standard vague picture: increased guardband  
⇒ lost benefits of technology = no ROI



# On “Cost of Variability and Reliability”



# Looking Forward ... (spurring of innovation)

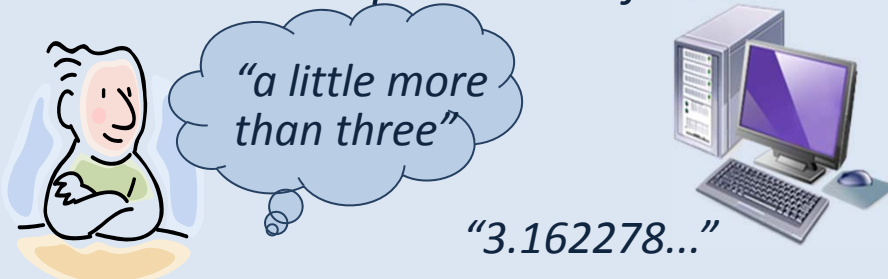
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- **“Innovation in computer design” will be spurred by**
  - IoT: Power and Performance
  - Cost: “Trillions of ...”
  - Energy (~ cost): green, energy-proportional, ...
    - E.g., systems will need to “do nothing well”
- **Examples**
  - Conventional architecture + innovative optimizations
    - > 1 node of scaling simply left on the table today by EDA
  - Approximate computing
  - System design: e.g., “do nothing well”, scenario-specificity
  - *Stochastic computing*
  - *Neuromorphic computing*

# What If We Knew ... (accuracy requirements)

## Approximate Design

What is the square root of 10 ?



"3.162278..."

Approximation could be faster and more powerful

### Problem:

- Accuracy requirement can change during runtime → **benefits of approximation could be reduced**

**Adapt to changing requirements with runtime accuracy configuration**

**[DAC 2012]**

"accuracy-configurable approximate adder"



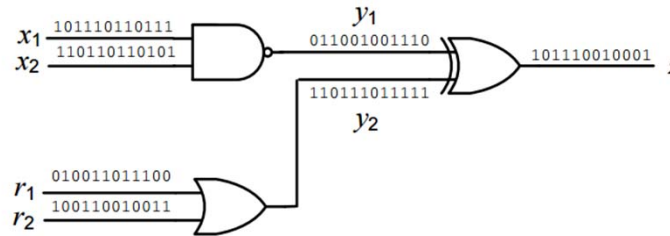
lower power consumption

higher accuracy

# Stochastic Computing

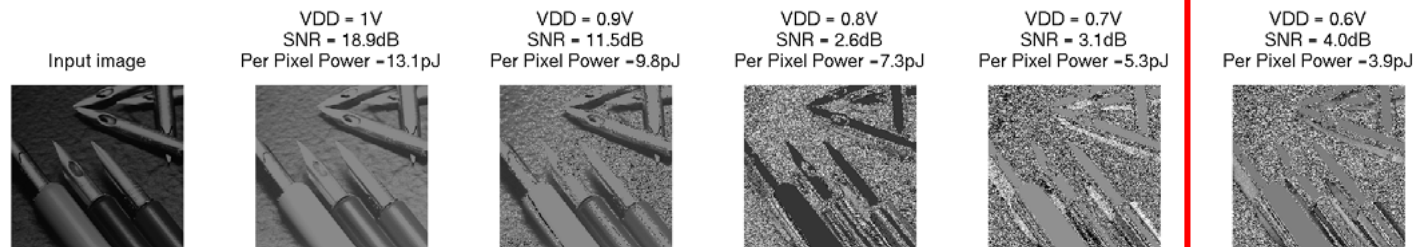
- Conventional computation circuits rely on parallel bits aligned by clock → timing errors are fatal when occur in MSB
- Stochastic circuits are promising architectures, which replace parallel bits with serial bit-stream → resilient to voltage scaling

Example:  $Z = \frac{1}{4} + \frac{1}{2} \cdot X1 \cdot X2$

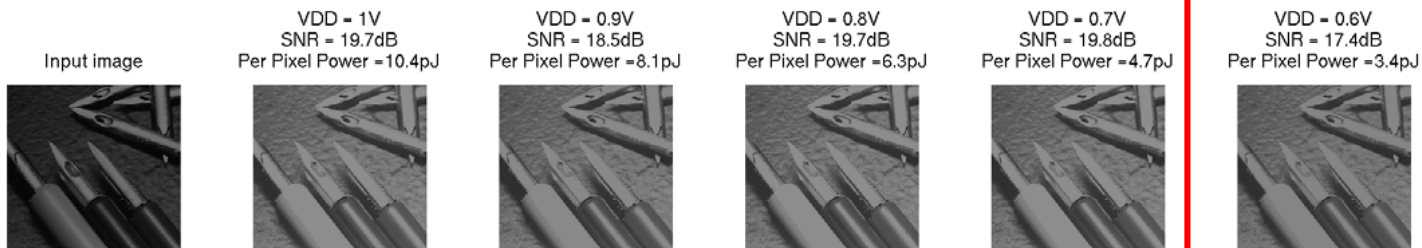


SC is resilient to voltage scaling

Conventional,  
clock period =  
400ps



SC, clock  
period =  
200ps



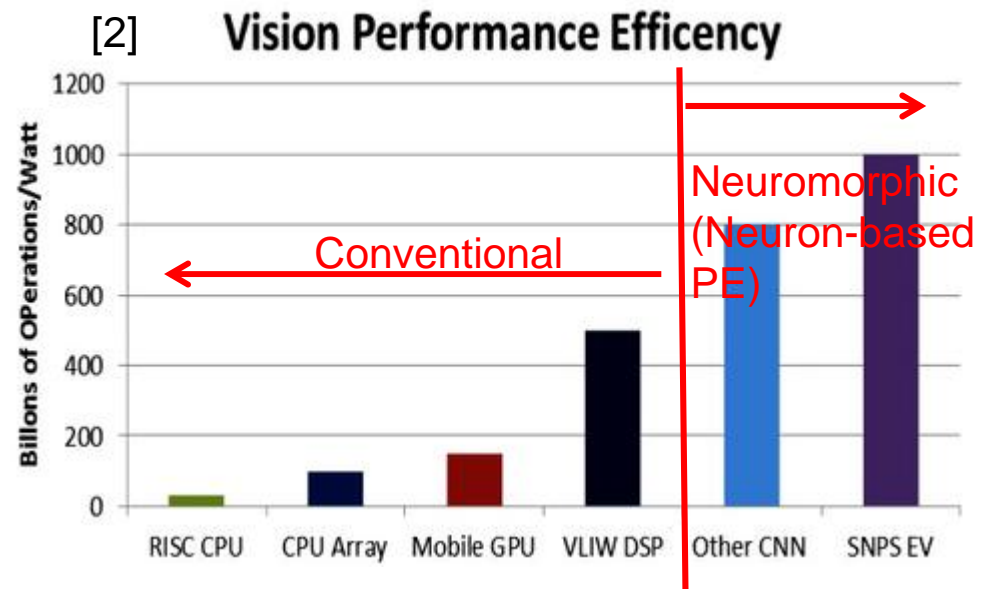
# Neuromorphic Computing

- Conventional:
  - Good at numerical calculation
  - Becoming less energy-efficient to mock human brain (computer vision, pattern recognition, etc.)
- Neuromorphic:
  - Inspired by brain structure
  - Power efficient for recognition problems

[1]

Processing Powers		
	What they do well	What they're good for
Neuromorphic chips	Detect and predict patterns in complex data, using relatively little electricity	Applications that are rich in visual or auditory data and that require a machine to adjust its behavior as it interacts with the world
Traditional chips (von Neumann architecture)	Reliably make precise calculations	Anything that can be reduced to a numerical problem, although more complex problems require substantial amounts of power

MIT Technology Review



[Source]

[1] <http://www.technologyreview.com/featuredstory/526506/neuromorphic-chips/>

[2] [http://www.eetimes.com/document.asp?page\\_number=1&doc\\_id=1326162&image\\_number=2](http://www.eetimes.com/document.asp?page_number=1&doc_id=1326162&image_number=2)



# Looking Forward ... (spurring of innovation)

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  - *Stochastic computing*
  - *Neuromorphic computing*
- **Start from understanding !!!**
  - Dependability ~ area ~ power ~ margin ~ cost
    - All positively correlated and fungible → new system, optimization mindsets
  - Mandatory futures: IoT, 3D, cloud, ...
  - Mandatory helpers: scaling, adaptivity, specialization, path-finding

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**THANK YOU**