Automated Layout and Migration in Ultra-Deep Submicron VLSI

June 25, 1999

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Handouts in .pdf

- HTTP://vlsicad.cs.ucla.edu/DAC99TUTORIAL/
  - will provide .pdf files for updated presentations, and reference lists
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Evaluation Forms

- Part 1: Andrew Kahng CODE = 13
- Part 2: Cyrus Bamji CODE = 11
- Part 3: Maarten Berkens CODE = 12
- Part 4: Chris Strolenberg CODE = 14

What Did We Cover ?

- **New** issues and problems arising in UDSM technology
  - ASIC chip implementation methodology context
  - drivers toward automated-custom **layout**
- Solutions: Custom layout design
  - compaction
  - performance optimization
  - layout synthesis
  - automated-custom (interactive)
- Solutions: Layout-level modifications for perf, yield
  - yield optimization
  - density control algorithms
  - phase-shift mask layout
- Applications: Hard-IP reuse and optimization

Implications of Complexity

- UDSM: Silicon complexity + Design complexity
  - convergent design: must abstract what's beneath
    - prevention with respect to analysis/verification checks
    - many issues to worry about (all are "first-class citizens"
    - apply methodology (P/G/clock design, circuit tricks, …) whenever possible
  - must concede loss of clean abstractions: need unifications
    - synthesis and analysis in tight loop
    - logic and layout : chip implementation planning methodologies
    - layout and manufacturing : CMP/OPC/PSM, yield, reliability, SI, statistical design, …
  - must hit function/cost/TAT points that maximize $/wafer
    - reuse-based methodology
    - need for differentiating IP → **custom**-ization

Implications of Technology

- A hard look at hard IP reuse
  - divergent foundry processes
  - design- and context-specific variants of cells, macros, cores
    - filling densities
    - thermal, noise sensitivity contexts
    - layer usage and local region porosity constraints, physical access
    - incompatibility of separate phase solutions, or phase solutions + local routing
    - tool-specific variants (e.g., for different auto-routers)
    - diffusion sharing, continuous device sizing, tuning (dual Vt, multiple supply voltages (thermal, IR drop contexts), different input arrival times/slews,…)
- Hard-reuse: An ideal that must be tempered by hard realities

Many Worries

- Implications of UDSM technology trends
  - subwavelength lithography
    - WYSIWYG fails completely!
    - OPC, PSM, CMP-driven filling essential for printability, process windows
    - huge worries about broken hierarchy, reusability of layout
  - other yield-driven objectives
    - critical area, antennas
  - signal integrity
    - delay uncertainty, crosstalk noise, IR drop
  - reliability
    - electromigration, AC self-heat, hot electrons
- All of these are first-class objectives
- Can ASIC methodology handle all these effectively?

Recall: ASIC Design → Custom Design

- How much is on the table w.r.t. performance?
  - 4x speed, 1/3x area, 1/10x power (Alpha vs. Strongarm vs. "ASIC")
  - layout methodology spans RTL syn, auto P&R, tiling/generation, manual
  - library methodology spans gate array, std cell, rich std cell, liquid lib, …
- Traditional view of cell-based ASIC
  - Advantages: high productivity, TTM, portability (soft IP, gates)
  - Disadvantages: slower, more power, more area, slow production of std cell library
- Traditional view of Custom
  - Advantages: faster, less power, less area, more circuit styles
  - Disadvantages: low productivity, longer TTM, limited reuse
- What happens when relative cost of Custom decreases ???

Toward Automated-Custom

- Hierarchy of approaches
  - hard-IP migration
    - compaction-centric
    - needs meld with xtor-level performance analyses in tight loop
  - block optimization
    - high-capacity
    - Jiffy-Tune, Einstuner, … CoreMaster, AMPS, …
    - needs meld with migration or layout tools (embedding-relevant process abstraction): poor understanding of, e.g., resizing implications
  - peephole optimization of layout
    - for timing/power/area (e.g., for mismatched input arrival times, slews)
    - for auto-layout (e.g., pin access and cell porosity for router)
    - for manufacturability (density control, critical area, phase-assignability)
    - DOF's: diffusion sharing, sizing, new mapping / circuit topology sol's
    - antecedents: IBM C5M, Motorola CELLERITY, DEC CLEO
    - needs meld with xtor-level performance analyses in tight loop

Toward Automated-Custom

- "Layout or re-layout on the fly" is an element of performance- and cost-driven ASIC methodology going forward
- "Polygon layout as a DOF in circuit optimization" is a very small step from "polygon layout as a DOF in process migration"
  - designers are already reconciled to the latter
- **What you have seen today:** motivation and technology/methodology building blocks for this future

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