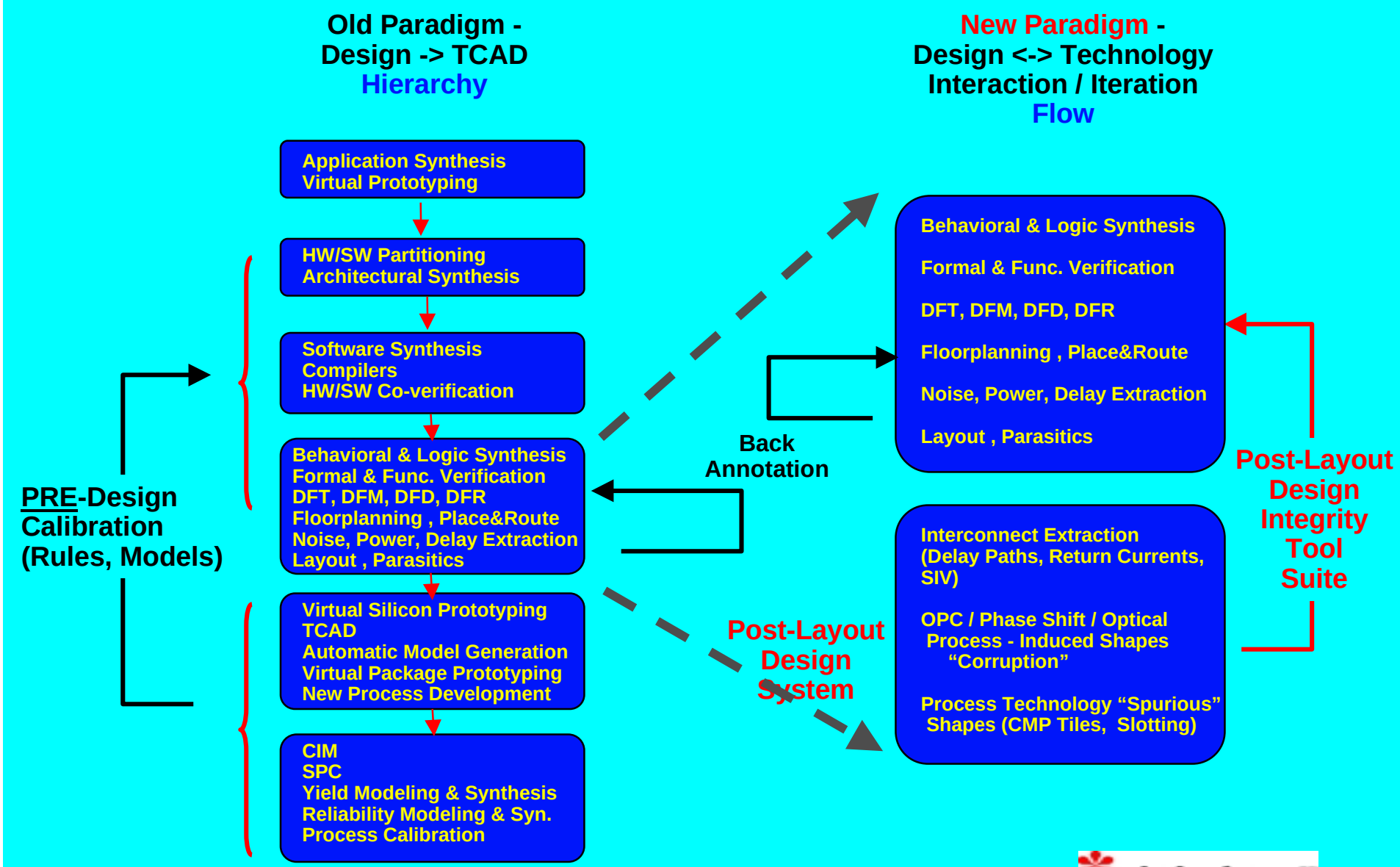
Some New ECAD Tool Domains & Issues for Design Integrity in the Deep Sub- Micron Era

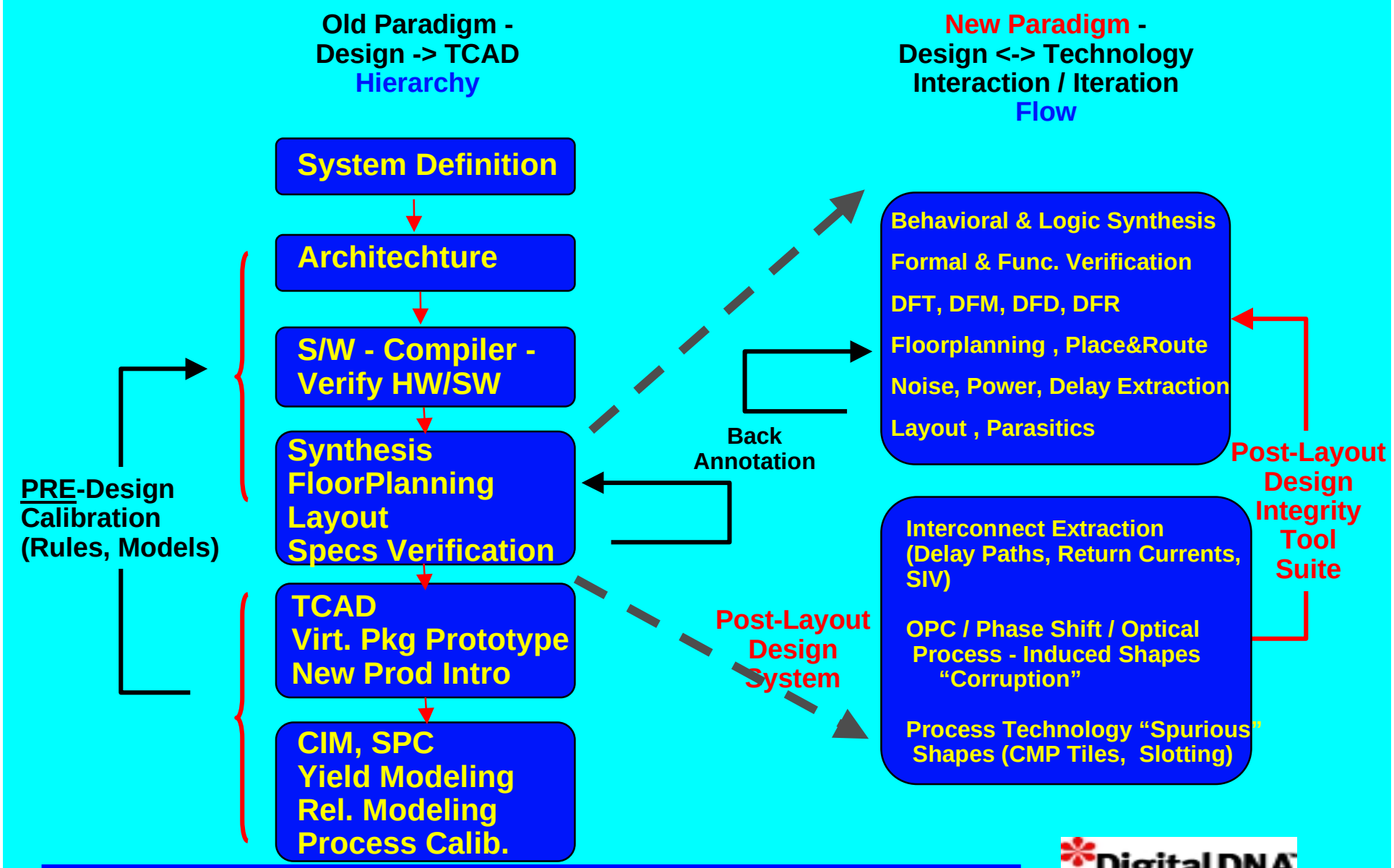
- **Lithography Process - Optics, Resist, Physical Process**
  - Bitcell Parasitics
  - Post-layout DRC
  - Model-Based Optical Proximity Correction
  - Phase-shift Mask
  - New Rules - avoid phase conflicts
- **Chemical-Mechanical Polish Enhancement (Planarity)**
  - Tiles of Metal in Oxide in Large “Missing Metal” Areas
  - Slots in Wide Metal Busses
  - Rule-based Early Post-layout (Delay Verification Compromised)
  - Pre-layout Rules-based Required
- **Interconnect Modeling**
  - Local, Rules-based
  - Non-local, Inductance, Full EM Calculation
  - Hierarchical
  - Strong Connection Between ALL Levels of Design Hierarchy at High f

New ECAD Tools Will Guarantee Design Integrity in Deep Sub- Micron Era



Digital DNA from Motorola
Warren D. Grobman

New ECAD Tools Will Guarantee Design Integrity in Deep Sub- Micron Era



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Strategic Deep-Submicron ECAD Tools and Systems

Process \ ECAD Tool	DRC	Layout	Parasitics (Delay, Power..)	Front-End Rules
Litho Process	Litho Modeling Post-layout	Optical Proximity Layout - Rule-based - Model-based Phase-Shift		✓
Chemical / Mechanical Polish		Tiling / Slotting - Rule-based - Model-based (“Smart”)	Metal Tiles Slots in Metal	✓ ✓
Interconnect			Rule-based Model-based - Local - Non-local - Hierarchical	
Pattern Transfer Process (Etch…)	Post-layout Modeling	?		?

Status of Deep-Submicron ECAD Tools and Systems

Process \ ECAD Tool	DRC	Layout	Parasitics (Delay, Power..)	Front-End Rules
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Interconnect			Rule-based Model-based - Local - Non-local - Hierarchical	
Pattern Transfer Process (Etch…)	Post-layout Modeling	?		?

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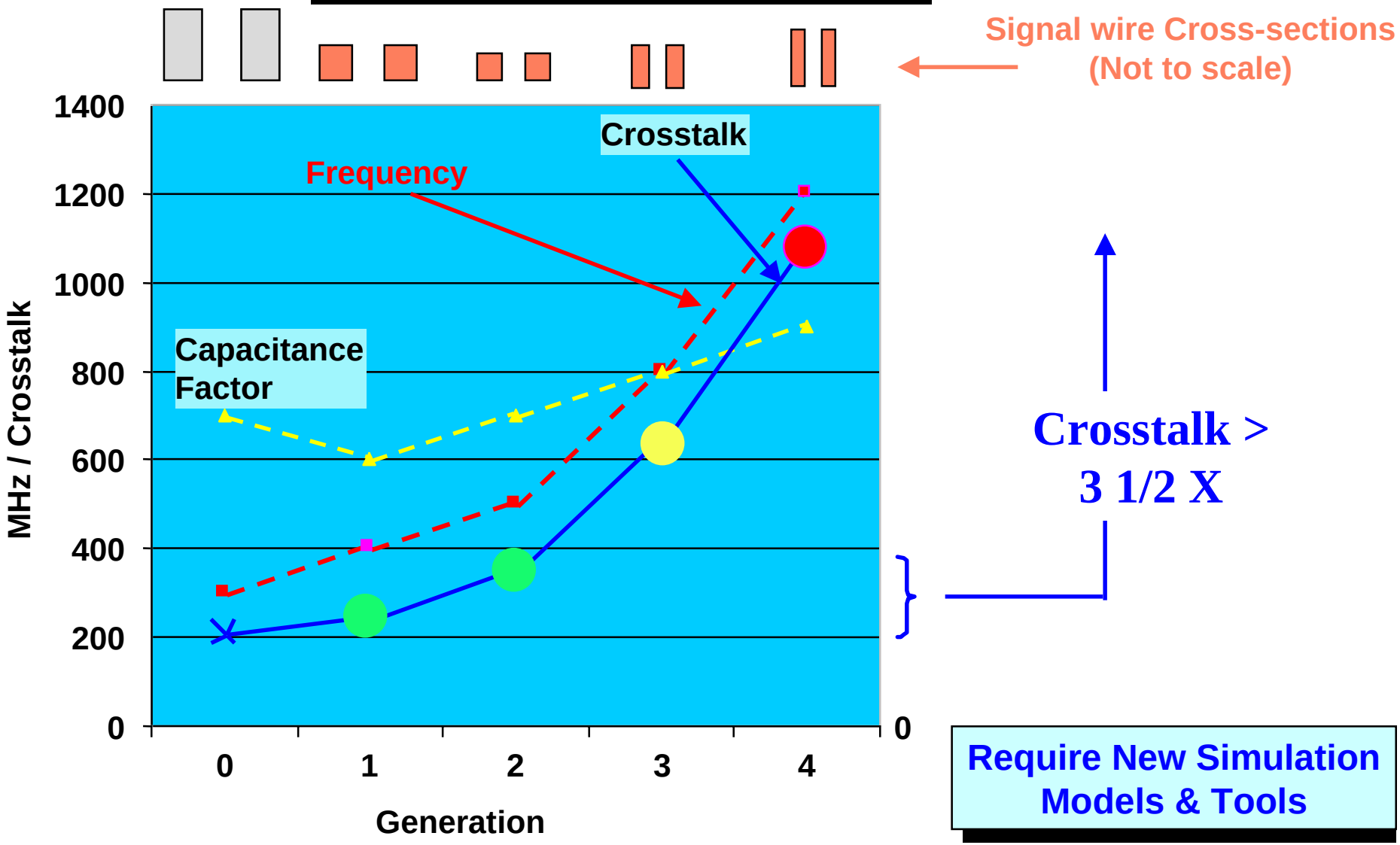
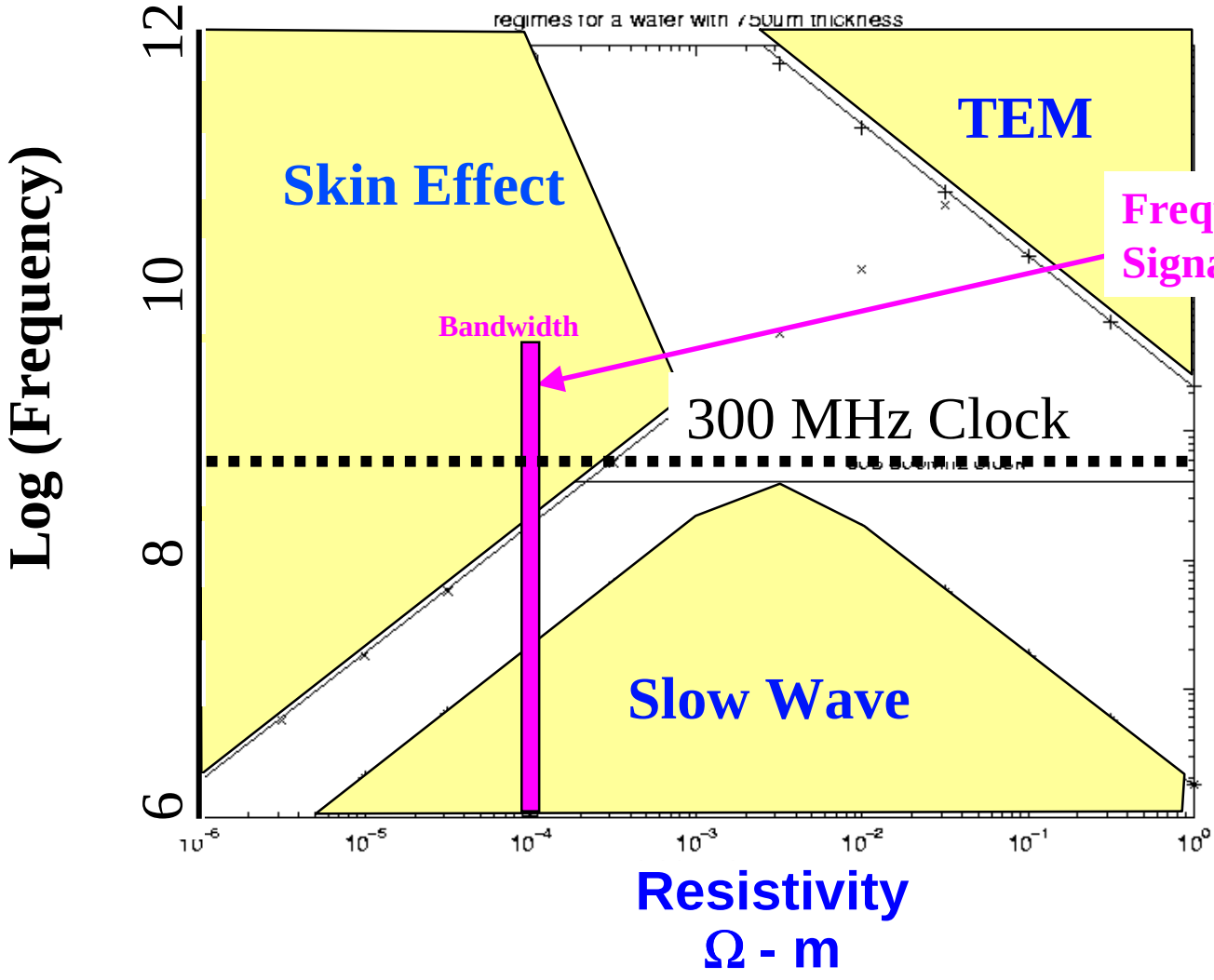
CMOS Circuit Trends (Schematic)
SIGNAL INTEGRITY ISSUE



Signal Propagation Regimes
Wafer t = 750 μm



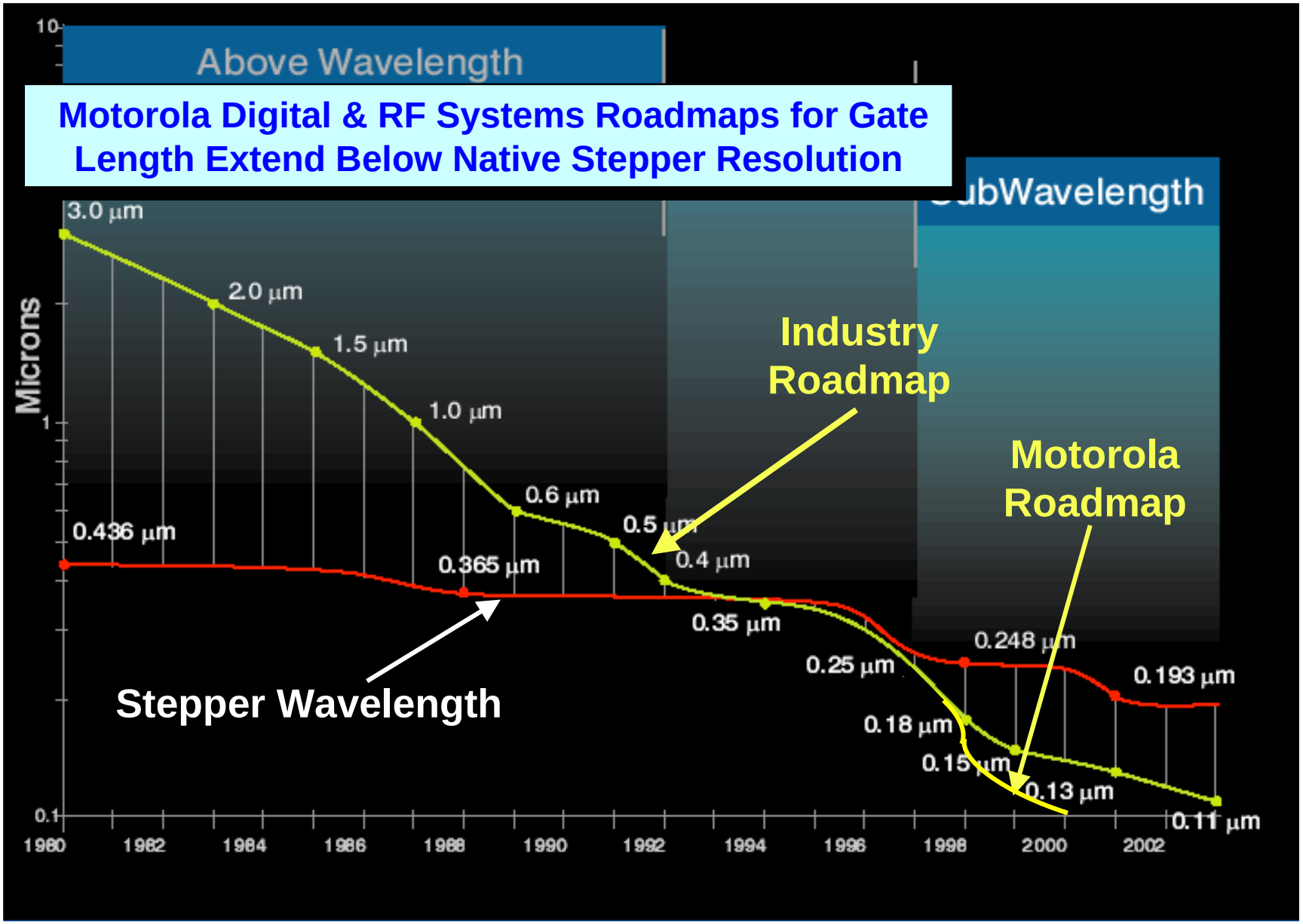
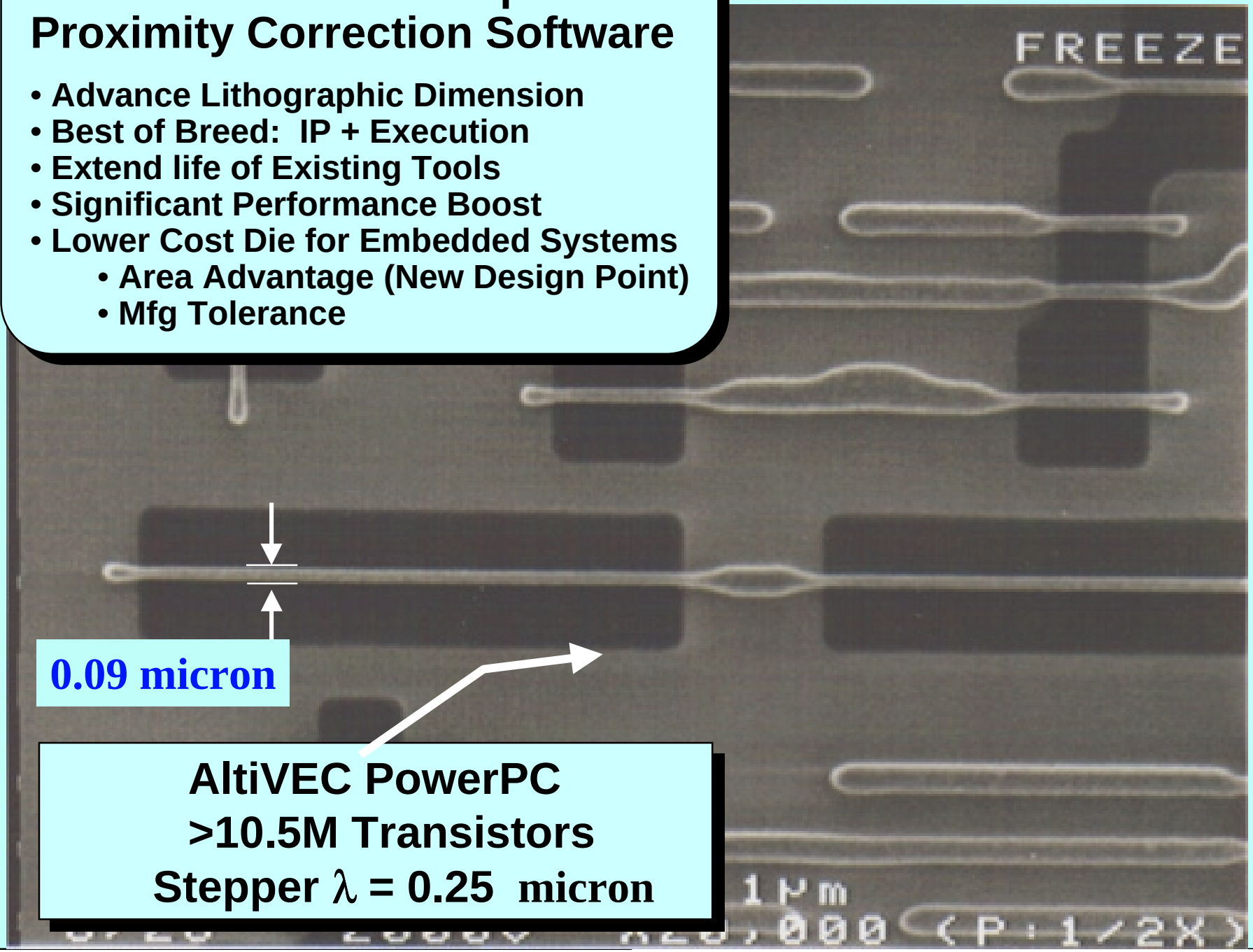


Chart Courtesy of Numerical Technologies, Inc.

Phase Shift Mask & Optical Proximity Correction Software

- Advance Lithographic Dimension
- Best of Breed: IP + Execution
- Extend life of Existing Tools
- Significant Performance Boost
- Lower Cost Die for Embedded Systems
  - Area Advantage (New Design Point)
  - Mfg Tolerance

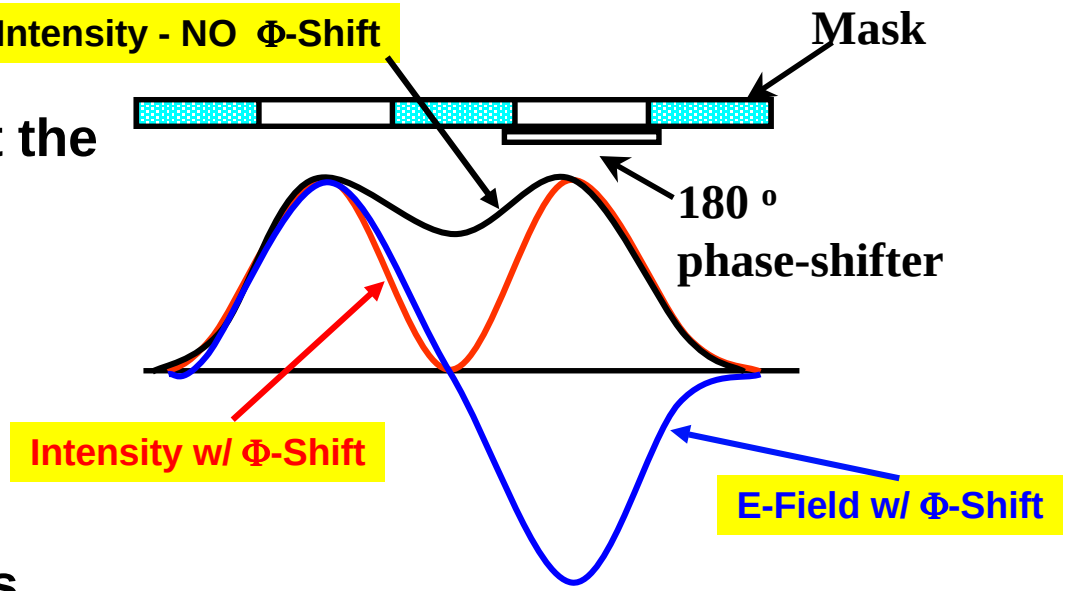


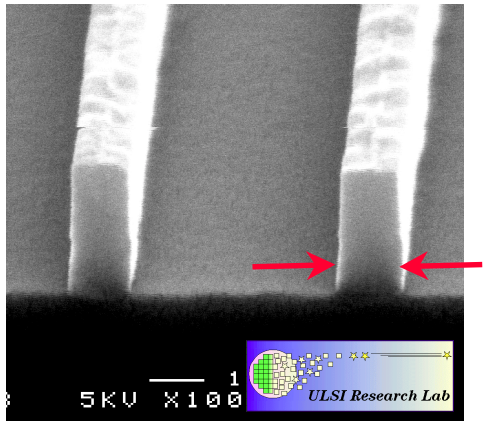
Phase Shift Greatly Improves Gate Image Definition

Uses phase-modulation at the mask level to further the resolution capabilities of optical lithography

Benefits:

- **–Smaller feature sizes**
- **–Improved yield (process latitude)**
- **–Dramatically extended useful life of current equipment**
- **– Performance Boost**
- **– Chip Area/Cost Advantage for Embedded Systems**





0.11µm

Printed using a ~0.18 µm nominal process