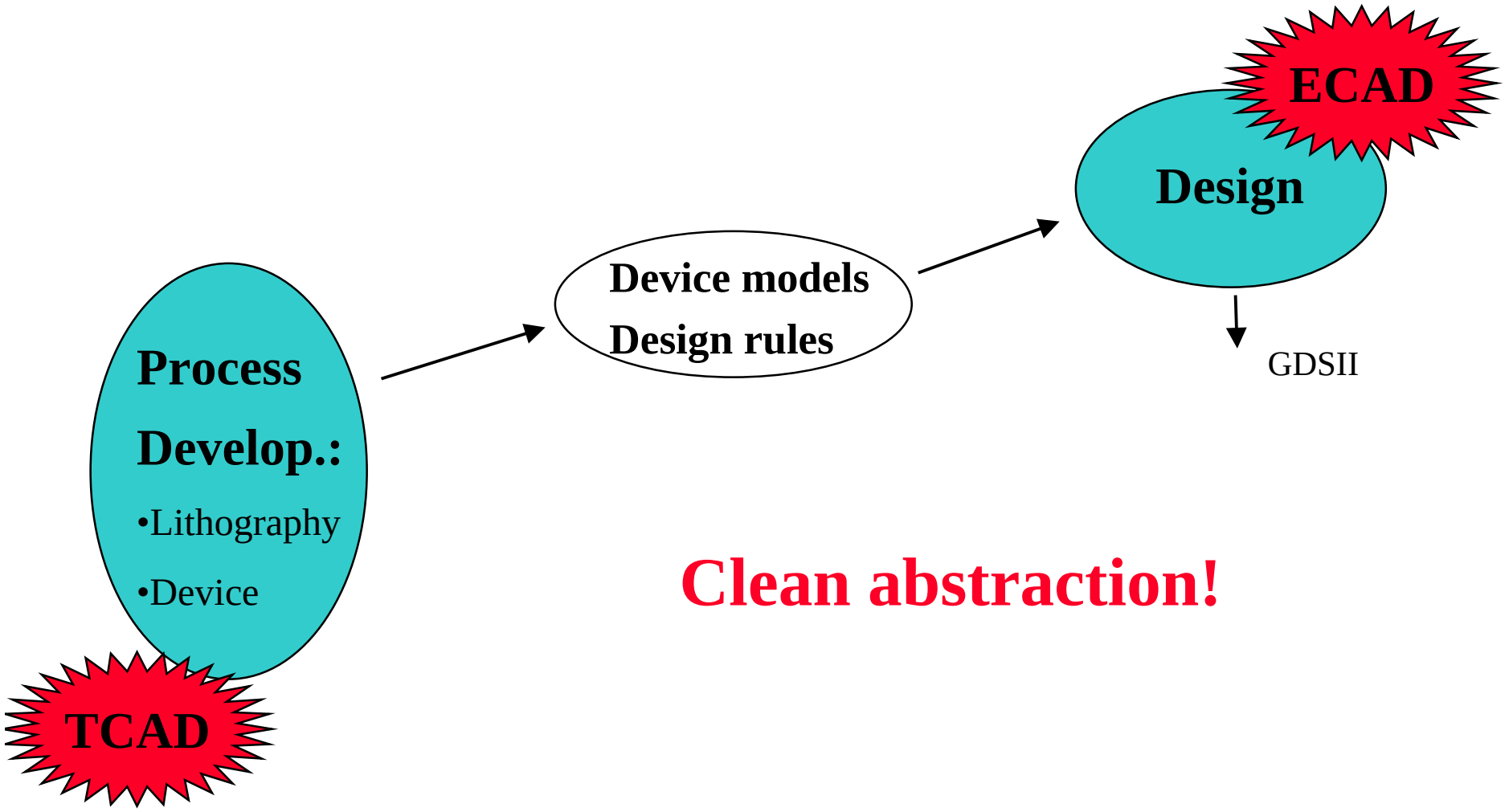
Sub-Wavelength Litho and EDA: Panel Context

Andrew B. Kahng

DAC-99 Session 45

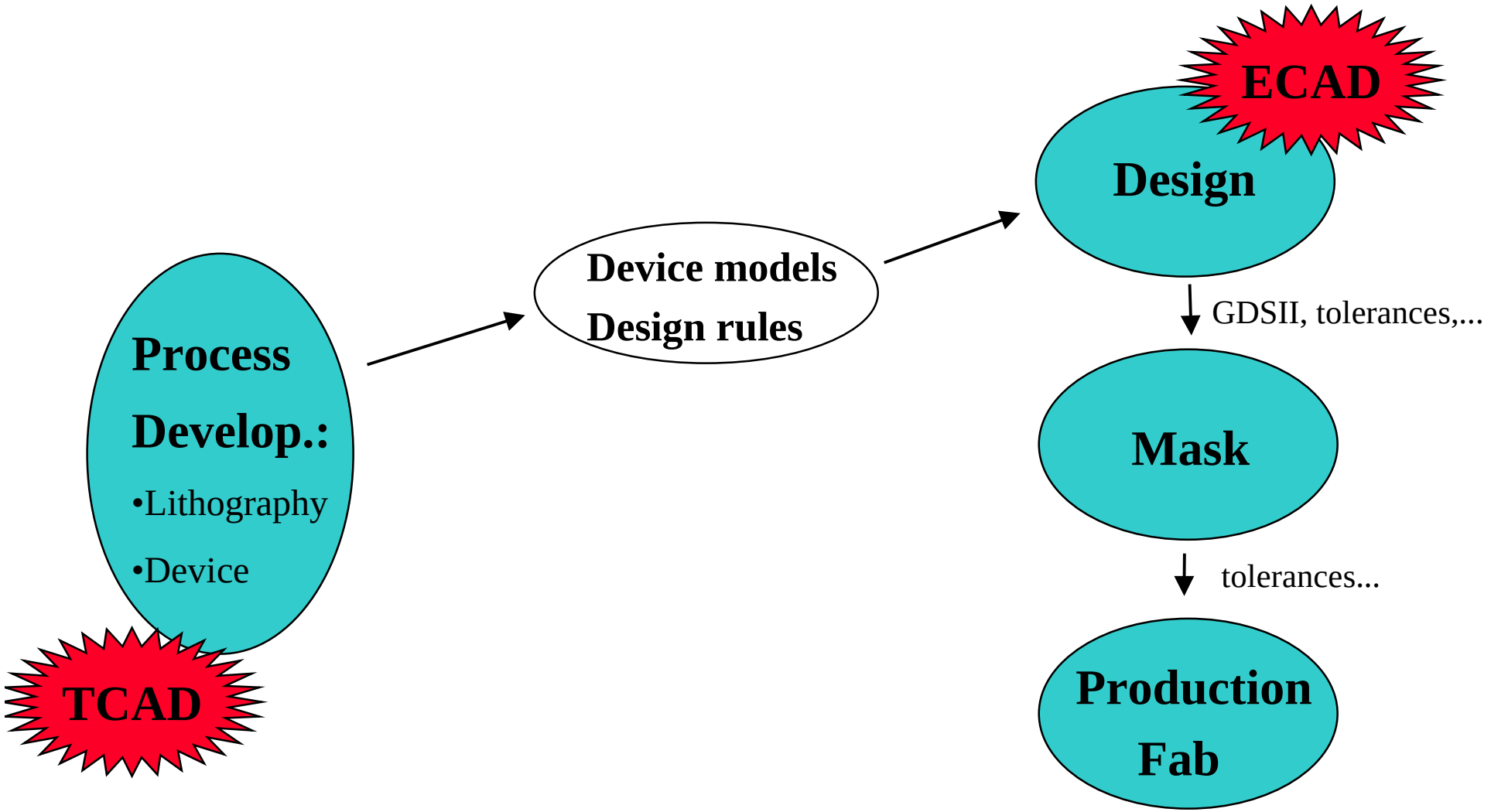
June 24, 1999

What does EDA know about process?

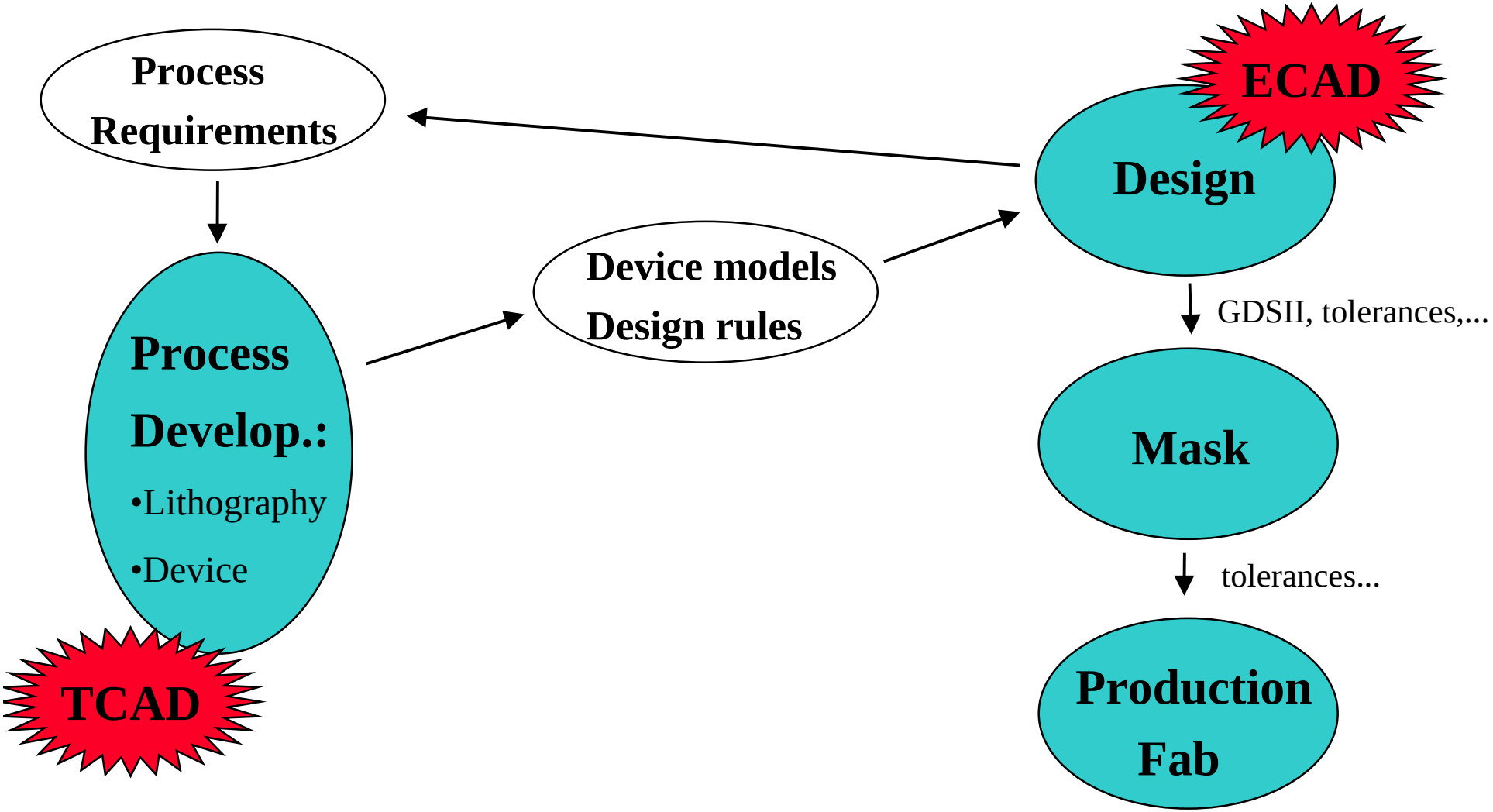


Clean abstraction!

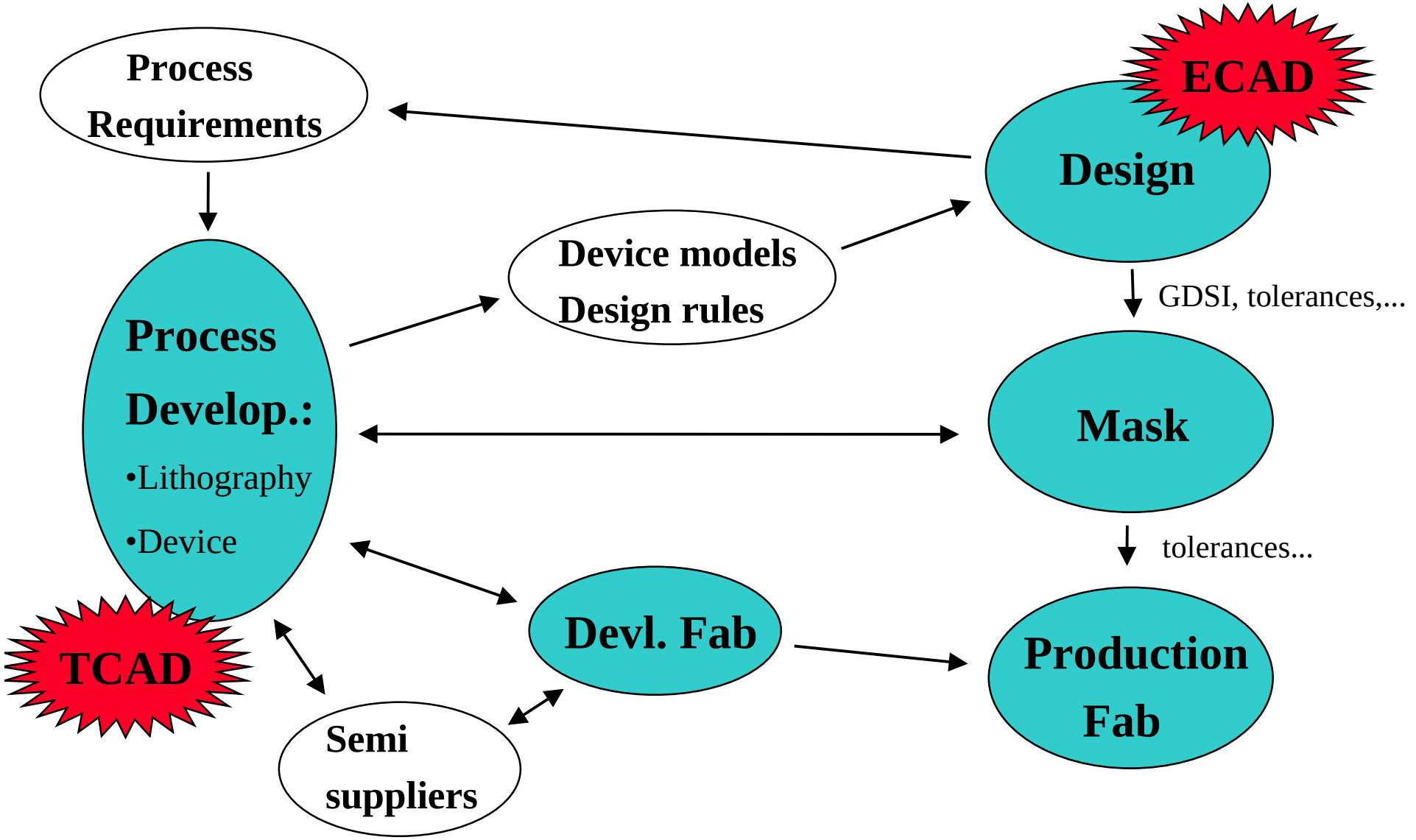
But design is just the start...



Design drives process development



Developmental fab in tight loop



Sub-Wavelength Litho Issues

- **Clean abstractions of process**
  - **OPC: a “rectangle” has 26 edges in 3 polygons**
  - **PSM: cell layouts and legal routes not freely composable**

Sub-Wavelength Litho Issues

- **Mask inspection / validation bottleneck**
  - **if Layout ≠ Silicon but the circuit is still functional… is it really an error ?**
  - **must the Design ↔ Mask boundary change ?**

Sub-Wavelength Litho Issues

- **Tool flow**
  - **line end extensions in the router**
  - **hammerheads in the library generator**
  - **OPC insertion in physical verification**
  - **RC extraction for timing signoff in P&R**
  - **post-P&R density control (filling and cheesing)**

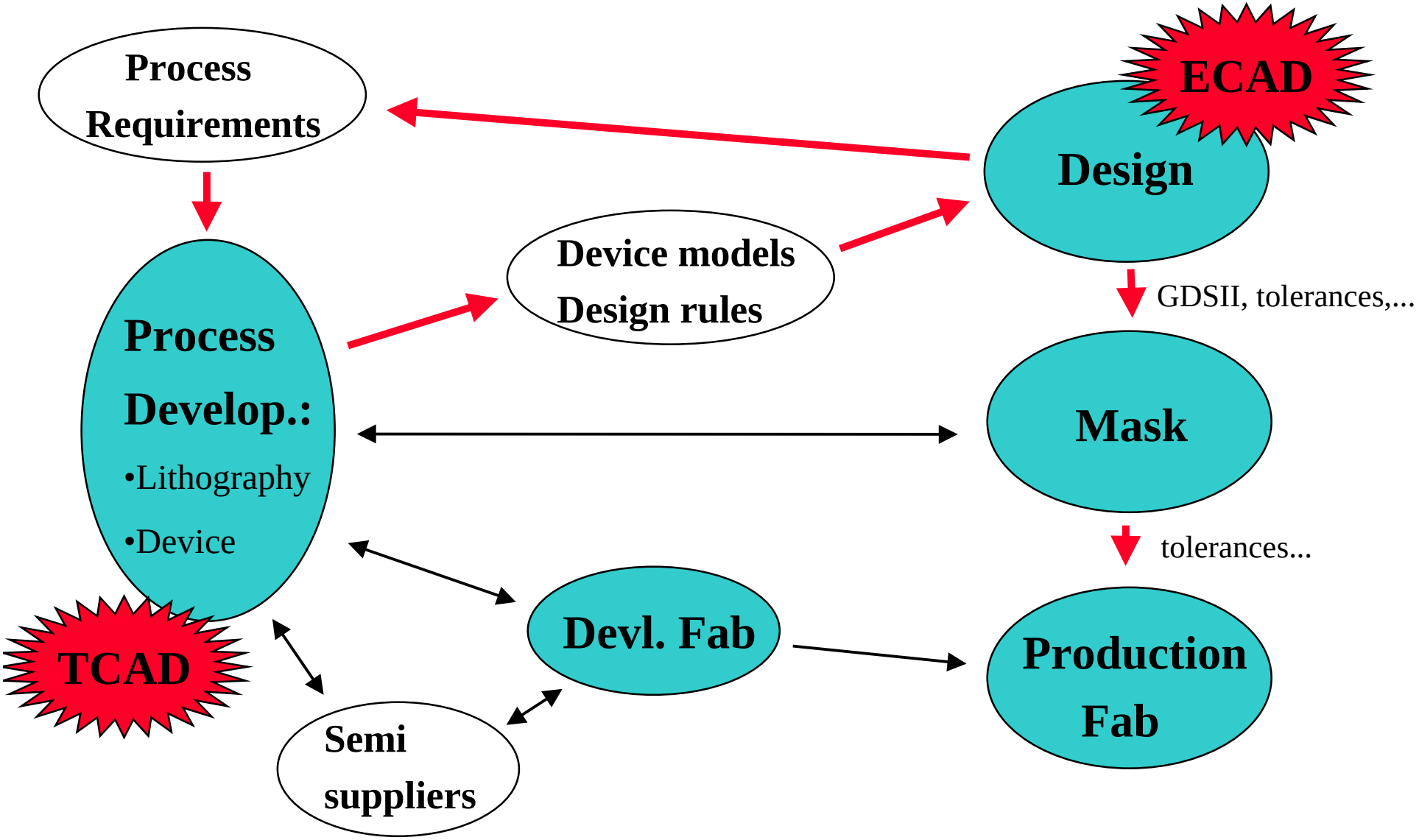
Sub-Wavelength Litho Issues

- **“Life changes” for circuit and layout designers**
  - **only particular geometries and pitches ?**
  - **self-adapting circuits ?**
  - **huge verification guardbands ?**
  - **reuse-based design at risk -- at all levels ?**

Sub-Wavelength Litho Issues

- **Partial ownership of the problem = no ownership ?**
  - **when designs fail, who owns the scrap ?**

Structure


Process Requirements
ECAD
Design
Device models
Design rules
GDSII, tolerances,...
Process Develop.:
•Lithography
•Device
Mask
tolerances...
TCAD
Devl. Fab
Production Fab
Semi suppliers

Panelists

- Mark Lavin, IBM
- Warren Grobman, Motorola
- Lance Glasser, KLA-Tencor
- Kenneth Rousseau, Synopsys
- Buno Pati, Numerical Technologies
- Robert Pack, Cadence Design Systems

- 5-minute position statements
- 30 minutes of moderated discussion