Andrew Kahng and Matthew Morrison on Industry and Academia

I attended two presentations on the academic track at the recent Cadence-LIVE Americas. The first was Andrew Kahng's presentation *A 'Life Cycle' of Teaching and Research on EDA and IC Implementation Methodology*. The second was Matthew Morrison's presentation *Challenges and Successes of a Cloud-Based High-Level Synthesis Course in a Virtual Environment*.

I've known Andrew for over 20 years. It has to be a long time since he was at UCLA at the time, and he's been at UCSD since 2001. Back when I was last at Cadence, one of my responsibilities was to run our TAB, our Technology Advisory Board. Andrew was one of the members, having spent a year just a short time before, as a visiting professor at Cadence on sabbatical from UCLA.

Andrew has shown up many times on Breakfast Bytes:

- Andrew Kahng on Industry-Academia Cooperation
- Andrew Kahng on PPAC Scaling Below 7nm
- Andrew Kahng on the Last Semiconductor Scaling Levers
- OpenROAD: Open-Source EDA from RTL to GDSII
I don't know Matthew well, although I have met him a couple of times. The first time was when he and a couple of his students presented a project at CDNLive when he was at the University of Mississippi. He then moved to the University of Notre Dame (as someone who speaks French, I can't help but cringe at some of the ways this gets pronounced). I met him at DAC last year (2019) and he has a walk-on part in my post Cadence Cloud Passport Partner Program. I talked to him because he was doing a pilot program with CMC, AWS, and Cadence about using EDA in the cloud in the classroom. This turned out to be prescient when everything had to switch to distance learning. Matt was also planning a workshop at DAC (along with Cadence) on High-Level Synthesis (HLS). Read on to find out how that went.

Andrew Kahng

This is what Andrew calls the "lifecycle" for industry-academic cooperation. Industry supplies tools, problems, and grant money. At the university, students are trained, and many of them go on to be masters or PhD students doing some research, too. Those students become interns and then full-time employees in industry. Rinse and repeat. Andrew said that of his PhD graduates, at some point in their careers 40% end up at Cadence, and about 20% end up at Qualcomm (who are also located in San Diego, as you probably know). To give you an idea of the scale of Andrew's graduate class, there are over 130 MS and PhD students enrolled for Winter 2020.
Andrew's research focus is physical design, and so naturally, that is the focus of the research students, too: back-end IC implementation, PPA, and tools/methodology issues. Students in his ASIC Implementation class are required to take some Cadence training courses too, what Andrew calls "readiness for job". Those courses are Innovus block-level, Basic STA, Tempus Signoff, Genus. The contents of Andrew's courses are regularly updated for relevance, with the latest updates to content being machine learning, 3D-IC, power planning, and the chip-package interface. These are all topics I write about regularly, for the same reason: they are on the new stuff moving into the current and next generation of SoCs.

Andrew went on to describe some of the research projects that he and his team have worked on. They generally use Cadence tools (Andrew said they have "hundreds of copies of Innovus"). Obviously his PhD graduates don't end up at Cadence just because they know how to use the tools, they end up here because it is a great place to work. But I can't but believe it helps to know how to run the Cadence physical flow, and probably have become a power-user.

Andrew finished up with some of his beliefs:

- There is synergy between teaching and research
- Life cycle: faculty + course + lab + industry engagement
- Tools + commercial training modules strengthen the course
- Tools are inseparable from research and you can't do research without access

But he believes we can do even better:

- Run more contests. They are relatively cheap to organize and host (his students organized the ICCAD19 global routing contest), and they have long-lasting impacts on faculty, courses, and research efforts
- Share more real-life problems to give students a sense of what are real-life challenges, and to make courses and projects more meaningful (and it's a great filter to identify students who have a passion and talent to work on real-world problems)
- Work together to create an even more virtuous lifecycle for our field.

Matthew Morrison
Matt is more focused on undergraduate education than on leading-edge research. Or perhaps a better way to put it is that he is doing research into how to do semiconductor design education in the modern era of cloud computing, and using high-level synthesis to let students achieve more in a short time.

Matt started by outlining the advantages of using HLS. I'm going to skip that since I've covered it before. For example, see Designing a Wi-Fi HaLow Baseband in Less than Six Months or Building Neural Networks with High-Level Synthesis.

But there is a lack of undergraduate courses on electronic system-level design (ESLD). In the same way as Andrew's students get introduced to real-world physical design tools, at the front end there is a need to introduce students to state-of-the-art ESLD tools such as Stratus, Cadence's HLS product. In fact, there are just two universities in the world that offer such a course:

- Columbia University – CSEE W4848 – System-on-Chip Platforms
- University of Notre Dame – CSE 40457 – High-Level Synthesis

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Above is the breakdown of what goes into Matt's CSE 40457 course at Notre Dame. Note that it is SystemC/TLM-based.

But things didn't go quite as planned.

Midway through the semester, COVID-19 hit. That over-stressed the campus servers. But, as I said above, Matt was working last year on a pilot program with CMC, AWS, and Cadence to host Cadence tools in the cloud. That pilot program suddenly became mainstream. Students could log in from anywhere in the country (world?) without needing to use a VPN. That is a problem at many universities (such as University of Mississippi where Matt was before) which don't allow students VPN access. Of course, EDA companies don't want their tools to be on completely open servers for just anyone to use, so that often students can only access the tools when they are physically on site. So the cloud solution, even absent distance learning, has a lot of attraction.

Matt was also organizing a summer school at DAC along with Cadence. The original plan had been to have 50 students on the course on site in San Francisco (where DAC was planned this year). When the conference went online, DAC said that they wanted any student who chose to be able to enroll. So suddenly there were 421 students. In the end, something over 200 students actually showed up and took the course. They all were able to synthesize a convolutional neural network for image detection. This is a first to run a course at this scale using Stratus HLS (and other tools) running in the cloud.

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